Bifurcation Analysis of Stabilization Circuits in an L-Band LDMOS 60-W Power Amplifier

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***Abstract*—In this letter, the global stability analysis of an L–band push-pull power amplifier is presented. The analysis is carried out for the amplifier operating in different modes, such as Class AB, Class B, and Class E/F, considering variations in the bias voltages, the input power and the input frequency. After determination of the oscillation mode, three different stabilization techniques are applied and compared: feedback resistors, neutralization capacitors, and odd-mode stabilization resistor. The element values of each stabilization network, ensuring a stable behavior for all the operating conditions, are calculated with a bifurcation-analysis technique. Good agreement is found between measured and simulated results.**

***Index Terms*—Bifurcation, push-pull power amplifier, stability analysis, stabilization.**

I. Introduction

POWER amplifiers are likely to exhibit instabilities, leading to oscillations at sub-harmonic or incommensurate frequencies [1]–[5]. The oscillations can be associated with negative resistance exhibited by the nonlinear capacitances, and also to gain increase versus the input power and undesired feedback. These oscillations, occurring from a certain level of input power, cannot be detected with conventional techniques, based on the k-factor. Their prediction requires a large-signal stability analysis of the steady-state solution. Different techniques [1]–[5], based on harmonic balance (HB), have been proposed for this analysis. In case of variation of circuit parameters, the boundary between stable and unstable operation can be efficiently determined through bifurcation detection on HB [1], [5]. In general, the amplifier will operate under different values of bias voltages and different input frequency and power, so the bifurcation analysis should be carried out in terms of all significant operation parameters. This global analysis will be applied here to a push-pull power amplifier, in the band from 1.1 to 1.3 GHz. The actual design goal will be the stabilization of the amplifier, and the knowledge of the instability regions in the parameter space, together with the analysis of the oscillation mode, will be helpful to devise a proper stabilization technique. Three different techniques will be considered here, based on the use of odd-mode stabilization resistor, neutralization capacitors, and feedback resistors. The use of bifurcation analysis enables efficient determination of the element values of each stabilization network. The performances of the resulting stabilized amplifiers will be compared, in terms of output power and efficiency.

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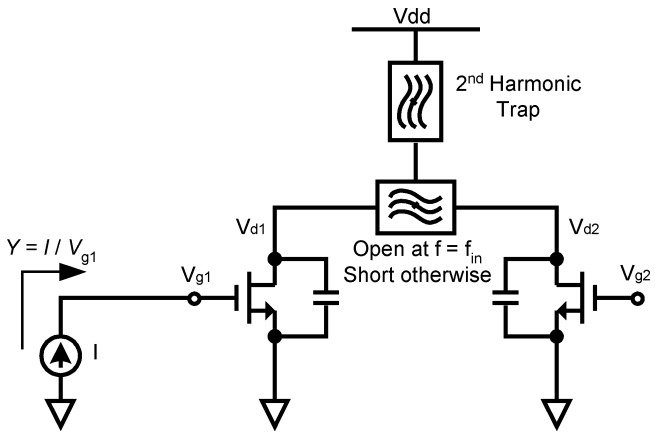

Fig. 1. Simplified schematic of the Class $\mathrm{E/F_{odd,2}}$ amplifier.

II. Stability Analysis of the Push-Pull Amplifier

Fig. 1 shows the simplified schematic of our push-pull amplifier. The amplifier is optimized for a Class-$\mathrm{E/F_{odd,2}}$ operation [6], [7]. When backing off from deep nonlinear regions, it can also be operated in other modes, such as Class AB, and Class B. When operating in the Class-$\mathrm{E/F_{odd,2}}$ mode, this amplifier has zero-voltage switching like a Class-E amplifier, while the odd harmonics and the second harmonic are terminated like a Class-$\mathrm{F^{-1}}$ amplifier.

The amplifier contains four parameters that can be varied: gate-bias voltage V_{G}, drain-bias voltage V_{D}, input power P_{in}, and input frequency f_{in}. For some operation conditions, the pole-zero identification technique [2] predicts an oscillation at about 200 MHz. For a global determination of the unstable operation ranges on HB, a bifurcation-analysis technique will be used, providing the oscillation boundaries in terms of V_{G}, V_{D}, P_{in}, and f_{in}. A small-signal current generator i_{s} at the frequency f_{a}, nonharmonically related with the input-drive frequency f_{in}, is introduced into the circuit at the gate terminal of one of the transistors. The generator enables the definition of an admittance function Y, given by the current-voltage ratio, which is calculated with the conversion-matrix approach [4]. Then, the bifurcation condition is given by $Y = 0$. First, the plane defined by f_{in} and P_{in} is considered. For a given V_{D} and V_{G} the oscillation boundary is obtained from

$$Y\left(f_{\mathrm{a}}, P_{\mathrm{in}}, f_{\mathrm{in}}\right) = 0. \tag{1}$$

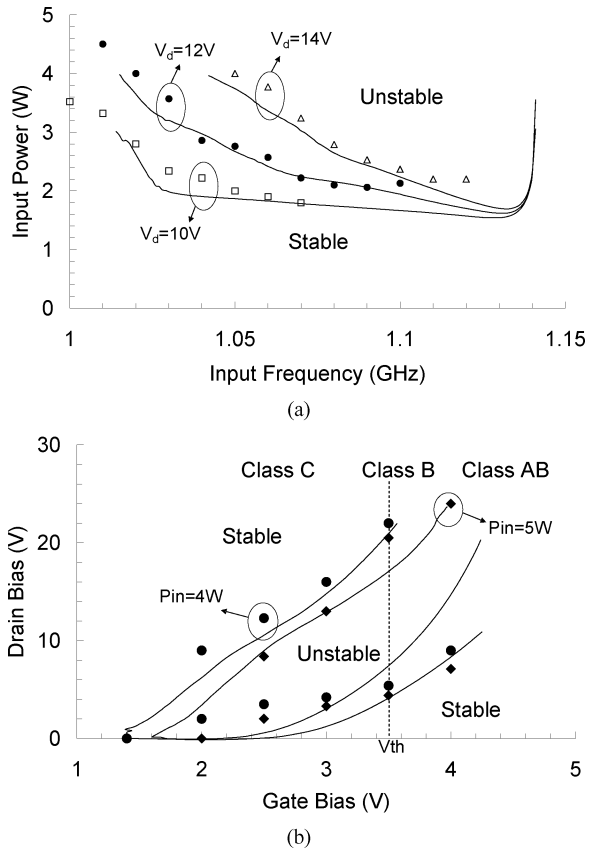

Fig. 2. Boundaries between the stable and unstable regions based on global-stability analysis of the amplifier, for different operation conditions. Lines indicate simulation results, and markers indicate measurement points. (a) In the plane defined by $f_{\rm in}$ and $P_{\rm in}$. (b) In the plane defined by $V_{\rm G}$ and $V_{\rm D}$.

The above system is solved through error-minimization or optimization procedures, combining HB and the conversion-matrix approach. The analysis is performed for different $V_{\rm D}$ and constant $V_{\rm G} = 3$ V, obtaining the loci of Fig. 2(a). The frequency $f_{\rm in}$ is swept, calculating, at each step, $P_{\rm in}$ and the oscillation frequency $f_{\rm a}$, which varies along the locus. As confirmed by pole-zero identification, the instability occurs at medium input power, where the gain is the highest. As the drain-bias voltage increases, the instability region shrinks due to reduced feedback through the gate-drain capacitance ($C_{\rm gd}$). For $f_{\rm in} > 1.14$ GHz, no instability is obtained at any of the considered bias voltages. Measurements are superimposed.

The second analysis is carried out in the plane defined by $V_{\rm G}$ and $V_{\rm D}$ [see Fig. 2(b)] solving

$$Y\left(f_{\rm a}, V_{\rm G}, V_{\rm D}\right) = 0. \tag{2}$$

Constant $f_{\rm in} = 1.03$ GHz and two typical operation $P_{\rm in}$ values have been considered, with the results of Fig. 2(b). In agreement with the pole-zero identification technique, the amplifier is unstable inside the different loci. The unstable behavior is observed in different operating modes: Class AB, Class B, and Class C. However, the instability region is smaller for the Class-C operation, which corresponds to lower $V_{\rm G}$. At higher $V_{\rm D}$, oscillation vanishes due to smaller feedback capacitance.

TABLE I
PHASES OF VOLTAGES AT THE GATE AND DRAIN TERMINALS

	V_{g1}	V_{g2}	V_{d1}	V_{d2}
$f_{\rm a}$ (200 MHz)	0°	180°	−98°	72°
$f_{\rm in}$ (1030 MHz)	−137°	43°	−84°	96°

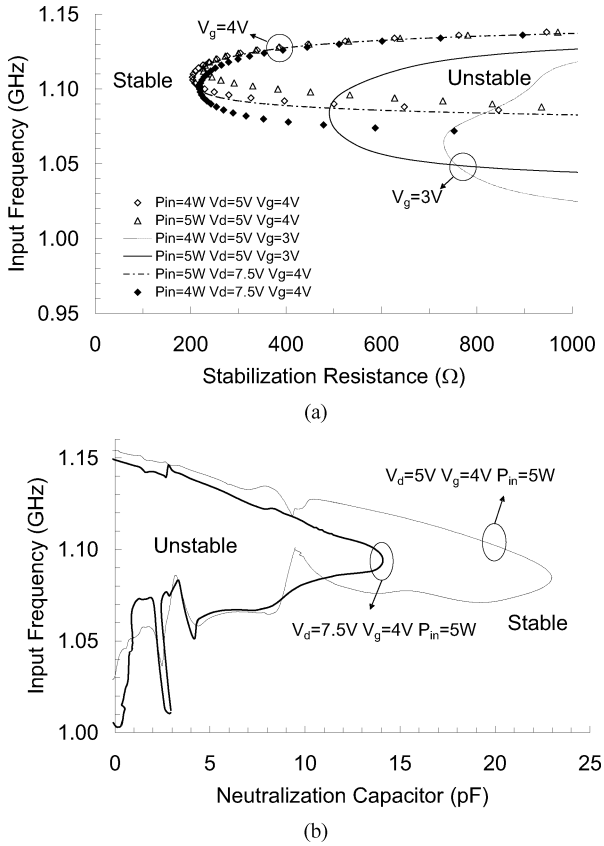

Fig. 3. (a) Stabilization with an odd-mode stabilization resistor. Typical operation conditions have been considered in these simulations. (b) Stabilization with neutralization capacitors using bifurcation loci.

III. STABILIZATION TECHNIQUES

The nature of the oscillation has been investigated obtaining the steady-state solution within the unstable regions, where the amplifier behaves as a self-oscillating mixer, at the two fundamental frequencies $f_{\rm in}$ and $f_{\rm a}$. An auxiliary generator (AG) has been used, in order to avoid the HB convergence to the unstable periodic solution at $f_{\rm in}$ [1]. The transistor harmonic voltages at the input-drive and oscillation frequencies are compared in Table I, for $V_{\rm G} = 3.5$ V, $V_{\rm D} = 7$ V, $P_{\rm in} = 3$ W, $f_{\rm in} = 1030$ MHz. The voltages exhibit a phase difference close to 180° at both $f_{\rm in}$ and $f_{\rm a}$. Thus, there is an odd-mode oscillation. In the following, three different stabilization techniques will be considered.

A. Stabilization With an Odd-Mode Stabilization Resistor

The odd-mode oscillation can be eliminated through the connection of a resistor between the gate terminals of the two transistors. The maximum allowed value for the stabilization resistor R is obtained by tracing the oscillation boundary in the plane defined by R and one of the four circuit parameters. In

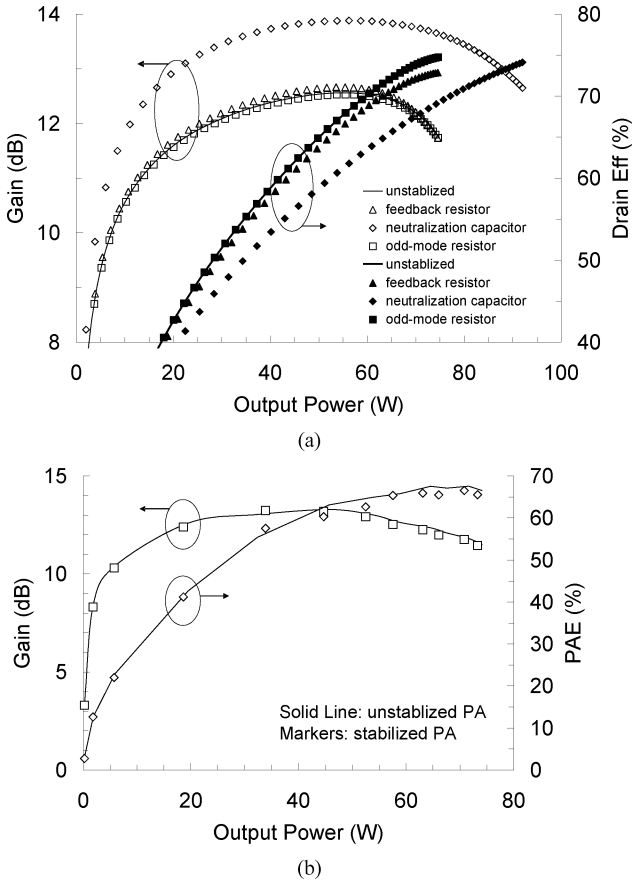

Fig. 4. (a) Simulated amplifier performance after applying three different stabilization techniques. (b) Measured amplifier performance before and after applying odd-mode stabilization resistor of 150 Ω.

the analysis of Fig. 3(a), the considered parameter is $f_{\rm in}$ and the oscillation boundary is determined for different $P_{\rm in}$ and bias values. The amplifier is unstable on the right-hand side of the represented loci. Note that the selected bias values correspond to the edges of the operation intervals. Due to the continuity of the system, this provides information about the required resistance for a general stabilization of the amplifier, for all the operation conditions. In order to avoid the instability, the amplifier must operate outside the instability regions for all the $f_{\rm in}$ values. Thus, the maximum allowed value for the stabilization resistance is 200 Ω.

B. Stabilization With Neutralization Capacitors

In push-pull configurations, neutralization capacitors can be connected between the gate and drain terminals of the opposite transistors to cancel undesired feedback through $C_{\rm gd}$. Effectively, a negative capacitance is added in parallel. To determine the minimum capacitance value required for stable operation, the oscillation boundary will be traced on the plane defined by $C_{\rm n}$ and $f_{\rm in}$, considering different $P_{\rm in}$ values and bias conditions. For clarity, only two loci have been represented in Fig. 3(b). To ensure stable behavior for all the operating conditions, the entire set of bifurcation loci must be taken into account. From this global analysis, the neutralization capacitance should be larger than 25 pF.

C. Stabilization With Feedback Resistors

In order to reduce the positive feedback, a resistor and a dc-blocking capacitor are connected between the gate and the drain terminals of the same transistor. Only limited power is dissipated, as parasitic inductances of the two elements provide high impedance at $f_{\rm in}$, which is about five times the oscillation frequency. These parasitic inductances do not have a significant effect on the feedback resistance at $f_{\rm a}$. The bifurcation-analysis technique indicates the maximum value of stabilization resistance of 90 Ω.

D. Comparison of Performance

Fig. 4(a) shows the comparison of the stabilized-amplifier performance for the three different stabilization techniques. The resistive stabilization techniques show little change in performance. The neutralization capacitors improve the gain of the amplifier by about 2 dB, but the PAE is reduced by 6%. In this particular amplifier, neutralization is not easy to implement due to layout constraints. The odd-mode resistor is implemented in the amplifier. Fig. 4(b) shows the gain and the PAE at 1210 MHz before and after applying the odd-mode stabilization. The measured performances are almost identical.

IV. Conclusion

In this letter, the global stability analysis of an LDMOS amplifier has been presented. Four parameters–two bias voltages, the input power and the input frequency–have been considered. After determination of the oscillation mode, three different stabilization techniques have been compared. For each approach, the values of the stabilization elements ensuring stable behavior for all the operation conditions have been determined through bifurcation analysis.

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References

[1] A. Suárez and R. Queré, *Global Stability Analysis of Microwave Circuits*. Boston, MA: Artech House, 2003.

[2] A. Anakabe, J. M. Collantes, J. Portilla, J. Jugo, S. Mons, A. Mallet, and L. Lapierre, "Analysis of odd-mode parametric oscillations in HBT multi-stage power amplifiers," in *Proc. EuMW 11th GAAS Symp.*, Munich, Germany, Oct. 2003, pp. .533–536.

[3] A. Collado, F. Ramírez, and A. Suárez, "Analysis and stabilization tools for microwave amplifiers," in *IEEE MTT-S Int. Dig.*, Fort Worth, TX, Jun. 2004, pp. .945–948.

[4] S. Jeon, A. Suárez, and D. B. Rutledge, "Global stability analysis and stabilization of a class-E/F amplifier," *IEEE Trans. Microw. Theory Tech.*, to be published.

[5] ——, "Analysis and elimination of hysteresis and noisy precursors in power amplifiers," *IEEE Trans. Microw. Theory Tech.*, to be published.

[6] S. Kee, I. Aoki, A. Hajimiri, and D. B. Rutledge, "The class-E/F family of ZVS switching amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 6, pp. 1677–1690, Jun. 2003.

[7] F. Wang and D. B. Rutledge, "A 60-W L-band class-$\mathrm{E/F_{odd,2}}$ LDMOS power amplifier using compact multilayered baluns," in *Proc. IEEE Topical Workshop Power Amplifiers for Wireless Communications*, San Diego, CA, Sep. 2004.