The unknown equivalent electric current on the dipole surface

![Graph](image)

**Fig. 3** Input impedances for half-split CDRA

- a $T_{E_{01}}$ mode with $x_1 = 1.6cm$, $z_0 = 0cm$, and $l_1 = 1.25cm$
- b $HEM_{11}$ mode with $x_2 = 0.02cm$, and $l_2 = 0.838cm$

is modelled as piecewise linear subdomain functions [3]. After application of a Galerkin procedure to the integral equations, the resulting MoM matrix is solved for the current distribution on the wire and the input impedance is computed from the current at the driving source. Other parameters such as the radiation pattern and the near field distribution can also be obtained.

**Numerical results:** Excitation of the $T_{E_{01}}$ mode of the antenna of Fig. 1 will result in a broadside radiation pattern. This broadside radiation pattern is similar to the radiation pattern of a narrow slot in a ground plane. Excitation of the $HEM_{11}$ mode results in a radiation pattern with a null along the $y$-axis. The radiation pattern with a null along the $y$-axis.

The computed resonance frequencies and the radiation $Q$ factors were computed in the complex plane without excitation and are, respectively, 2.033GHz and 7.7 for the $T_{E_{01}}$ and 3.021GHz and 6.25, for the $HEM_{11}$ mode.

**Summary:** A numerical design tool has been used to design a half-split CDR antenna excited by a coaxial probe which promises improved bandwidth, radiation efficiency, and power handling capabilities as compared to conventional microstrip and slot-coupled transmission line antennas. Although results were presented only for the $T_{E_{01}}$ and $HEM_{11}$ modes, other quasi-TE modes can be excited using this configuration.

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**References**


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**Computing centroids in current-mode technique**

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**Indexing terms:** Circuit design, Analogue computer circuits

A novel current-mode circuit for calculating the centre of mass of a discrete distribution of currents is described. It is simple and compact, an ideal building block for VLSI analogue IC design. The design principles are presented as well as the simulated behaviour of a one-dimensional implementation.

**Introduction:** The idea of using resistive sheet or grids of linear resistors to determine the position of objects, in contrast to previous designs, is to be as compact as possible and to provide an ideal building block for VLSI application. However, a number of difficulties remain:

(i) so far, linear resistive sheet implementations require either complex area-expensive circuitry, or technology-dependent solutions that are not electronically tunable;

(ii) the computation of the centroid often requires off-chip processing using sophisticated buffers;

(iii) they do not work well for very low levels of injected current, thus preventing direct interface of photoelectric detectors with resistive grids for low light levels.
The above-mentioned problems led us to investigate a new circuit technique using a current-mode approach [3]. This Letter presents a novel CMOS circuit using a current-mode subthreshold MOS approach [4] that is simple, requires little area, does not require off-chip processing, works well with small currents and has low power consumption.

To overcome this limitation we propose the solution described in the section on position calculation. A differential pair of transistors ID1 and ID2, with the output currents independently of the value of the node voltages. However, owing to the intrinsic differences of device characteristics, a sufficiently accurate matching of the boundary currents is difficult to achieve, making the position estimation through the function (I1 - I1)(I1 + I1) accurate only for high values of R and/or I. Thus the requirement to keep high is extremely important for low values of injected current, but hard to meet in VLSI by using either passive layers or complex circuit strategies. To overcome this limitation we propose the solution described in Fig. 1a, where each resistor has been substituted by a MOS transistor. Assuming the general current expression of an MOS transistor ID = K(VDS, VDS) it is easy to show that

\[ z = \frac{n - m}{L} \left( I_1 - I_1 \right) + \frac{2n + 1}{n + m} \frac{(V_2 - V_1)}{L} \left( I_1 + I_1 \right) \]

where n and m are the number of elements on the left- and right-hand sides of the injection node, R is the single-element resistance value and L is the half-length of the structure as illustrated in Fig. 1a. It can be seen from the above equation that if \( V_1 = V_2 \) the position may be calculated by means of a simple fractional function of the output currents independently of the value of the node voltages. However, owing to the intrinsic differences of device characteristics, a sufficiently accurate matching of the boundary currents is difficult to achieve, making the position estimation through the function (I1 - I1)(I1 + I1) accurate only for high values of R and/or I. Thus the requirement to keep high is extremely important for low values of injected current, but hard to meet in VLSI by using either passive layers or complex circuit strategies.

Circuit description. The well known idea underlying our position-sensitive device is described in Fig. 1a. For a discrete 1-D resistive network it may be proved that the relative position \( x/L \) of current injection is related to the boundary currents \( I_1, I_2 \) and voltages \( V_1, V_2 \) by the following expression:

\[ z = \frac{n - m}{L} \left( I_1 - I_1 \right) + \frac{2n + 1}{n + m} \frac{(V_2 - V_1)}{L} \left( I_1 + I_1 \right) \]

where \( n, m \) are the number of elements on the left- and right-hand sides of the injection node, \( R \) is the single-element resistance value and \( L \) is the half-length of the structure as illustrated in Fig. 1a. It can be seen from the above equation that if \( V_1 = V_2 \) the position may be calculated by means of a simple fractional function of the output currents independently of the value of the node voltages. However, owing to the intrinsic differences of device characteristics, a sufficiently accurate matching of the boundary currents is difficult to achieve, making the position estimation through the function (I1 - I1)(I1 + I1) accurate only for high values of R and/or I. Thus the requirement to keep high is extremely important for low values of injected current, but hard to meet in VLSI by using either passive layers or complex circuit strategies.

To overcome this limitation we propose the solution described in Fig. 1a, where each resistor has been substituted by a MOS transistor. Assuming the general current expression of an MOS transistor \( ID = K(VDS, VDS) \) it is easy to show that

\[ z = \frac{n - m}{L} \left( I_1 - I_1 \right) + \frac{2n + 1}{n + m} \frac{(V_2 - V_1)}{L} \left( I_1 + I_1 \right) \]

where \( K \) is the channel width to length ratio. Note that the current division technique is valid in all operating regions of an MOS transistor: weak and strong inversion, linear region and saturation as recently reported also in [5]. For example, referring all voltages to bulk, the value of \( f(VDS, VDS) \) for pMOS transistors working in weak or strong inversion is \( K(VDS, VDS) + VDS \) or \( 2n(VDS, VDS) + VDS \) respectively, where \( VDS \) could be either \( VDS \) or \( VDS \), \( K \) is the gate effectiveness coefficient, related to the body effect, and \( VDS \) is the thermal voltage. Furthermore, note that eqn. 2 is still consistent for MOSFETs in moderate inversion, whatever is the expression of \( f(VDS, VDS) \).

This implementation offers the capability of controlling the voltage-dependent term of eqn. 2 simply by adjusting the level of \( ID \), thus determining the resistivity of the network, which trades off time response for boundary offset cancellation. It is easy to see that for both networks, in the presence of multiple inputs and assuming \( V_1 = V_2 \), the output currents encode the normalised first moment \( z \) of the current distribution.

\[ z = \sum_{i=1}^{N} \frac{I_i}{L} \int_{-\infty}^{\infty} x f(x) dx \]

In order to calculate the \( (I_1 - I_1)(I_1 + I_1) \) function we propose using the translinear principle in a circuit with subthreshold MOSFETs (Fig. 2). Two current-controlled current conveyors consisting of the two pairs M0-M1 and M10-M11 ensure equal magnitude to \( ID \) and \( V_1 \) while the currents flowing out of the resistive network are delivered at the drain of \( M3 \) and \( M6 \), avoiding any current-mirror mismatch. Applying the translinear principle to the loop of \( M3, M4, M5 \) and \( M6 \) we can prove that \( I_1 = I_1 = I_2 = I_2 \) if \( f(VDS, VDS) \) is the translinear principle function normalised to the biasing current of the differential pair \( ID \). Finally, note that the above approach and the current-division technique are not directly constrained by power supply margins, an attractive feature for low-voltage applications.

Circuit evaluation. The proposed architecture has been simulated by using ANALOG [6] which is particularly tailored for evaluating MOSFET circuits working in mixed operating regions. A 13-node current divider, along with the proposed computational block, has been simulated with typical parameters of a general-purpose 2μm CMOS process. All transistors have the same size \( W/L = 4μm/4μm \) to ensure maximum compactness to the structure. In Fig. 3 the output current is plotted against the centre of mass position of the input distribution assuming a 50mV offset between \( V_1 \) and \( V_2 \). The circle marked characteristics belong to a three-current pattern whose centroid corresponds to the indicated node while the square marked characteristic is related to a four-current pattern whose centre of mass is aligned to an internode position. The circuit has been simulated for different values of \( VDS \) in the range 1.35-4.4V (voltages referred to ground) to evaluate the current division performance for different transistor operating regions and to analyse the offset cancellation effect as predicted by eqn. 2. Note that the linearity of the characteristic is not affected by the transistor working region, and that the offset effect gradually decreases for increasing values of \( VDS \). For all characteristics we have observed high linearity with correlation coefficient deviations below 0.01%. Fixing \( VDS \) in the range 1.5-4.4V, we then varied the total amount of input current over three decades, from 200nA (solid markers) to 20mA (open markers), obtaining a small variation (+1.5%) of static characteristics. The lower limit is set by the leakage currents of diffusions and the upper one by the strong
Conclusions: We have investigated a new technique for locating in analogue fashion the centre of mass of a discrete distribution of currents using current-mode concepts. The simulation results presented above, which exhibit high linearity characteristics over three decades of input values, indicate that this architecture has application versatility in the design of position-sensitive devices (PSD), current-mode subthreshold MOS circuits for analogue VLSI neutral systems, and mesh-type high-speed optical position-sensitive devices (MEPSDs).

References

Novel PLL-based clock distribution scheme
S.H.K. Embabi and K.I. Islam

A technique for minimising clock skew in VLSI chips and multichip modules is proposed. A phase-locked loop is used to tune the delay of the clock interconnects. The clock interconnects are skewed by the amount of that delay. If, however, a PLL is used as shown in Fig. 1, where the phase detector (PD) and the lowpass filter (LPF) are kept in the proximity of the clock source, the VCO is remotely located such that its output taps the line at its middle point \( c \) (i.e. \( L_1 = L_2 \)), the delays of the two halves will be equal. The clock at point \( c \) will be leading the clock at \( a \) (and \( b \)) by \( t_1 \) which is proportional to \( R_2C_2 \). The delay between point \( c \) and \( d \) is equal to that between \( c \) and \( e \). Hence, the skew between \( a \) and \( d \) is ideally zero as opposed to twice \( t_1 \) if the PLL is not used. By the same token, if the tapping point \( c \) is shifted to the right or left, an intentional skew can be introduced. For example, if \( L_1 > L_2 \), the delay between \( c \) and \( b \) will be greater than that between \( c \) and \( d \), hence, the clock at \( d \) leads the clock at \( a \) as shown in Fig. 1. This implies that the skew achieved is negative, which is an interesting result. The opposite case is also illustrated in Fig. 1. This approach can be used to tune the intra-element delay, an effect achieved by the individual sizing of buffers in the Friedman-Powell scheme [4]. Fig. 2 illustrates this application. Let us assume that the phase delays of functional elements \( FE \) and \( FE \) are \( t_{in} \) and \( t_{in} \), respectively, with \( t_{in} < t_{in} \). To avoid skewing between \( e_1 \) and \( e_2 \), the delay of the first interconnect (\( d \) to \( d_1 \)) should be larger than that of the second interconnect (\( a \) to \( d_2 \)). This requirement contradicts the fact the length of the first interconnect is shorter than that of the second. However, using negative skewing by proper positioning of the remote VCO, the clock at \( d_2 \) may be made to lead the reference \( c \) by \( t_1 \) and the clock at \( d_2 \) to lag the reference by \( t_2 \). The net result of this arrangement is that the clock at \( d_2 \) lags the clock at \( d_1 \) by \( t_2 - t_1 \), which is equal to \( t_1 - t_2 \). If \( t_1 \) equals \( t_{in} - t_{in} \), the skew between \( e_1 \) and \( e_2 \) is zero. The condition

Note 1: The phase delay is the maximum delay between the master clock source and any leaf node.