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Experimental and theoretical study of ultra-thin oxides

E S Daniel†, D Z-Y Ting†‡ and T C McGill†§

† T J Watson Sr Laboratory of Applied Physics, California Institute of Technology, Pasadena, CA 91125, USA
‡ Department of Physics, National Tsing Hua University, Hsinchu 30043, Taiwan

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Abstract. We report on an experimental and theoretical study of transport through thin oxides. The experimental study was carried out on the tunnel switch diode (TSD) which consists of an MOS junction on top of a pn junction. The properties of the TSD depends critically on the properties of the tunnel oxide layer. Our results indicate that these devices can exhibit two different modes of behaviour depending on the stress history of the oxide. An unstressed device exhibits a thyristor-like I–V characteristic with fairly low current density. As the oxide is stressed, however, the I–V characteristic discontinuously shifts into a higher-current thyristor-like mode in which current transport appears to be highly non-uniform and depends strongly on stress history. This suggests a possible structural change in the oxide layer which is not completely destructive in that the device continues to function. We present a possible theoretical model of such a structural change in which microscopic filaments are generated in the oxide. Calculations of J–V curves for such structures with varying filament heights qualitatively match stressed MOS I–V curves found in the literature and qualitatively explain the dual-mode behaviour of the TSD.

1. Introduction

Advanced metal–oxide–semiconductor (MOS) field-effect transistors and novel silicon-based devices require the use of ultrathin gate or tunnel oxides. As a result, transport and breakdown mechanisms in such oxides have been studied extensively in MOS structures, although these properties are still not completely well understood. It has been shown that the tunnel switch diode (TSD) device, consisting of an MOS junction on top of a pn junction, is quite sensitive to the transport properties of its thin oxide layer [1–3]. Therefore, studies of this device may reveal information concerning the oxide properties supplemental to that obtained in MOS research. Here, we present the stress-dependent behaviour of a set of TSD devices and we discuss the role of the oxide in determining this behaviour. The variation of these I–V characteristics has motivated the study of transport through non-uniform thin oxide layers. We present 3D quantum mechanical scattering calculations which allow theoretical investigation of the tunnelling properties of non-uniform oxides. In particular, we examine n-poly Si/oxide/p-Si devices with conducting filaments in an attempt to model stressed oxide behaviour.

§ Author to whom correspondence should be addressed.

2. Tunnel switch diode results

2.1. Background

The TSD, first discovered by Yamamoto in 1972 [4], consists of a stack of layers as shown in figure 1(a). If current is driven through these layers with negative bias on the gate, a thyristor-like I–V curve results, as shown in figure 1(b). For applied voltages between the peak and valley voltages, two stable current states are allowed. It has been demonstrated theoretically [2] and experimentally [1, 3] that this device relies critically on the oxide as a tunnel barrier. If the oxide is either too thin or too thick, the peak in the I–V curve disappears, and there is no range of voltage over which bistable current states may be supported.

Given that the TSD device is so sensitive to the oxide transmission properties, one would expect that the effects of electrical stress on the device would be primarily determined by the stress modification of the oxide layer. Typical MOS electrical stress studies, in which an MOS device is subjected to a constant current while the voltage is monitored over time, indicate that the oxide becomes more transmissive with time, as the voltage across the device drops [5, 6]. Initially, this increase in conductivity is gradual, and is often termed stress-induced leakage current (SILC). After some time, however, the conductivity increases sharply, indicating a 'breakdown', characterized by the total integrated charge per unit area which has

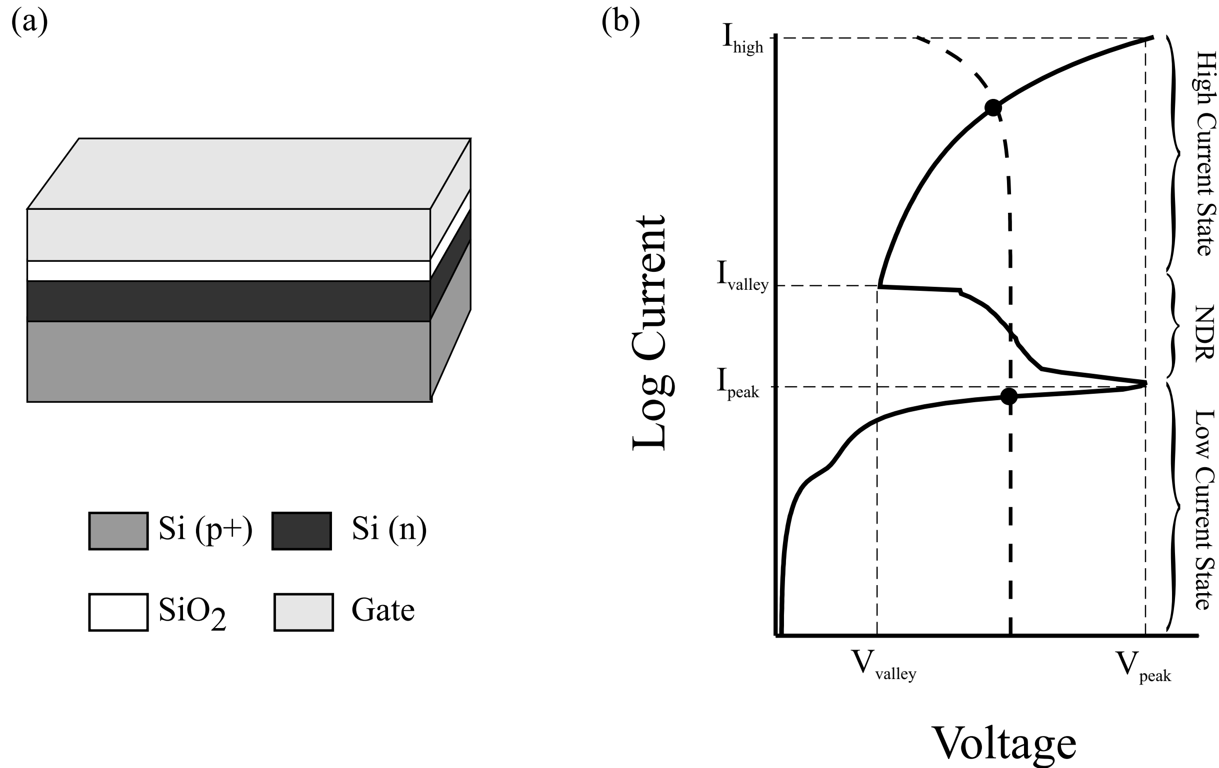

Figure 1. TSD. (*a*) The TSD device consists of a p$^+$-Si substrate with an n-Si epilayer, typically a few microns thick, a tunnel oxide (1.0–4.5 nm) and a conductive gate on top. (*b*) A typical measured I–V curve for a 2.5×10^{-5} cm^2 device plotted together with a 2.5 V, 10 Ω load line, illustrating the two stable current states. For this particular device, I_{high} = 100 mA, I_{valley} = 100 μA, I_{peak} = 9 μA, V_{valley} = 1 V and V_{peak} = 4 V.

permeated the device at this point, the charge to breakdown (Q_{bd}). Even though typical operation of the TSD device exposes the oxide to charge fluences much greater than typical Q_{bd} values, most reported studies of the TSD do not discuss any stress-related effects, except for an occasional mention of an initial 'forming' behaviour which occurs the first time the device is ever switched into the high-current state [3]. In this section, we present stress-dependent measurements of a set of TSD devices in an attempt to understand this behaviour.

2.2. Fabrication and measurement procedures

Wafers of size 6 in, consisting of p-type 2×10^{18} cm^{-3} substrates with n-type 2×10^{15} cm^{-3} epilayers, either 1.5 μm or 2.5 μ thick, were used. A field oxide was defined using a local oxidation of silicon procedure [7], and the thin tunnel oxide grown within the field oxide window. Samples with 2.0 nm, 2.5 nm, 3.5 nm and 4.5 nm oxides were prepared. Polysilicon gates (n type) were defined, covering the thin oxide region and extending onto the field oxide. Square devices with edges 85, 200, 500, 1320 μm were defined in this way. Roughly 1 μm of Al was deposited on the back surface of the wafers to provide the back contact.

Measurements of the devices were performed using an HP4145 parameter analyser connected to an Alessi probe station. Two probes were used for each measurement: one to source the current to the gate contact and the other to sense the voltage. This allowed elimination of probe contact resistance from the measurement. The contact resistance between the conducting probe station chuck and the wafer back contact was assumed to be negligible. As the HP4145 was operated as a current source rather than a voltage source, the entire I–V curve could be measured in one sweep without any hysteresis. Further processing and measurement details can be found elsewhere [8].

It was found that the act of measuring a single I–V curve over a current range such as that shown in figure 1(*b*) could significantly change the TSD behaviour, as evidenced by subsequent I–V curve measurements. As mentioned above, this 'forming' behaviour has been observed by others as well. In order to characterize better this forming process, a simple method was used, which proceeded as follows. A device which had never been subjected to electrical stress would be connected to the parameter analyser, and an I–V curve would be scanned from zero current to some small maximum current. This process yielded the 'virgin' scan. While this measurement proceeded, the stress induced by the measured currents may have modified the device. A subsequent scan to a slightly higher maximum current would then reveal a modified I–V curve, while further stressing the device. Another scan to a still higher maximum current could then be taken, and so on. This method, which we will refer to as 'incremental current stressing', was used to obtain sets of I–V curves for each device studied.

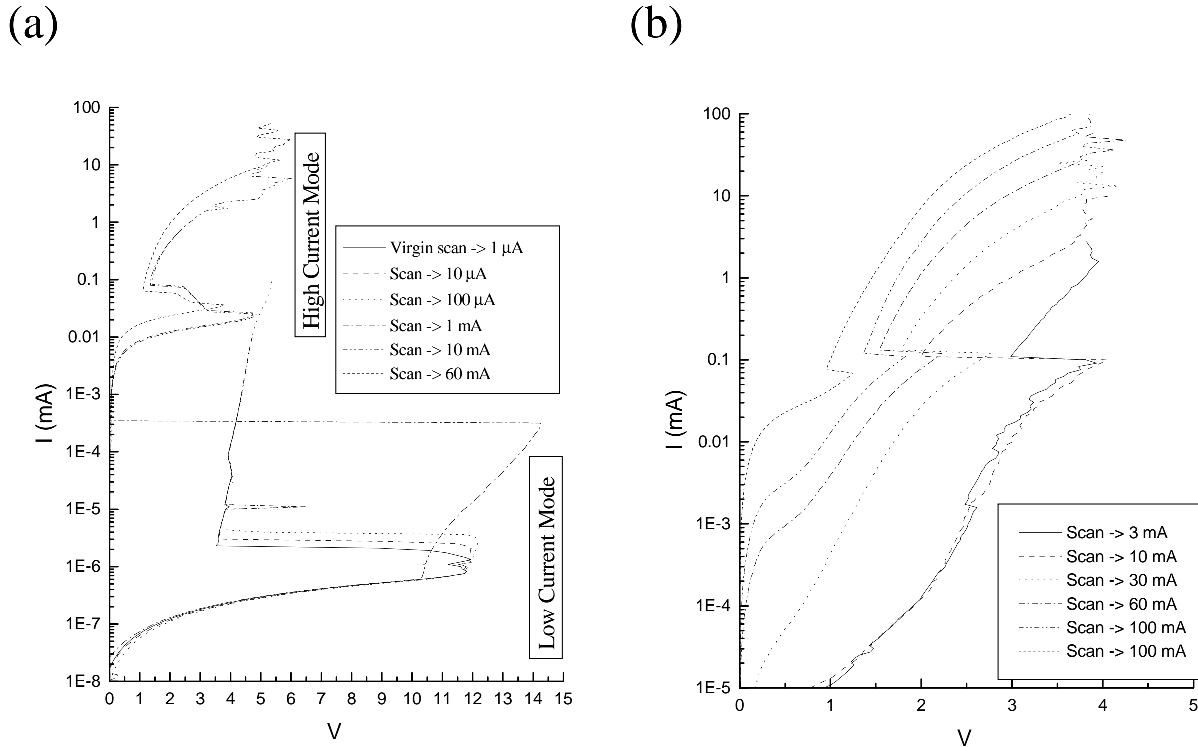

Figure 2. (*a*) Incremental current stress I–V curves for a 200 × 200 μm^2 TSD device with a 3.5 nm oxide layer and a 2.5 μm epilayer. The device exhibits two distinct 'modes' of operation, each of which can support low- and high-current states characteristic of the TSD. (*b*) Incremental current stress I–V curves for an 85 × 85 μm^2 device with a 2.0 nm oxide layer and a 1.5 μm epilayer, illustrating a voltage-limiting behaviour.

2.3. Results and discussion

Consider the incremental current stress curves shown in figure 2(*a*). The three lowest stress scans each sweep out a very low current bistable TSD I–V curve and are very nearly identical except for a slight increase in the switching current with stress. After a maximum current stress of 0.1 mA (corresponding to a voltage of $\sim$ 5.4 V), however, the I–V curve begins to change significantly. During the subsequent sweep, the voltage drops suddenly to zero in what appears to be some kind of breakdown but, as the sweep continues, a higher-current TSD I–V curve results, and remains (albeit modified) in subsequent scans. Thus, a 'low-current TSD mode' is observed when the device has been subjected to little or no stress, and a 'high-current TSD mode' abruptly takes over once some critical stress has been reached. Both 'modes' exhibit bistable current states for a range of voltage. This behaviour was observed in nearly all devices measured.

Note that there are several major differences between these two TSD modes. For example, the low-current mode does not change appreciably with incremental current stress until the device is forced into the high-current mode. The high-current mode, however, changes substantially with each incremental scan, and the oxide seems to become just conductive enough to limit the voltage to a fixed maximum of a few volts (see figure 2(*b*)). This limit voltage was found to decrease with decreasing oxide thickness, but the limiting electric field was not constant, as might be expected. Another difference is found in the shape of the high-current state in each of the two modes. The I–V curve in the high-current state of the low-current mode is exponential in shape (linear on the log–linear plot), and extremely steep, spanning nearly 5 orders of magnitude in current over a range of roughly 2 V. The high-current state of the high-current mode, however, does not have an exponential shape, and increases only 2 orders of magnitude over a range of a few volts, suggesting a somewhat different transport mechanism. Many more differences between the two TSD modes were found, as discussed elsewhere [8].

The relatively weak stress dependence and the exponential high-current state of the low-current mode of the TSD suggest that the oxide has not broken down and is in the SILC regime. Similarly, the high stress levels and the voltage-limiting behaviour of the high-current mode suggest that this mode results after the oxide has reached breakdown. If this is true, however, the fact that the device can support two current states in the high-current mode suggests that the broken-down oxide still acts as a partial barrier. In the next section, we explore one possible physical model which can reflect this behaviour.

3. Simulations of stressed MOS structures

3.1. Background

Non-uniformities in oxides are typically not treated theoretically because of the dramatically increased complexity and computational demands. However, they can have dramatic effects on the current–voltage characteristics of

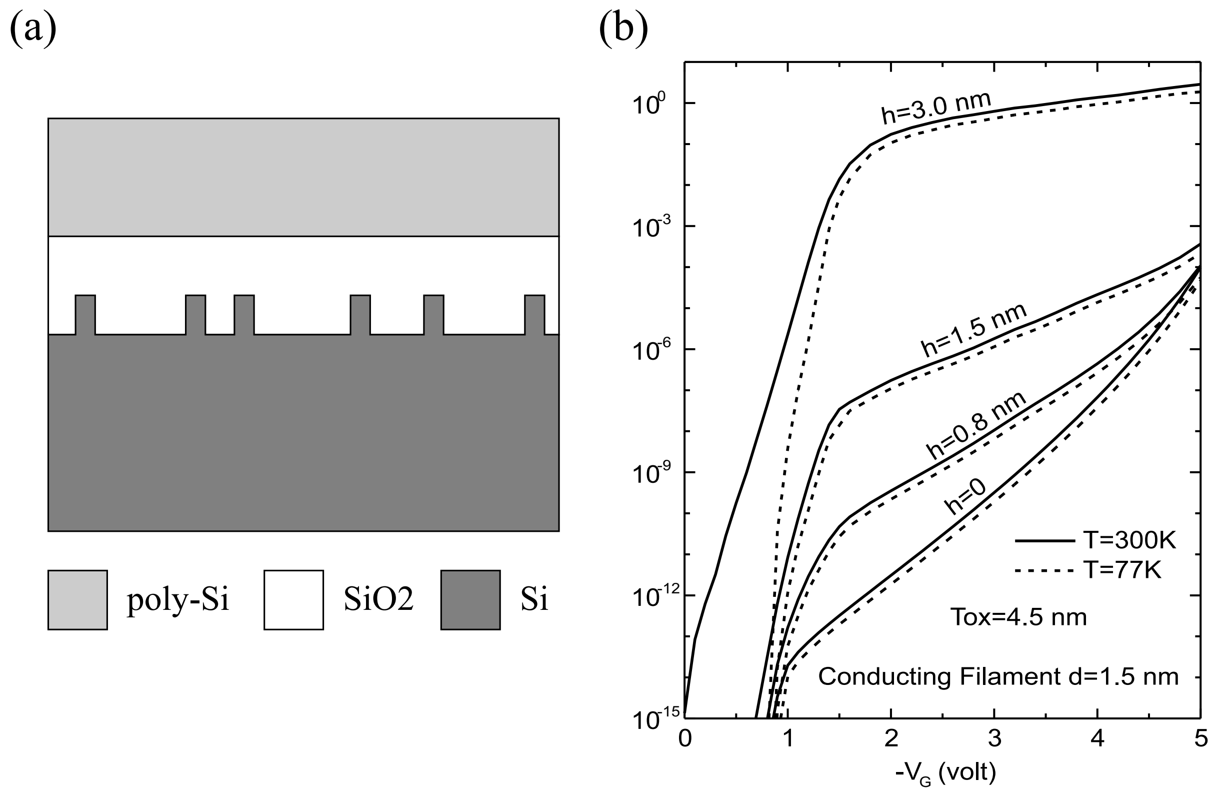

Figure 3. (*a*) Modelled MOS structure with Si filaments embedded within the oxide. (*b*) Calculated current density–voltage curves for a set of n$^+$ poly-Si/SiO$_2$/p-Si tunnel structures with oxide-embedded cylindrical conducting filaments with various cylinder heights. The oxide thickness is 4.5 nm. Conducting filaments have a diameter of 1.5 nm, and cover approximately 10% of the cross-sectional area.

MOS tunnel structures with ultrathin oxide barriers. One possible type of non-uniformity results when conducting filamentary paths are created in an oxide layer. Several researchers have postulated the stress-induced formation of localized conducting filaments extending from the Si–SiO$_2$ interface into the oxide as a model for breakdown or quasi-breakdown [5, 9, 10]. Here, we use a 3D model which allows calculation of the J–V characteristics of MOS tunnel structures containing such non-uniform oxide layers.

3.2. Method

A standard treatment of oxide tunnelling uses a 1D potential to describe the oxide barrier. In order to treat interfacial non-uniformity, a 3D description is necessary. In principle, variations in the non-uniform potential extend indefinitely in the directions along the interface. In practice, we do not perform computation on an infinite domain, but use instead a quasi-3D supercell geometry, in which a finite 3D cell is replicated infinitely in the two dimensions parallel to the layer interfaces, to approximate the physical structure. We treat the problem of tunnelling through this system using the open boundary planar supercell stack method [11].

Our model of the MOS tunnel structure consists of an n$^+$ poly-Si electrode, followed by the non-uniform oxide layer, and finally a p-type silicon region (see figure 3(*a*)). Because the nature of the filamentary conducting material is not well known, we choose to fill the cylinders with silicon for simplicity. In order to obtain J–V curves, transmission coefficients are calculated for a range of energies at each bias voltage and integrated to obtain a current density. The values of the parameters used and the details of the calculations are presented in [12].

3.3. Results and discussion

We consider a set of structures with 4.5 nm thick oxides, embedded with cylindrical conducting filaments 1.5 nm in diameter. The filaments account for approximately 10% of our computational domain in cross-sectional area, and extend from the SiO$_2$–Si interface into the oxide layer with cylinder heights of $h = 0.8$, 1.5 and 3.0 nm. A fourth, 'undamaged' ($h = 0$) structure is also included for comparison.

Figure 3(*b*) shows the J–V curves for these structures calculated at 300 K and 77 K. In general, the current densities increase dramatically with the filament length, h. This is due to lateral localization of transmitting state wavefunctions in the more highly conductive filaments. In order to estimate quantitatively the fraction of current flowing through the filaments, we define the 'filament transmission fraction' for a transmitting state as the sum of probability densities over the filament sites, divided by the total probability densities in the layers which contain the filaments.

Filament transmission fractions for tunnelling states with incoming energy equal to E_F^M at forward gate biases

of 2 V (direct tunnelling) and 5 V (Fowler–Nordheim tunnelling) were calculated in the case of each cylinder height. In all cases, the filament transmission fraction was found to exceed greatly 10%, the fraction of cross-sectional area occupied by the filaments. This clearly indicates that conduction is strongly localized to the filaments. In the direct tunnelling regime, the filament transmission fraction was found to be roughly 80–90% for all cylinder heights. The localization was found to be weaker in the Fowler–Nordheim regime, ranging from 26% for $h = 0.8$ nm to 46% for $h = 1.5$ nm to 87% for $h = 3.0$ nm. This is because the rough edge of the oxide is biased below the incoming electron energy in the Fowler–Nordheim regime, so the transmitted electron wavefunction is evanescent only through part of the filament. Therefore, the electron only tunnels through some fraction of the oxide layer adjacent to the gate. Since tunnelling properties in this regime are primarily determined by this leading edge of the oxide barrier, the $h = 0.8$ and 1.5 nm structures show current densities which converge with that of the undamaged ($h = 0$) structure as high bias. The filament in the $h = 3.0$ nm structure, however, extends sufficiently close to the leading edge of the tunnel barrier so that the large current density increases persist even at higher biases.

Our J–V curves of increasing filament heights bear a very strong qualitative resemblance to experimental I–V curves of MOS devices under increasing levels of stress [5, 6, 9]. It is worth noting that within our model we have reproduced levels of stress all the way from ‘unstressed’ to ‘breakdown’ using the same model, with the only difference being the height of the filaments. We note that in particular we can reproduce the breakdown behaviour without using filaments which completely permeate the oxide; we have kept the filament height to under 3 nm for the 4.5 nm oxide, as suggested by Hirose *et al* [9]. This may explain why the TSD device may operate in the high-current mode even after breakdown has been reached, as the oxide still is a partial contiguous barrier.

Another issue of note is the dependence on the fraction of gate area occupied by the filaments. We have performed a few calculations where we kept the filament size the same, but enlarged the supercell size by a factor of 4, effectively reducing filament density by a factor of 4. We find that the corresponding current density reduction is approximately fourfold in the direct tunnelling regime, but less in the Fowler–Nordheim regime. In fact, in the case of short filaments, the high bias current densities are essentially independent of filament density, since, again, high-bias currents are primarily controlled by the leading edge of the barrier, which is out of reach for the short filaments. These variations in scaling as a function of applied bias are consistent with the above discussion of filament transmission fraction.

The $h = 3.0$ nm curve differs from the others in its low-bias temperature dependence. In the $h = 0$, 0.8, and 1.5 nm cases, the 77 K and 300 K results appear essentially the same. In the $h = 3.0$ nm curve, however, current densities at low biases increase significantly with temperature. This is due to resonant tunnelling through quantum-confined states in the filaments. This behaviour is described in detail elsewhere [12]. It is therefore possible that temperature-dependent measurements of stressed-oxide I–V curves may provide further insight into the applicability of this filament model.

4. Conclusions

We have found that n^+ poly-Si/SiO_2/n-Si/p-Si TSD devices can exhibit two modes of operation depending on the level of stress to which they have been subjected. These modes seem to correspond to the SILC and breakdown phases found in MOS device stress experiments. Even though the oxide in the TSD devices has reached breakdown in the high-current mode of operation, the device can support bistable current states, suggesting that the oxide still acts as somewhat of a tunnel barrier. These results, as well as MOS stress results, can be understood in terms of a model in which increased stress creates larger and larger conducting filaments extending from the Si–SiO_2 interface. We performed 3D quantum mechanical calculations to analyse the current–voltage characteristics of n^+ poly-Si/SiO_2/p-Si tunnel structures containing such oxides with embedded filaments. The filaments are found to act as localized conduction paths, leading to dramatic increases in current densities. Depending on the filament length, this model can produce current–voltage characteristics reminiscent of those observed experimentally for ultrathin oxides subjected to wide ranges of stress.

Acknowledgments

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