Microfabrication of silicon–nitride micromesh bolometric detectors for planck high frequency instrument

Minhee Yun,[a] Jamie Bock, Warren Holmes, Tim Koch, Jerry Mulder, Richard P. Vasquez, and Larry Wild
Jet Propulsion Laboratory, California Institute of Technology, Pasadena, California 91109

Andrew Lange
Department of Physics, California Institute of Technology, Pasadena, California 91125

The high frequency instrument (HFI) on the National Aeronautics and Space Administration/European Space Agency Planck Surveyor, scheduled for launch in 2007, will map the entire sky in six frequency bands ranging from 100 to 857 GHz to probe cosmic microwave background anisotropy and polarization with angular resolution ranging from 9′ to 5′. The HFI focal plane will contain 48 silicon–nitride micromesh bolometers operating from a 100 mK heat sink. Four detectors in each of the six bands will detect unpolarized radiation. An additional four pairs of detectors will provide sensitivity to linear polarization of emissions at 143, 217, and 353 GHz. We have fabricated and developed sensitive Si_3N_4 micromesh spider-web bolometers for submillimeter observation using microelectromechanical system techniques. The spiderweb architecture in this research provides high infrared absorption with minimal heat capacity and volume. © *2004 American Vacuum Society.* [DOI: 10.1116/1.1642644]

I. INTRODUCTION

The Planck surveyor was selected in 1996 as the Medium Mission of the Horizon 2000 Plan of the European Space Agency. Planck is dedicated to obtaining definitive images of the cosmic microwave background (CMB) fluctuations and extracting, with high accuracy, the primordial signal from contaminating astrophysical sources of confusion. Planck will allow precise determination of the fundamental cosmological constants that define our universe, including the densities of baryonic, cold, and hot dark matter; the value of the cosmological and Hubble constants; and the neutrino content of the universe. Planck will use two focal plane units: a low-frequency instrument using high electron mobility transistors, sampling in the frequency range of 30–100 GHz, and a high frequency instrument (HFI) using bolometers,[1,2] sampling in the frequency range of 100–857 GHz. Planck will be launched in 2007 on an Ariane 5 launch vehicle into a halo orbit around the L2 libration point in the Sun–Earth system. The spacecraft will be spin stabilized with a spin rate of 1 rpm. The HFI is designed to measure the temperature anisotropy and polarization of CMB radiation over the frequency bands where contamination from foreground sources is at a minimum and the CMB signal is at a maximum. Emission from foreground contributions (from the Galaxy and from extragalactic sources) will be removed from sky maps by measuring the spectral signature of the fluctuations over a wide frequency range. To measure CMB over this range, the HFI has been designed as a multiband instrument with six bands from 100 to 857 GHz. The focal plane is a layout of 48 bolometric channels in 36 pixels, permitting fulfillment of all scientific requirements for the HFI.

The HFI consists of: (i) the HFI focal plane unit, (ii) the junction field effect transistor (JFET) box, (iii) the readout electronics, (iv) the data processing unit, (v) the coolers, and (vi) the harness and tubes linking various subsystems. The HFI is based on bolometers cooled to 100 mK. Bolometers are sensitive to the heat deposited in an absorber by incident radiation. They require very low temperatures to obtain a low heat capacity, giving high sensitivity with a short thermal time constant. Cooling the detectors at 100 mK in space is a major requirement that drives the architecture of the HFI. Starting from the passively cooled 50/60 K stage of the payload module, this cooling is achieved by a four-stage cooling system (18–4–1.6–0.1 K). This cooling system also provides an electromagnetic shield (a Faraday cage) for the high-impedance part of the readout electronics. The ac bias and readout electronics perform all the electrical functions of the cold stages, including temperature measurement and control.

In this research, we have fabricated and developed detectors using microelectromechanical system (MEMS) techniques for HFI models. The use of MEMS techniques in this research has improved the fabrication process required for developing spider-web bolometer detectors. In order to produce detectors suitable for flight use, the fabrication process must give a high mechanical yield. The etch technique used in this process is challenging in part because our large $(300 \times 100 \times 25 \ \mu m)$ neutron-transmutation-doped (NTD) Ge thermistor and associated In bump bonds must not be damaged during the process. NTD Ge was chosen for this application because of its extreme noise stability.[3] The thermal conductance G determines the responsivity and sensitivity of a bolometer. Therefore the fabrication process must result in uniform thermal conductivity to give uniform detector performance. Finally, the process must not result in excess heat capacity, particularly over the extended-area absorber, be-
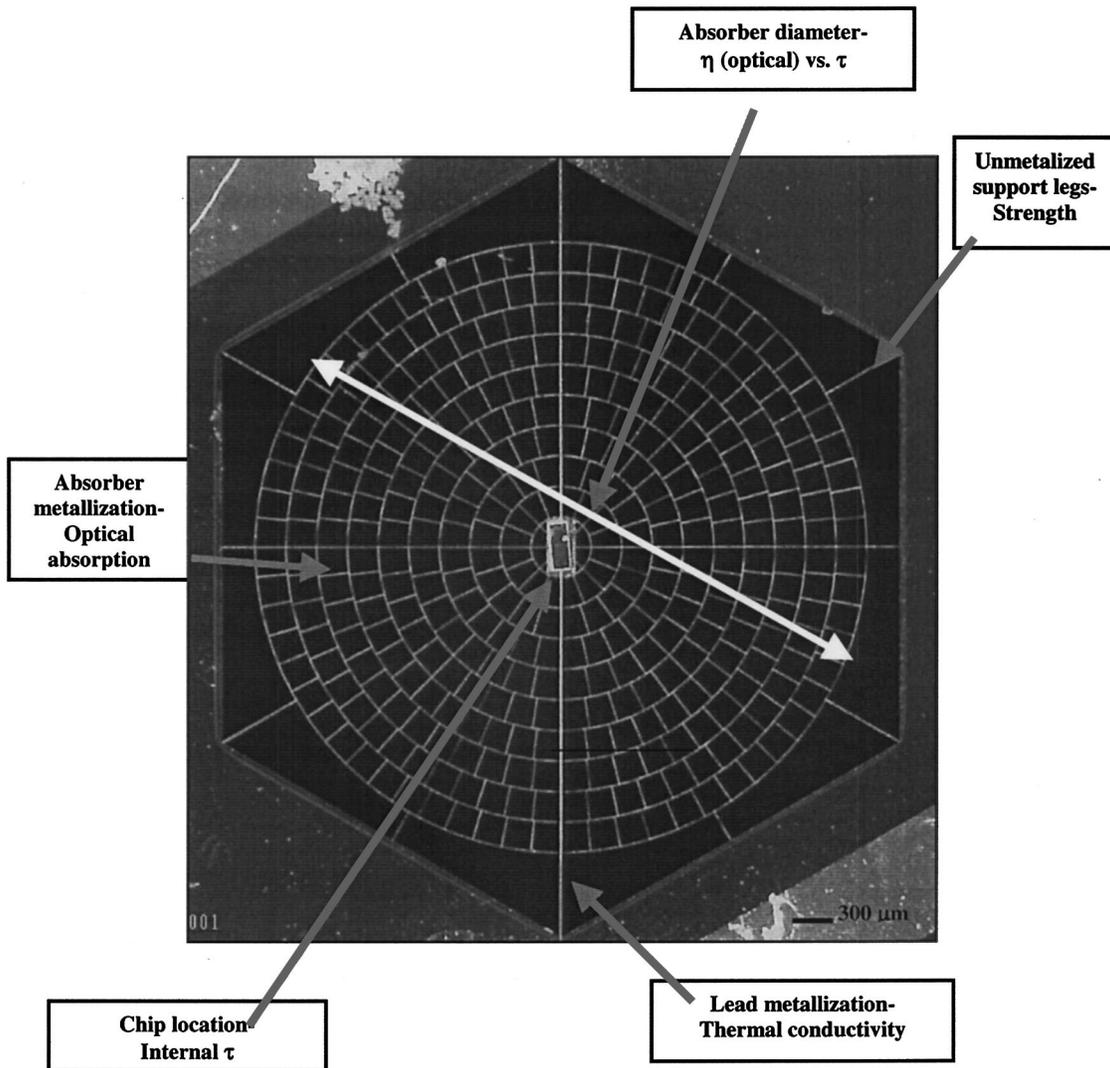
FIG. 1. Spiderweb architecture with NTD Ge thermometer. Absorber metal thickness and diameter affect optical efficiency and internal time constant, chip location affects internal time constant, lead thickness affects thermal conductivity, and support legs increase device strength.

cause the speed of response of the detectors will be degraded thereby.

II. DETECTOR FABRICATION

The silicon–nitride micromesh spiderweb bolometer (SWB) technology developed for Planck will provide background-limited performance in all bands. Planck will map the entire sky in six frequency bands ranging from 100 to 857 GHz to probe CMB anisotropy and polarization with angular resolution ranging from $9'$ to $5'$. The radiation is efficiently absorbed in a conducting film deposited on a micromesh absorber. This absorber is thermally isolated by radial legs of uncoated silicon nitride that provide rigid mechanical support with excellent thermal isolation, as shown in Fig. 1.

The use of MEMS techniques in this research has improved the fabrication process required for developing large-format bolometer arrays. In order to be suitable for large-format arrays, the fabrication process must give a high mechanical yield. The process sequence of the fabrication of silicon on insulator (SOI) micromesh spiderweb bolometers is shown in Fig. 2. In this research, we used HF–HNO_3–de-ionized (DI) water (HND) wet etching and deep-trench reactive-ion etch (DRIE) technologies to fabricate the micromesh spiderweb bolometer. HND etching technology[4] is a very common wet process widely used for removing damaged layer materials and cleaning the surface of materials. In addition to HND etching, silicon wafers are typically wet etched in mixtures of nitric acid and hydrofluoric acid. The most common dry-etching technique is reactive-ion etching (RIE). With RIE, ions are accelerated toward the material to be etched and the etching reaction occurs in the direction of ion travel. Deep trench RIE is a technique used extensively in the semiconductor field. Compared to wet etching, deep-trench etching has many advantages such as etch uniformity and etch profile. The difficulties in performing a successful deep-trench etch process are compounded by the range of requirements for various MEMS applications:
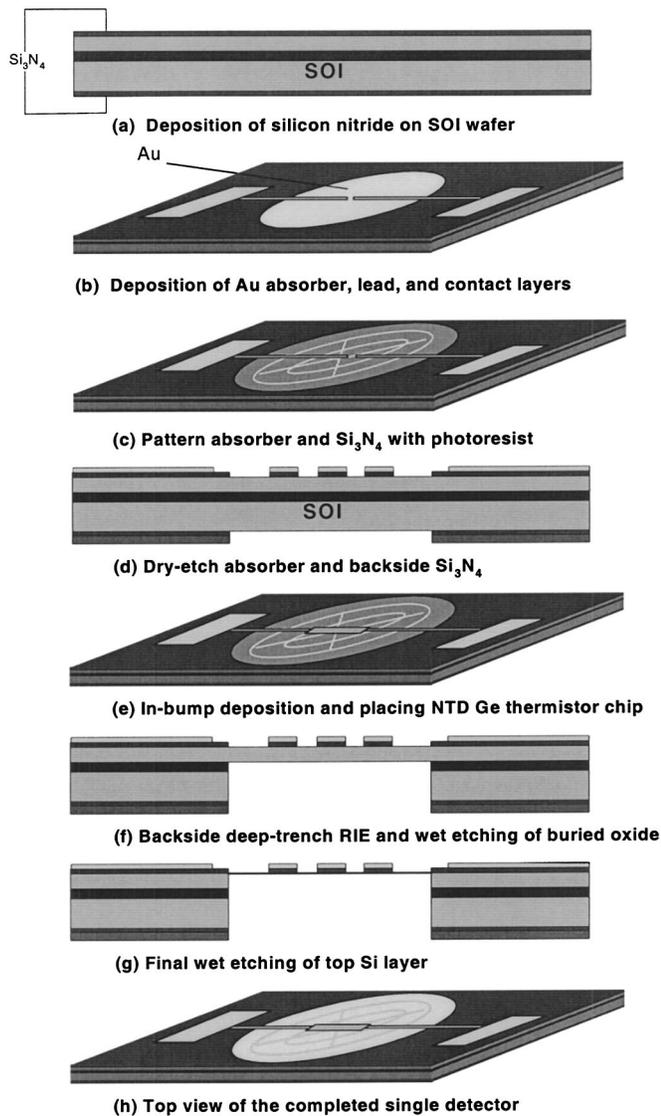
Si₃N₄

(a)   Deposition of silicon nitride on SOI wafer

Au

(b)   Deposition of Au absorber, lead, and contact layers

(c)   Pattern absorber and Si₃N₄ with photoresist

SOI

(d)   Dry-etch absorber and backside Si₃N₄

(e)   In-bump deposition and placing NTD Ge thermistor chip

(f)   Backside deep-trench RIE and wet etching of buried oxide

(g)   Final wet etching of top Si layer

(h)   Top view of the completed single detector

FIG. 2. Process flow diagram.

sorber heat capacity, and cosmic-ray cross section. Micromesh bolometers are currently used in numerous CMB experiments (BOOMERANG,[6] MAXIMA,[7] SuZIE,[8] and Archeops[9]) that operate under optical-loading and detector-sensitivity requirements similar to those needed here. Each polarization-sensitive detector uses a pair of bolometers. These polarization-sensitive bolometers (PSBs) use fabrication processes identical to those of the SWB but have an absorber geometry that makes the PSBs sensitive only to one linear polarization.[10]

The processes of cleaning, dry etching, low-pressure chemical vapor deposition (LPCVD), lithography, and metallization are standard semiconductor-fabrication techniques. The wafers used in this research were thermally bonded SOI wafers with (100) orientation. The thicknesses of the top Si, buried SiO_2, and bottom Si layer were 2, 1, and 350 μm, respectively, with $\pm$10% variation. First, the SOI wafers were prepared with standard RCA cleaning. Then, a 1 μm layer of Si_3N_4 [Fig. 2(a)], which forms support legs, was deposited on the wafer using LPCVD. Several Au depositions using photolithography processes form the absorber for optimal infrared absorption, the electrical leads that define the thermal conductance, and the wiring layer for electrical readout. Using a liftoff technique Ti–Au metal films are deposited to form the absorber layer [Fig. 2(b)]. The thickness of the Au layer, ranging from 90 to 300 Å, deposited on the absorber is chosen to give optimal infrared absorption. The thickness of the Au layer forming the electrical leads on the supports may be varied to tailor the thermal conductance. The wafer is then patterned to define the mask for the membrane [Fig. 2(c)], and etched, first with an Ar reactive-ion etch to form spider-web absorber Ti–Au layer, and then by a CF_4 and O_2 reactive-ion etch to remove the silicon nitride. The backside is similarly patterned, aligned to the front side with an infrared camera, and reactive-ion etched to remove the backside silicon nitride to define the silicon frame [Fig. 2(d)]. An Ni–In bump sized 15 μm$\times$40 μm [Fig. 2(e)] is deposited on each of the two contact pads located at the center of the device, using liftoff lithography to deposit 40 nm Ni+3 μm In. The nickel layer is used as an intermediate layer to prevent reaction of the indium with the gold during processing. Before the thermistors are attached, the back side is patterned with photoresist and hard baked at 130 °C for 5 min.

The thermistors are manufactured from a polished slab of NTD Ge material by p doping with a 4.53×10^{16} cc concentration of Ga and a 1.29×10^{16} cc concentration of As to have a resistance of 5 MΩ at 100 mK. Using photolithography, two contacts are defined on a single face of the chip. The contacts are B implanted and deposited with 2 nm Ti+20 nm Au. Two 15 μm$\times$15 μm In bump bonds are then patterned on each contact of the thermistor with the same Ni–In process used on the wafer. The chips are diced with a diamond saw and etched in a mixture of HF and HNO_3 to remove saw damage. The resulting chips are ~300 μm long, ~50 μm wide, and 25 μm thick, with two contacts 100 μm wide and 50 μm long, separated by 200 μm. The NTD Ge thermistor

an etch depth from 20 to over 300 μm; an aspect ratio of greater than 30; and a silicon exposed area of below 5% to over 80%.[5] The deep-trench RIE allows us to remove the bulk silicon without exposing the sensitive layer on the front side of the detector (e.g., In, Ge, Ti) to reactive etchants. The buried oxide layer also prevents fluorine-based etch products from contacting any portion of the active area of the detector. Because we found that the deep trench RIE process left significant residues with large excess heat capacity when the active area of the bolometer was directly exposed to the etch, we selected the HND liquid etch as the second step of the etch process. The liquid-etch step produces devices with low heat capacity, but unfortunately also results in lower device yield. The temperature of the absorber is measured by a small (25$\times$100$\times$300 μm) NTD Ge thermistor that is indium bump bonded with thin film leads that are photolithographed on two of the radial legs. Compared to a solid absorber, the micromesh has a geometric filling factor of up to 11%. This factor provides a correspondingly small suspended mass, ab-

was located [Fig. 2(e)] over the contacts at the center of the absorber and attached by the In bumps with 1–2 N of force by a micrometer. Finally, the silicon was removed using a deep-trench reactive-ion etch to the insulating layer [Fig. 2(f)], followed by liquid etches to remove the thin oxide and silicon layers [Fig. 2(g)].

We have used an inductive-coupling plasma (ICP) system for deep-trench etching because ICP appears to be the most suitable system for this application. This system allows high etch rates and anisotropic etching with selectivity to conventional photoresist masks.[11] The DRIE is manufactured at Surface Technology Systems and is a single-wafer, load-locked system that employs inductively coupled plasma etching with the advanced silicon etch process.[11] The plasma is generated by an inductively coupled coil at 13.56 MHz with a maximum power output of 1000 W. Another 13.56 MHz generator was used to apply the power to the electrode. This technique allows independent control of the bias potential of the wafer with a power of up to 300 W. Using a temperature controller connected to a LN_2 supplier, the wafer temperature is maintained at less than 80 °C. The system and reaction pressure is controlled by an automatic pressure controller. Typical base pressures are 1×10^{-7} Torr, and operating pressures are from 1 to above 10 mTorr. During processing, the wafer electrode is lifted using a large bellows from loading height to a processing height within 10 mm of the bottom coil. This reduces ion-density loss by diffusion. The electrostatic chuck and platen assembly are cooled by a DI water chiller system. Wafer cooling is provided by mass-flow-controlled LN_2 on the back side of the wafer. Ion densities on the order of 10^{12} cm^{-3} are obtained at the center of the chamber. We have used SF_6 and C_4F_8 as the etch and passivation gases, respectively. During the etch step, SF_6 is used to etch Si isotropically. This is followed by a short passivation step[11] using C_4F_8. In general, to etch through the bottom (350 μm) silicon layer takes about 160 min. The selectivity to etching relative to silicon is 150:1 for the oxide and 75:1 for the photoresist. When the silicon has cleared, the etch process is stopped. After the final etch, the standby step is repeated and the load-lock handler removes the wafer from the reaction chamber.

After the DRIE process, 1 μm of SiO_2 and 2 μm of Si remain under the silicon–nitride absorber. The SiO_2 layer is removed with a standard 10:1 buffered oxide etch to expose 2 μm of the top Si layer. The bolometer elements are then released from the DRIE mounting wafer by dissolving the mounting wax via a combination of solvents. During this process, each bolometer is separated from all the other corresponding neighbors on the wafer. A thorough cleaning of each bolometer follows this dismounting process; then each device is recoated with an acid-resistant wax on top of the absorbing elements to complete the final wet-etch process. A mixture of hydrofluoric acid, nitride acid, and DI water is used to remove the final 2 μm of the top Si layer while the wax protects the metalization, nitride web structure, and Ge thermistor. After the Si is etched, the device is rinsed thoroughly. To complete the formation of the bolometer, the
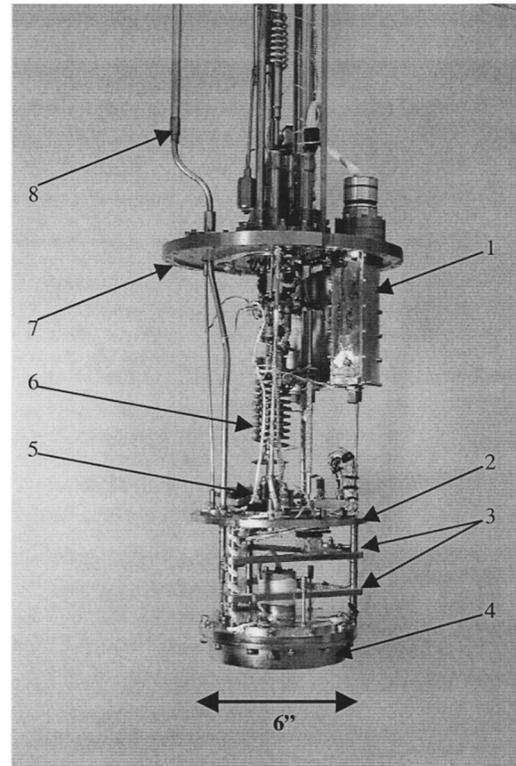

FIG. 3. 100 mK test bed: (1) JFET box; (2) 100 mK cold plate; (3) passive thermal filter stages; (4) evacuated sample can; (5) ^{3}He/^{4}He mixing chamber; (6) heat exchanger; (7) indium vacuum to LHe seal; and (8) light pipe.

acid-resistant wax is removed via a combination of solvents used to dissolve the wax and clean the surface.

Figure 2(h) shows the final single spider-web array after releasing and cleaning. Each bolometer Si_3N_4 support leg is 5 μm wide and 1 μm thick. The web legs are 4 μm wide and 1 μm thick, leading to a filling factor of approximately 3%–11%, dependent on the frequency ranges of the bolometers. This small filling factor over such a large area allows highly energized particles to pass undetected while still capturing the wavelength of radiation being observed. The absorber has a relatively small mass and is suspended by support legs of silicon–nitride that provide robust mechanical support and very low thermal conductivity. Therefore the fabricated bolometer device is mechanically insensitive to the relatively low frequency vibration encountered during launch and operation.

III. CHARACTERIZATION

A. Thermal environment

Because the HFI bolometers operate at 100 mK, an Oxford Instruments Kelvinox-25–^{3}He/^{4}He dilution refrigerator has been instrumented to perform the necessary low-temperature characterization of the detectors, as shown in Fig. 3. The test facility is capable of testing up to 21 bolometers per run. All channels have demonstrated intrinsic electronic noise <6 nV/$\sqrt{\text{Hz}}$ over the frequency range 0.010–25 Hz. Individual bolometers delivered for use in the flight pro-

TABLE I. Required bolometer performance.

Frequency (GHz)	g (μm)[a]	2a (μm)[b]	d (μm)[c]	ff (%)[d]	C (pJ/K)[e]	G (pW/K)[f]	NEP (e-17W/rtHz)[g]
100	320	4.8	4500	3	1.92	120	1.27
143	225	3.4	3160	3	1.81	160	1.37
217	160	2.4	2280	3	1.91	215	1.65
353	160	2.4	2280	3	2.15	215	2.08
545	110	6.4	2200	1.16	2.85	250	5.21
857	70	4	2100	11.4	18.0	1590	14.3

[a]Grid spacing (g).
[b]Linewidth in absorber (2a).
[c]Absorber diameter of active area (d).
[d]Absorber filling factor (ff).
[e]Required heat capacitance (C).
[f]Target thermal conductivity (G).
[g]Required noise equivalent power (NEP).

gram have been measured to have <12 nV/$\sqrt{\text{Hz}}$ intrinsic noise under biased conditions in the absence of illumination. The thermal stability required for bolometer intrinsic-noise determination is 40 nK/$\sqrt{\text{Hz}}$ from 0.016 to 25 Hz. This stability is implemented via passive-thermal design and active feedback using high-resolution thermometry. A four-stage structure provides passive-thermal filtering. Active control of a stage distributes the thermal-noise power density over a wider bandwidth, and modulation of the isolated stage where the detectors are mounted is reduced.

B. Optical excitation: speed of response measurement

A bolometer's heat capacity ($C \sim 1$ pJ/K) and the thermal conductance ($G \sim 100$ pW/K) of the link to the 100 mK thermal reservoir determines the speed of response. This bolometric response is modified from simple $\tau = C/G$ (~ 10 ms) by the weak electrothermal feedback of the thermistor, but essentially behaves as a single-pole rolloff. In order to measure the response to variable-frequency, constant-amplitude input radiation, a light pipe transports radiation from a source outside the Dewar at 300 K to bolometers at 100 mK via a thin-walled stainless-steel tube, gold plated on the upper section. This technique demonstrates the optical response of bolometers under conditions similar to those expected in flight.

C. Thermal cycling

A LN$_2$ cryogen Dewar has been modified with a sample holder that can hold two ''slices'' of eight bolometers, a variable-flow heat exchanger, and heaters. Automated operation allows unattended thermal cycling between 330 and 80 K. The resistance of each bolometer is recorded throughout the cycling intervals to a precision of $\pm 1\%$.

D. Qualification

Qualification testing is performed on devices that have completed flight-acceptance testing, after which they are not flight deliverables. Twelve detectors, six SWB (six bolometers), and six PSB (12 bolometers), are taken as a represen-

tative sampling. Acceptance performance tests are repeated on all devices and the test results are evaluated for a qualification report. The simple construction of the detectors allows us to qualify the entire assembly as a hybrid. The number of cryogenic thermal cycles for qualification, 80, was chosen based on the estimates from our various collaborators. These estimates indicate that the total number of cycles to cryogenic temperatures likely to be experienced by the flight devices is ~ 25. The choice of cycling to a low temperature of ~ 90 K (LN$_2$), rather than to the operating temperature of 100 mK or to 4.2 K (LHe), is based upon experience with similar devices, which indicates that most failures occur during transition within this temperature range, and on general experience within the low temperature community that the majority of damage due to differential thermal contraction occurs within this temperature range.

IV. DEVICE PERFOMANCE

We have fabricated freestanding Si$_3$N$_4$ micromesh with a wide variety of geometries depending on the various frequencies, as shown Table I. These criterias in Table I are chosen from previous fabrications.[3] The required heat capacities, C, are chosen to give sufficient speed of response such that the sensitivity to point sources is not significantly degraded at the Planck telescope scan rate. The target thermal conductivities are selected based on noise and time constant requirements. The absorber diameter is chosen to be 1.5*lambda and the grid spacing is lambda/5 to achieve sufficient optical efficiency.[12] The study of heat capacities for 545 and 857 GHz are ongoing. Because of the relatively large surface areas of the devices and the stringent requirements on the heat capacity, small amounts of residue that are left on the device after processing can easily degrade the device performance. These residues can take the form of unetched Si remnants on the absorber web or, more difficult to see, residue from the various waxes and ion- and wet-etching processes used in fabrication of the devices. Measured heat capacity as a function of absorber area is shown in Fig. 4(a). The heat capacities have been between 0.96 and 1.92 pJ/K for 100 GHz bolometers, between 0.24 and 3.03
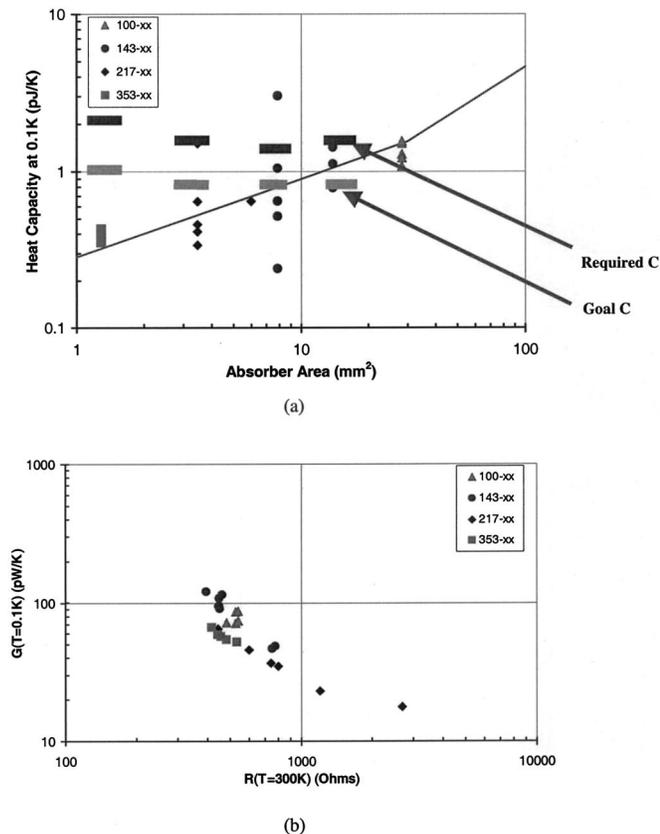
FIG. 4. (a) Measured heat capacities showing required (dark boxes, 1.92 for 100 GHz, 1.81 for 143 GHz, 1.91 for 217 GHz, 2.15 for 353 GHz), goal (gray boxes. 0.96 for 100 GHz, 0.91 for 143 GHz, 0.96 for 217 GHz, 1.08 for 353 GHz), achieved and (b) measured thermal conductivity dependent on lead impedance.

ductivity required for absorption and dominates over the silicon nitride at lower than 300 mK temperature.[14] This correlation allows for early screening between the room-temperature resistance of the electrical leads and their thermal conductivity at ~100 mK. This relationship allows for early screening of the detectors based on a simple room temperature measurement. In addition, the data show that the contribution to the thermal conductivity from the Si_3N_4 legs is negligible in comparison with the design values of the thermal conductivities, which are >100 pW/K. All other measurements, for example of time constant and noise equivalent power, are ongoing.

V. SUMMARY

We have developed and fabricated for the Planck mission Si_3N_4 micromesh bolometers using MEMS to obtain definitive images of the CMB fluctuations and to extract the primordial signal to high accuracy from contaminating astrophysical sources of confusion. The process that we have developed reliably produces detectors that meet all of the requirements for Planck. We are close to completing the testing of the cryogenic qualification model detectors, and are scheduled to complete fabrication of the proto-flight model detectors and to complete testing and delivery of these detectors in 2003. Using our fabrication techniques Planck can achieve high-resolution, high sensitivity ($dT/T < 3 \times 10^{-6}$ in each 7 arcmin pixel), wide frequency coverage, and excellent control of systematic errors. This combination of requirements cannot be met either by ground-based or balloon-borne observatories and demands a space mission such as Planck.

ACKNOWLEDGMENTS

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pJ/k for 143 GHz, between 0.30 and 1.90 pJ/k for 217 GHz, and between 0.23 and 2.15 pJ/K for 353 GHz. The results to date indicate that there is an anomalous component of heat capacity that is scaling with the detector area, but that this component is at an acceptably low level to yield a high fraction of detectors that meet the flight requirements. Since these results were obtained, we have made improvements in details of the process, resulting in less visible residue on the detectors.

The preliminary results of thermal-conductance properties dependent on lead impedances at room temperature are given in Fig. 4(b). Thermal conductivity across the absorber could result in a loss in optical responsivity. The conductivity between absorber and heat sink is more than 1 order of magnitude smaller than the thermal conductivity of the nylon supports used in other low-background composite bolometers at 300 mK, which allows Si_3N_4 micromesh bolometers to achieve higher sensitivity under low-background conditions.[13] The internal thermal conductivity of the absorber corresponds to the conductivity of a single leg in the central active area and has contributions from both the metal film and the silicon nitride. The thermal conductivity of the metal is related by the Wiedemann–Franz law to the electrical con-