A Three-Switch High-Voltage Converter

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***Abstract*— A novel single active switch two-diodes high-voltage converter is presented. This converter can operate into a capacitor-diode voltage multiplier, which offers simpler structure and control, higher efficiency, reduced electromagnetic interference (EMI), and size and weight savings compared with traditional switched-mode regulated voltage multipliers. Two significant advantages are the continuous input current and easy isolation extension. The new converter is experimentally verified. Both the steady-state and dynamic theoretical models are correlated well with the experimental data.**

***Index Terms*—DC–DC power conversion, voltage multipliers.**

I. Introduction

In high-voltage/low-current applications, such as TV-CRT's, lasers, X-ray systems, ion pumps, electrostatic systems, etc., a capacitor-diode voltage multiplier is usually preferable to a transformer with a large turns ratio and diodes with enormous breakdown voltages. A transformer with a large turns ratio is undesirable because it exacerbates the transformer nonidealities: the leakage inductance and the winding capacitance. These nonidealities cause voltage and current spikes and increase loss and noise.

A common pulsewidth modulation (PWM)-controlled voltage multiplier [4] is shown in Fig. 1, where a buck converter is followed by a push–pull voltage multiplier. The main disadvantages of this converter are: 1) the circuit requires two stages including three switches and a complex control system, which increase loss and cost; 2) the input current is discontinuous, thus, input filter is invariably required to smooth out the switching ripple; and 3) high power factor is hard to realize with the buck preregulator.

In this paper, we propose a novel single-stage high-voltage converter, which can be used to drive voltage multipliers. It eliminates the above drawbacks, reduces the size and cost, and increases the efficiency and reliability.

The basic operation of the new converter is explained in Section II. Dynamic analysis and transfer functions are given in Section III. In Section IV, extensions for the basic three-switch version are discussed. A soft-switching mechanism is explained in Section V. The experimental results are presented in Section VI, and the conclusion is given in Section VII.

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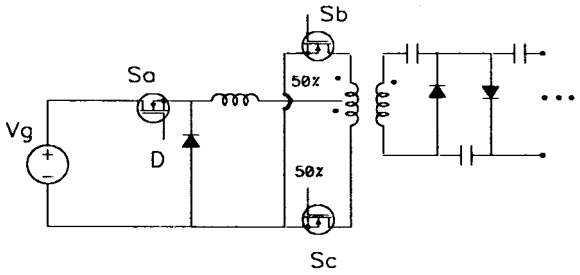


Fig. 1. A common PWM-controlled voltage multiplier.

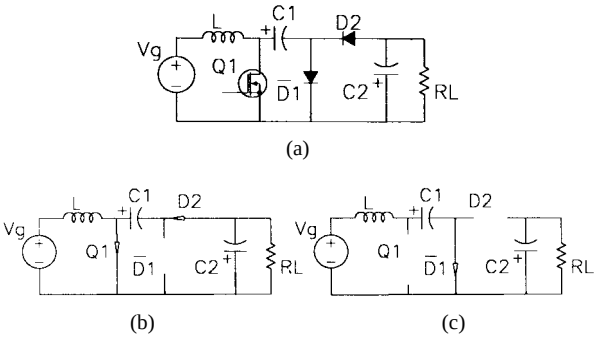


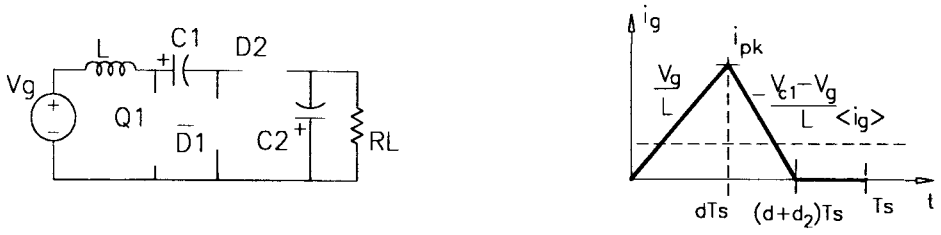
Fig. 2. The new three-switch HV converter: (a) the basic version, (b) the equivalent circuit during DT_s, and (c) the equivalent circuit during $D''T_s$.

II. Basic Operation of the New Converter

A. Continuous Inductor Current Mode (CICM)

The basic version of the HV converter is shown in Fig. 2(a). It appears like the Cuk converter, except that the output inductor of the Cuk converter is replaced by a diode. The cost for doing so is the loss of continuous output current, but in applications which require very high output voltage and small output current, the new converter gives substantial savings in size and weight.

The basic operation for the converter is as follows. At the beginning of each switching cycle, Q_1 is turned on, the equivalent circuit is shown in Fig. 2(b). Since the voltage across C_1 is larger than that of C_2, D_2 is turned on simultaneously and D_1 is turned off by the negative output voltage across it. C_1 is charging the output capacitor C_2 and the load resistor R_L (note that the peak of the charging current is limited by parasitic resistance in series with C_1 and C_2). At the end of DT_s period, Q_1 is turned off, the circuit is equivalent to that of Fig. 2(c). The input inductor current forces D_1 to turn on. Then, D_2 is turned off by the negative output voltage. In this period, C_1 is being charged up by the inductor current while C_2 is being discharged to supply the load current. If the parasitics are neglected, the voltage conversion ratio M can



(a) (b)

Fig. 3. The three-switch converter operates in DICM: (a) the third interval $i_L = 0$ and (b) the input inductor current waveform.

be easily derived as

$$M = \frac{V}{V_g} = -\frac{1}{D'}. \tag{1}$$

The new converter can also be developed from the boost converter by exchanging the position of the diode and the capacitor in the boost converter and adding another diode and an output capacitor. As a result, the new converter shares many similar properties with the boost converter. However, unlike the boost converter, the new converter can be easily extended to provide dc isolation and drive a capacitor-diode voltage multiplier. These features will be discussed later in Section IV.

B. Discontinuous Inductor Current Mode (DICM) and Automatic Current Shaping

If the input inductor current is discharged to zero before the end of the switching cycle, the converter is operating in discontinuous inductor current mode (DICM). The equivalent circuit in this interval is illustrated in Fig. 3(a) and the current waveform in Fig. 3(b). The steady-state analysis is the same as that of the boost converter [1].

The conversion ratio at DICM is

$$M = \frac{1 + \sqrt{1 + \dfrac{4D^2}{K}}}{2} \tag{2}$$

where the conduction parameter K is defined as

$$K = \frac{2L}{RT_s}. \tag{3}$$

The converter operates in CICM when

$$K > DD'^2 \tag{4}$$

and in DICM when

$$K < DD'^2. \tag{5}$$

For off-line applications, the new converter can work as an "automatic" current shaper when operating in DICM.

The input inductor current averaged over one switch period is given by

$$\begin{aligned} \bar{i}_g(\theta) &= \frac{|V_g(\theta)|}{2L}\, dT_s[d + d_2(\theta)] \\ &= \frac{|V_g(\theta)|}{2L} \times d^2 T_s \left[1 + \frac{|V_g(\theta)|}{V_{c1} - |V_g(\theta)|}\right] \\ &= \frac{|V_g(\theta)|}{R_{em}} \left[\frac{M}{M - |\sin(\theta)|}\right] \end{aligned} \tag{6}$$

where

$$V_g(\theta) = V_g \sin(\theta) \tag{7}$$

$$M = \frac{V_{c1}}{V_g} \tag{8}$$

$$R_{em} = \frac{2L}{T_s d^2} \tag{9}$$

is the emulated resistance of the shaper.

By keeping the duty ratio and switching frequency constant, the power factor is theoretically greater than 0.97 for conversion ratio $M > 1.5$, which is the same as the boost "automatic" current shaper [5].

C. The Peak Capacitor Charging Current

As in Fig. 2(b), C_1 is charging C_2 directly through switches Q_1 and D_2. The peak charging current through C_1 can be approximately expressed as

$$I_{C1\text{peak}} = \frac{I_o\left(T_s - DT_s \dfrac{C_1}{C_1 + C_2}\right) e^{-(t/\tau_C)}}{\tau_C(1 - e^{-(DT_s/\tau_C)})} + I_o \frac{C_1}{C_1 + C_2} \tag{10}$$

where

$$\tau_C = (C_1 || C_2)(r_{C1} + r_{C2}) \tag{11}$$

r_{c1} and r_{c2} are the ESR associated with C_1 and C_2, respectively. The peak current through Q_1 equals the sum of $I_{C1\text{peak}}$ and the inductor current. Increasing the capacitance reduces the peak current and power loss. Increasing ESR values also reduces the peak current, but will increase the power loss. Another way to reduce the peak current and di/dt is to insert a small inductor (e.g., [9]) or saturable reactor in series with the capacitor C_1.

III. Small-Signal Dynamics

The method of state-space averaging [1] or averaged switch model [2] can be used to determine the dynamic responses for the three-switch converter [Fig. 2(a)]. The state-space averaging technique is justified by the assumption of the linear capacitor voltage ripple, which requires the time constant of capacitor charging loop to be sufficiently longer than the switching period, i.e., $\tau_c = (C_1 || C_2)(r_{c1} + r_{c2}) \gg DT_s$.

The control-to-output-voltage transfer function is found as

$$\frac{\hat{V}}{\hat{V}_d} = \frac{V}{D'} \frac{\left(1+\frac{S}{w_{z1}}\right)\left(1-\frac{1}{Q_{zo}}\frac{S}{w_{zo}}+\frac{^2}{w_{zo}^2}\right)}{\left(1+\frac{S}{w_{p1}}\right)\left(1+\frac{1}{Q_{po}}\frac{S}{w_{po}}+\frac{S^2}{w_{po}^2}\right)} \tag{12}$$

where

$$L_e = \frac{L}{(D')^2} \tag{13}$$

$$w_{zo} = \frac{1}{\sqrt{L_e C_1}} \sqrt{\frac{D^2 R}{D'(r_{c1}+r_{c2})}} \tag{14}$$

$$Q_{zo} = \frac{1}{\sqrt{L_e/C_1}} \sqrt{\frac{D'R(r_{c1}+r_{c2})}{D^2}} \tag{15}$$

$$w_{z1} = \frac{1}{C_2 r_{c2}} \tag{16}$$

$$w_{po} = \frac{1}{\sqrt{L_e(C_1+C_2)}} \tag{17}$$

$$Q_{po} = \frac{R}{\sqrt{\frac{L_e}{(C_1+C_2)}}} \frac{1}{1+\frac{R}{L_e/C_2}\left(\frac{r_{c1}}{DD'}+\frac{r_{c1}C_1}{D'C_2}+\frac{r_{c2}}{D}\right)} \tag{18}$$

$$w_{p1} = \frac{D}{(C_1 \| C_2)(r_{c1}+r_{c2})}. \tag{19}$$

The double right-half plane (RHP) zero w_{zo} is separated into two real zeros when $Q_{zo} \ll 1$ and the two zeros are

$$w_1 = \frac{R}{L_e} \tag{20}$$

$$w_2 = \frac{D^2}{D'} \frac{1}{C_1(r_{c1}+r_{c2})}. \tag{21}$$

Note that w_1 is exactly the same RHP zero as that for a boost converter, and w_2 is normally at a much higher frequency range.

Also, the line-to-output transfer function is given by

$$\frac{\hat{V}}{\hat{V}_g} = \frac{1}{D'} \frac{1+\frac{S}{w_{z1}}}{\left(1+\frac{S}{w_{p1}}\right)\left(1+\frac{1}{Q_{po}}\frac{S}{w_{po}}+\frac{S^2}{w_{po}^2}\right)}. \tag{22}$$

If the time constant of capacitor charging loop τ_c is comparable to the switching cycle, the linear ripple assumption is not satisfied. Therefore, the state-space averaging method does not apply. However, the expression for the dominant double poles W_{po} remains the same as in (17) since they are caused by the resonance between input inductor and the two capacitors, which are independent of τ_c. The accurate small-signal analysis in the higher frequency range can be carried out by using the method of state-space analysis without the linear ripple approximation. The results should be computed numerically since the symbolic expressions for matrices exponential are too involved to be useful.

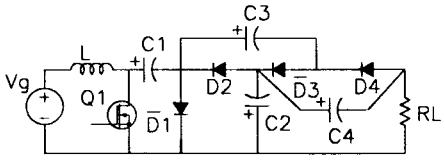


Fig. 4. A capacitor-diode quadrupler extension of the basic three-switch HV converter.

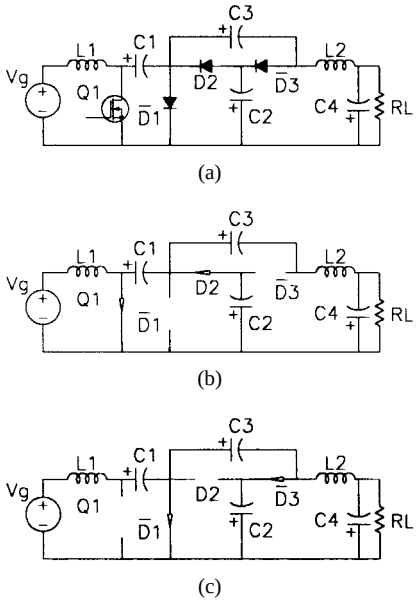


Fig. 5. An extension of the three-switch HV converter with (a) continuous input and output currents, (b) the equivalent circuit during DT_s, and (c) the equivalent circuit during $D'T_s$.

IV. Extensions of the Basic Three-Switch Converter

The first extension of the basic three-switch converter is adding a capacitor-diode voltage multiplier at its output. A quadrupler version of the HV converter is shown in Fig. 4. The output voltage is $-2V_g/D'$. Generally, for an n-stage multiplier, $M = -nV_g/D'$ (one stage consists of two diodes and two capacitors). By using the voltage multiplier, the voltage stress on each switch or capacitor is reduced. Since fast diodes with enormous reverse voltage ratings are hard to find, reduction of the diode ratings decreases the reverse-recovery current in each diode. However, all the diodes are in series with the output at dc (when capacitors can be considered as open branches since no averaged dc current goes through them), and the on loss caused by the forward voltage drop of the diodes is increasing. Also, the capacitance charging loss increases with the number of stages. In addition, output voltage ripple and the dc output resistance increase rapidly with the increasing of n [6]. Therefore, after choosing reasonable voltage ratings for devices, the minimum number of stages should be used to reduce loss and output voltage ripple. In the applications which need enormous step-up ratio, a transformer may be used together with the capacitor diode voltage multiplier to provide the required output voltage.

The full dynamic analysis for the voltage multiplier in Fig. 4 will not be discussed in this paper. However, it is worthwhile to give the dominant double poles, which can be simply

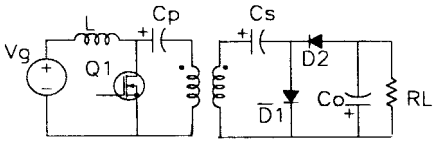


Fig. 6. The dc isolated three-switch converter. The input inductor can be coupled with the transformer.

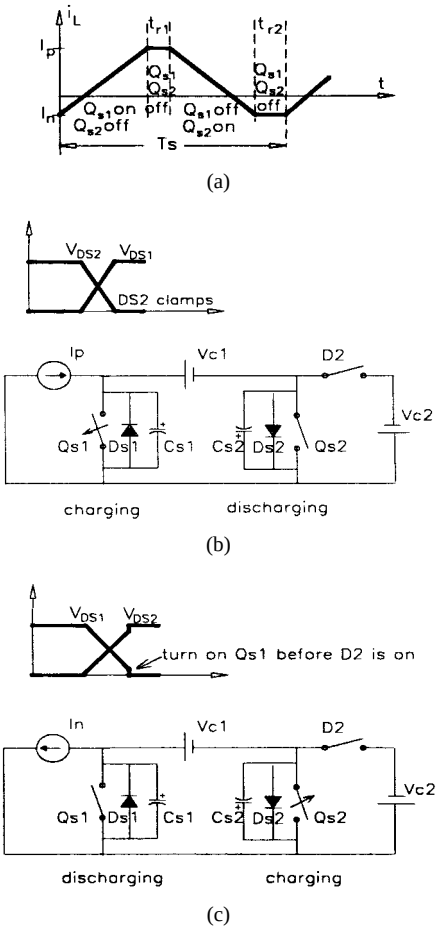


Fig. 7. Soft-switching mechanism: (a) bidirectional inductor current, (b) resonant interval #1, and (c) resonant interval #2.

expressed as

$$w_{po} = \frac{1}{\sqrt{L_e \sum_{i=1}^{4} C_i}} \tag{23}$$

where L_e is defined as in (13).

This result can be extended to the n-stage voltage multiplier, with the summation of all $2n$ capacitances replacing that of the four capacitances in (23). The physical insight is as follows: at low frequency, all capacitors function as though they are in parallel. The total capacitance is resonant with the equivalent inductance, which gives rise to the dominant double poles.

Another interesting converter developed from the three-switch HV converter is shown is Fig. 5, where both the input and output current are continuous. The input inductor L_1 and the output inductor L_2 are in a loop with V_g, C_1, C_2, and C_4, which appear as short circuits at switching frequency and its harmonics. So, L_1 and L_2 are effectively in parallel and have identical ac-voltage waveforms. Hence, the two inductors can be coupled to reduce size and provide the ripple-steering feature.

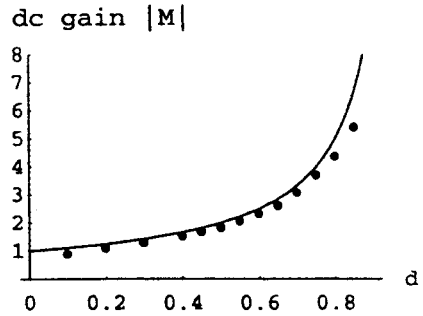


Fig. 8. Theoretical (line) and experimental (dot) dc gain characteristics of the three-switch HV converter in CICM.

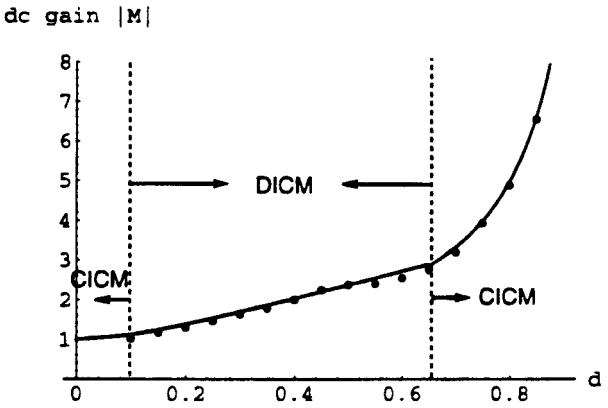


Fig. 9. Verification of the conduction mode type and dc gain in the three-switch converter in DICM when duty cycle is less than 0.65. Theoretical (line) and experimental (dot).

This converter can be viewed as an extension of the Cuk converter by inserting a voltage doubler before the output inductor. The conversion ratio for this converter is $1+D/1-D$, which can be easily derived from equivalent circuits of the converter in intervals DT_s and $D'T_s$ [Fig. 5(b) and (c)].

In comparison with the basic Cuk converter, the new converter operates at lower duty ratio for the same overall conversion ratio. The relation between the respective duty ratios D_N and D is obtained from

$$\frac{1+D_N}{1-D_N} = M = \frac{D}{1-D} \tag{24}$$

which leads to

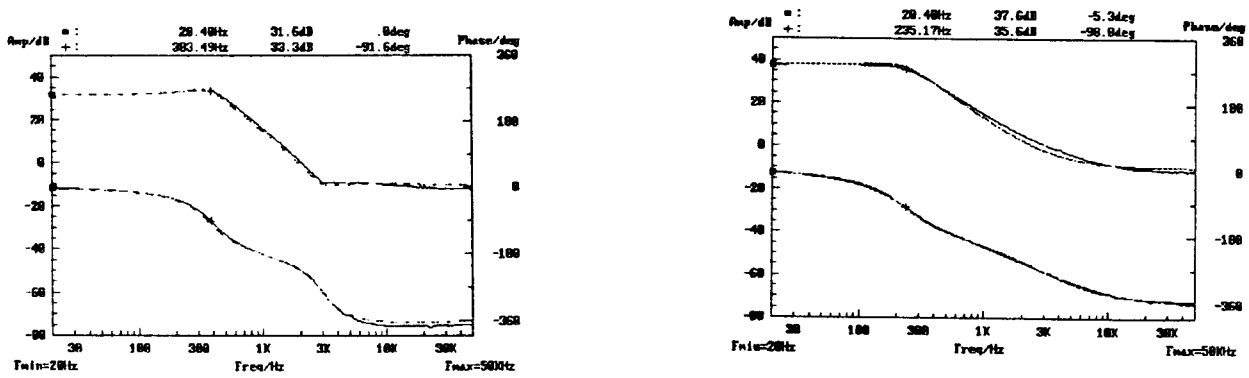
$$D_N = 2D - 1. \tag{25}$$

Clearly, D_N is always lower than D. (D is greater than 0.5 when the Cuk converter works as a step-up converter.)

The voltage stress on the transistor and diodes is

$$V_{\text{off}}^{N} = \frac{V_g}{1-D_N} = \frac{V_g}{2(1-D)} \tag{26}$$

which is half of the switch stress in the basic Cuk converter.



(a) (b)

Fig. 10. Measured (solid lines) and predicted (dashed lines) control-to-output-voltage transfer function: (a) D equals 0.5, and (b) D equals 0.7.

The peak voltage stress on L_1 and L_2 is

$$V_L^N = \frac{D_N}{1-D_N}V_g = \frac{2D-1}{2(1-D)}V_g \tag{27}$$

which is less than half of that in the basic Cuk converter.

Theoretically, a capacitor-diode multiplier with more stages (such as a quadrupler) can be inserted in place of the doubler in Fig. 5. However, this will introduce more losses as explained at the beginning of this section.

For many applications, it is essential to provide dc isolation between input and output and/or multiple outputs of different voltages and polarities. Similar to the Cuk converter, the three-switch HV converter and its extensions have an energy transfer capacitor. By splitting this capacitor into two in series, we can easily insert an ac transformer between the two capacitors. An isolated three-switch HV converter is shown in Fig. 6, where the input inductor and the transformer can be coupled. In the isolated version of the converter in Fig. 5, all the magnetics (input and output inductors and transformer) can be coupled.

V. Zero-Voltage Switching

For a hard-switching converter, in every switching cycle, charge stored in the junction capacitance during the turn-off transition is dumped into the transistor at the beginning of the transistor turn on. This switch turn-on loss is proportional to the switching frequency. It becomes significant at high-switching frequency and high-voltage applications. Moreover, the discharging current introduces high-current spike and high di/dt in the transistor, which result in high-switch stress and electromagnetic interference (EMI) noise. In order to achieve zero-voltage switching at constant switching frequency, the diode D_1 in the converter from Fig. 2 is replaced with the MOSFET Q_2. Soft-switching of both transistors is provided by discharging the junction capacitor across the MOSFET before it is turned on [7]. The simplest way is to design the input inductor such that its current is bidirectional (the peak-to-peak ripple current greater than twice of its average dc current at maximum load). During the transition periods, all the switches are off and the input inductor and the two junction capacitors exchange energy in the lossless resonant mode to realize zero-voltage switching. The mechanism for soft switching is illustrated in Fig. 7(a)–(c) and explained next.

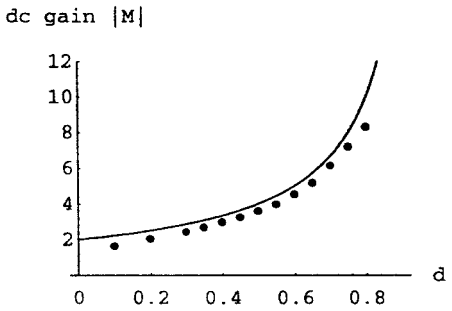


Fig. 11. Theoretical (line) and experimental (dot) dc gain characteristics of the quadrupler extension.

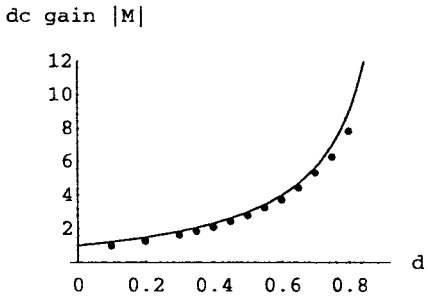
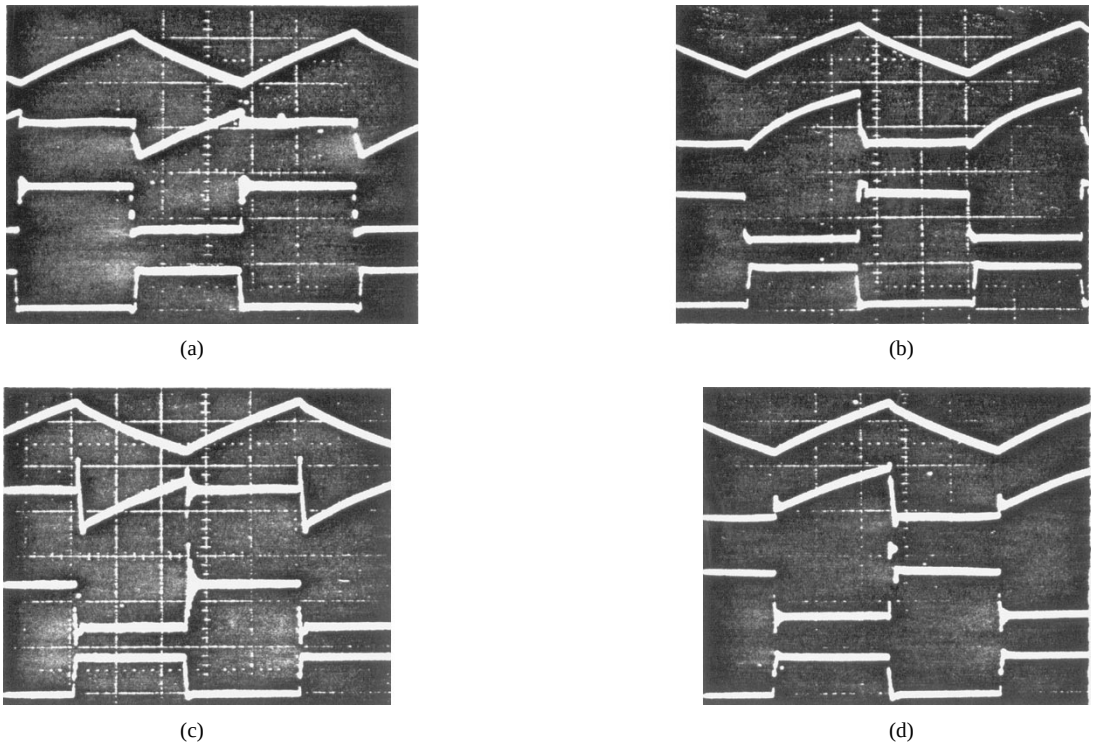


Fig. 12. Theoretical (line) and experimental (dot) dc gain characteristics of the continuous input and output currents extension.

The bidirectional input current is shown in Fig 7(a). Two resonant intervals t_{r1} and t_{r2} are introduced by delaying the turn on of one switch after the turn off of the other. The resonant intervals are assumed to be short compared with the switching period. Therefore, the input inductor can be replaced by current source in Fig. 7(b) and (c). Each MOSFET is replaced by a composite switch, consisting of a main switch, an antiparallel diode, and a junction capacitor. The energy transfer capacitor is replaced by a constant voltage source.

The first resonant interval t_{r1} starts when Q_{s1} is open. D_2 is open simultaneously. The positive peak input current I_p is charging C_{s1} and discharging C_{s2}. When the voltage on C_{s2} is discharged to zero, D_{s2} conducts and clamps the voltage at zero. Now, Q_{s2} can be turned on at zero voltage.



(a) (b) (c) (d)

Fig. 13. Comparison of the three-switch converter with or without soft switching. In each oscillogram photograph: (a) upper trace: input inductor current (5 A/div), (b) upper middle trace: drain-to-source current (5 A/div), (c) lower middle trace: drain-to-source voltage (20 v/div), and (d) lower trace: gate voltage (10 v/div); time scale: 2 μs/div.

The second resonant interval t_{r2} starts when Q_{s2} is turned off. The input current $(-I_n)$ is negative now, C_{s1} is discharged toward zero, and C_{s2} is charged toward V_{c1}. Since I_n is smaller than I_p, t_{r2} is always longer than t_{r1}. There is another difference from the first transition: D_{s1} will never conduct. This can be explained by looking at the loop consisting of C_1, C_2, D_{s1}, and D_2. At the beginning of DT_s, V_{c1} is always bigger than V_{c2}. When $V_{c1}-V_{c2}-V_{cs1}>V_{d2}$ (turn-on voltage of D_2), D_2 would turn on first. The capacitor charging current is usually bigger than the negative inductor current, the difference of these two currents will charge C_{s1}, and V_{cs1} will never reach zero. Therefore, we should turn on Q_{s1} before D_2. Fortunately, the difference between V_{c1} and V_{c2} is usually very small, thus, Q_{s1} is turned on very close to zero voltage.

The resonant transitions also provide zero-voltage turn off for D_2 and reduces the loss caused by the reverse recovery current in D_2.

VI. Experimental Results

First, a prototype of the basic three-switch converter was built to verify analytic results. Components used in this prototype are listed below: Q_1 = IRF540, $D_1 = D_2 =$ ERC88 $-$ 009, $L = 480$ μH, $C_1 = C_2 = 43$ μF, and $r_{c1} = r_{c2} = 0.55$.

The measured and predicted dc-voltage conversion ratios are shown in Figs. 8 and 9 ($V_g = 10$ V and $f_s = 50$ kHz). In Fig. 8, $R_L = 50\ \Omega$ and the converter is always in CICM. The deviation at the high end of the duty cycle is due to the parasitics (lossy elements) inside the converter. When R_L equals 630 Ω, the converter goes into DICM when the duty ratio is less that 0.65, which is consistent with the result from (4) or (5): operating in DICM when $0.094 < D < 0.655$. Since the load current is very small in this case, the parasitic elements have a negligible effect as shown in Fig. 9.

Fig. 10 gives the measured control-to-output transfer functions (where $f_S = 100$ kHz), together with the theoretical predictions from Section III. Good agreements can be observed up to half of a switching frequency.

The voltage conversion ratios of the two extensions of the basic three-switch converter (from Figs. 4 and 5) were measured. Results are displayed in Figs. 11 and 12.

Finally, experiments were done to demonstrate the soft-switching mechanism. Waveforms with and without soft switching are shown in Fig. 13(a)–(d) for comparison. In the experimental circuit, the drain-to-source voltage of each MOSFET is sensed to control the corresponding gate signal. Each MOSFET is turned on when its V_{ds} is close to zero. In Fig. 13(a), it can be seen that the current goes through D_{s2} when Q_{s2} is turned on. Therefore, Q_{s2} is turned on without switching losses. In Fig. 13(c), negative input inductor current discharges V_{ds1} to a negligible small value and the control (gate) signal turns Q_{s1} on before D_2 starts to conduct. After Q_{s1} conducts, D_2 is turned on. The current through Q_{s1} is the summation of the input inductor current and the output capacitive charging current. The high-current spike and oscillation in the hard-switched converter are eliminated by use of the soft-switching technique.

The measured efficiency (when $V_{\rm out} = 44$ V, $I_{\rm out} = 500$ mA) is 92%.

VII. Conclusion

A novel three-switch HV converter derived from the Cuk converter is discussed in this paper. It has the boost-like front end. Automatic current shaping is obtained by operating the converter in DICM. DC and dynamic analyses reveal that it has many similarities to the boost converter. However, exchanging of the position of the diode and capacitor in the boost converter provides significant benefits due to the floating capacitor. First, it can be used to drive a capacitor-diode multiplier, which is the common solution for ultrahigh-voltage application. Second, the isolation of input and output can be easily achieved as in a Cuk converter by splitting the energy transfer capacitor into two and inserting an ac transformer in between.

Another interesting extension, which features both continuous input and output current, is also introduced. The inductors in this converter can be coupled.

Experimental results agree well with the predictions.

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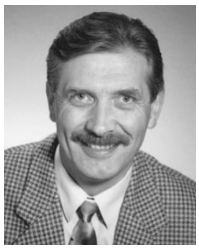

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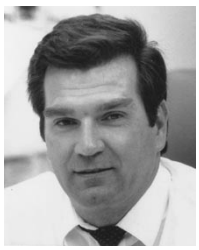

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