A Single Chip Two-stage W-band Grid Amplifier

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Abstract — **The first monolithic Grid Amplifier using a cascade differential-pair amplifier unit cell has been designed and measured. The grid is packaged using a reflection architecture with waveguide input and output. The measured gain at 82 GHz is 5.5 dB. The measured output power is 110 mW with 2.5dB residual gain. The size of the amplifier module is 20 mm ×10 mm×10 mm.**

I. Introduction

Recently, the use of W-band (75-110 GHz) for short-range high-speed communications has been approved by the FCC [1]. The tranceiver to be used in these applications has to be small, low cost and reliable in order to gain a high acceptance rate in the market. Millimeter-wave monolithic integrated circuits (MMICs) satisfy these requirements while traditional MMICs tend to have limited transmitter power, with single-chip output power of 427 mW[2]. Monolithic quasi-optic Grid Amplifiers share the advantages of MMICs with the potential for increased output power through large-scale power combining [3].

Grid Amplifiers, combining the power of several hundred transistors, have been demonstrated [4], and have recently been packaged in waveguide modules [5]-[6]. Unlike other spatial power combining approaches that use multi-stage MMICs [7], Grid Amplifiers have used single-stage amplification that limits the gain. One approach to increase the gain is to have several Grid Amplifiers in cascade [8]. Here we report another approach implementing a multi-stage Grid Amplifier unit cell.

II. Design of The Two-stage Amplifier Cell

The most commonly used two-stage designs are cascode and cascade amplifiers. An advantage of the cascode amplifier is the simplicity of the DC-bias. On the other hand, the cascade amplifier can use a small first-stage transistor that is optimized for gain while a large second-stage transistor can be used for power. The chip presented here uses the cascade approach. The simplified circuit diagram is shown in Fig. 1 with first-stage and second-stage gate-peripheries of 80 μm and 150 μm, respectively. The cell size is 620 μm (Fig. 2) and the entire array is 8×8 with an overall chip size of 5.5 mm × 5 mm. The design of the gate and drain leads follows Preventza *et al.* [9]. The drain bias of the first stage is connected through a feedback resistor which also stabilizes the second stage. Furthermore, the inter-stage capacitor, C_i, inductance of the feedback lead, L_f, and feedback resistor, R_f, provide inter-stage matching. The inter-stage capacitor also provides bias isolation. The second-stage gate uses self-biasing because of space limitations while the first-stage gate bias is controlled externally in order to maximize gain performance.

In order to reduce mutual coupling from the input and output lead to the inter-stage components, all the inter-stage components are enclosed in a source "ring" structure as shown in Fig. 2. Furthermore, because the simulation software does not support periodic (Floquet) boundary conditions, the inter-stage components are put as close to the center of the unit cell as possible. Simulated maximum available gain (MAG) of the chip using Ansoft's High Frequency Structure Simulator (HFSS) and Agilent's Advanced Design System (ADS) at 82 GHz is 9.5 dB. This design is fabricated using Northrop Grumman Space Technology (NGST) 0.15-μm InP power HEMT process [2]. Typical peak transconductance, maximum channel current, and off-state drain-source breakdown voltage are 750 mS/mm, 650 mA/mm, and 7 V. NGST's baseline 75-μm thick InP MMIC process was modified to achieve a 125-μm final thickness for this work.

* C. T. Cheung, M. P. DeLisio and J. J. Rosenberg were at Caltech when this work was done.

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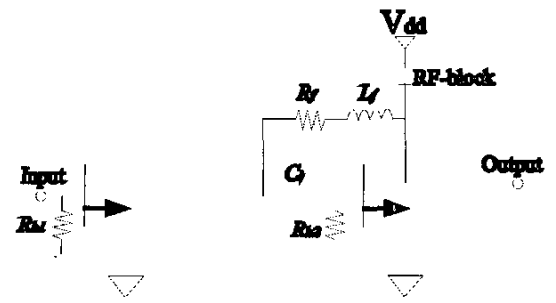

Fig. 1 A simplified circuit diagram for a cascade amplifier unit cell. Only one arm of the differential pair is shown. The drain of the first stage is biased through the feedback resistor, R_f. The first-stage gate is biased exxternally while the second-stage gate is self-biased to the source.

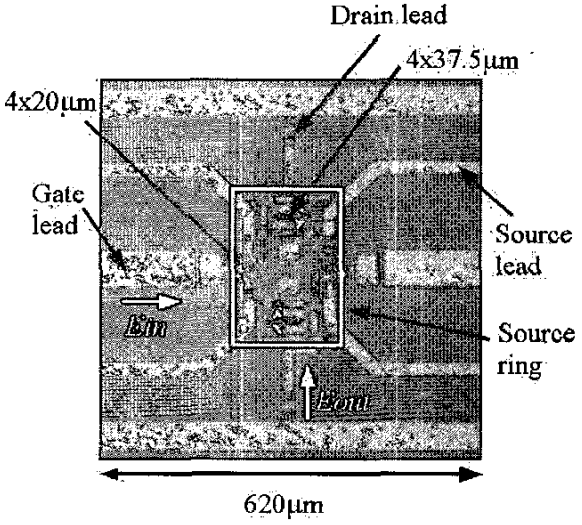

Fig. 2 The fabricated cascade Grid Amplifier unit cell. Each stage consists of two differentially driven transistor pairs.

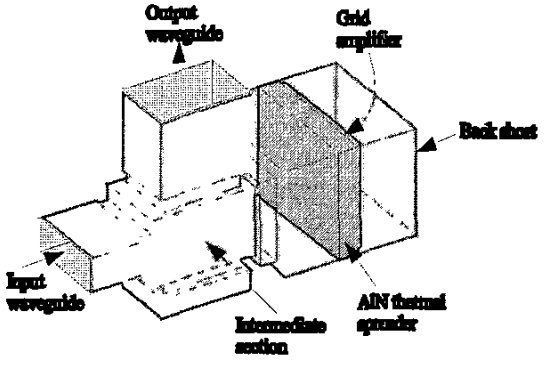

Fig. 3 A drawing of the two-stage Grid Amplifier using a reflection architecture and ortho-mode mode-converter. The thermal spreader is used for impedance matching for both input and output polarizations.

III. Design of the Waveguide Package

We used the reflection approach proposed by Wong [10] and demonstrated in [6]. A drawing of the mode-converter is shown in Fig. 3. The design process starts by designing a port-to-port mode converter that satisfies the desirable mode excitation with no thermal spreader or Grid Amplifier present. Then the amplifier chip, wire-bonds and thermal spreader are included, and the waveguide is then re-optimized for field uniformity across the surface of the chip. The Grid Amplifier is modeled as an impedance sheet set to the conjugate matching impedance in order to reduce simulation complexity. Microstrip low-pass filters are used for the DC-bias circuit to avoid leakage. In this work, the Aluminum Nitride (AlN) thermal spreader was not mounted directly against the back short because impedance matching for the input and output was achieved using the AlN as a quarter-wavelength transformer. Therefore we sacrificed the thermal management advantage of reflection approach in order to improve impedance matching. However, the reflection approach allows both input and output polarizations to use the quarter wave transformer as opposed to the transmission approach. Both input and output are connected to standard WR-10 waveguide. A square intermediate waveguide section is used to combine the TE_{10} and TE_{01} mode efficiently before expanding into the bigger over-moded waveguide. The size of the packaged amplifier including flanges is about 20 mm ×10 mm ×10 mm.

IV. Measurement Results

The waveguide unit was machined from brass and was gold plated to reduce loss. A photograph is shown in Fig. 4. We measured that the gold plating reduces the loss by 2.5 dB. A split-block approach is used to simplify machining. More advanced methods may reduce the amount of passive loss by removing the split-block cuts in the waveguide. Fig. 5 shows a photograph of the mounted chip and Fig. 6 shows the detailed cross-section of the assembly. The filter and the wirebonds affect the boundary condition of the over-moded waveguide. Therefore it is necessary to simulate them in order to understand the effects on the matching and field uniformity. DC-bias filters are fabricated on Roger's Duroid with relative dielectric constant of 2.2. The filter is designed such that in the operating frequencies, the transmission coefficient, S21, is less than −30 dB. Finally the chip was mounted on heat spreader and wire-bonded to the bias lines. In order to remove heat, water cooling was used with the water pipe soldered onto the back short.

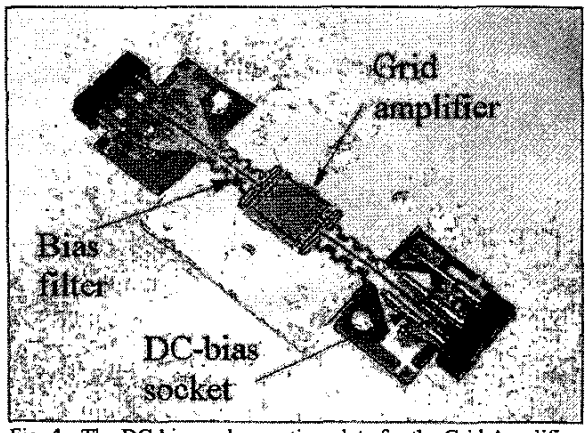

Fig. 4 The DC-bias and mounting plate for the Grid Amplifier. A band-stop filter is used to prevent RF interference. The thermal spreader is mounted by the method described in [5].

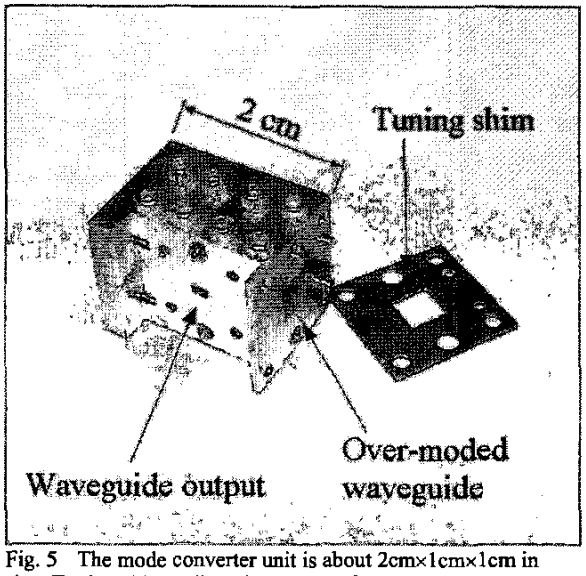

Fig. 5 The mode converter unit is about 2cm×1cm×1cm in size. Tuning shims adjust the distance from the mode converter to the chip for matching. This adjustment affects input and output matching simultaneously.

During measurements, the entire array was biased at a drain voltage of 1.6V and a total current of 5.2A. The first stage gate bias was set to –0.2V, which was found to give the best small-signal gain for the 1.6V drain bias. The transistors can be biased to 3V, but we were forced to use a lower bias due to thermal concerns. The low bias will limit both the gain and output power. Improved heat sinking will allow the device to be fully biased.

The measured small-signal gain and return losses are shown in Fig. 7. These measurements were made with a millimeter-wave vector network analyzer, which was calibrated to the WR-10 waveguide flanges of the Grid Amplifier module. The peak gain is 5.5 dB at 82 GHz, with a 3-dB bandwidth of 400 MHz. The input reflection coefficient is less than –5 dB and the output reflection coefficient is less than –10 dB over this frequency range. The poor bandwidth is due to highly mismatched input and output impedances, and is being addressed in an upcoming design. Furthermore, we suspect that losses in waveguide package may be considerable. Our simulations indicate that out of band, the grid should be highly reflective at both the input and the output. The measurements of S11 and S22 indicate that the passive losses may be 0.5 to 1 dB for the input and the output.

Fig. 8 shows the large-signal performance. For testing, we used a Backward-Wave Oscillator (BWO). The BWO output power prevented our measuring the amplifier's output power beyond 110 mW where the amplifier had 2.5 dB residual gain. At 110mW output power, the power-added efficiency (PAE) is 0.6%. Note that at low output powers, this measurement is 1 dB less than the small-signal gain as measured by the network analyzer; we suspect that this measurement may overestimate the input power due to excess noise generated by the BWO. The gain saturation curve has an unusual shape, indicating an early saturation leveling off to 2.5 dB. This could indicate a very poor field uniformity, with relatively few devices being illuminated. It could also be the result of the small first-stage transistor saturating prematurely.

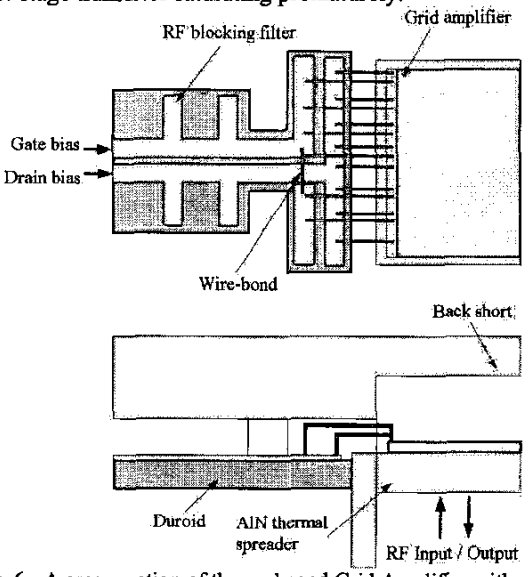

Fig. 6 A cross-section of the packaged Grid Amplifier with DC-bias. The grid is attached onto the AlN thermal spreader by thermal glue. The gate bias line, which carries low current, bridged over the drain bias line using bond wires. The source is connected to the waveguide chassis.

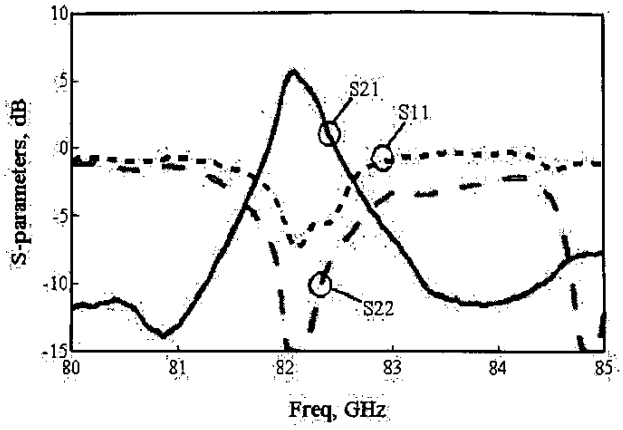

Fig. 7. The small-signal S-parameters of the Grid Amplifier with drain voltage and drain current of 1.6V and 5.2A, respectively.

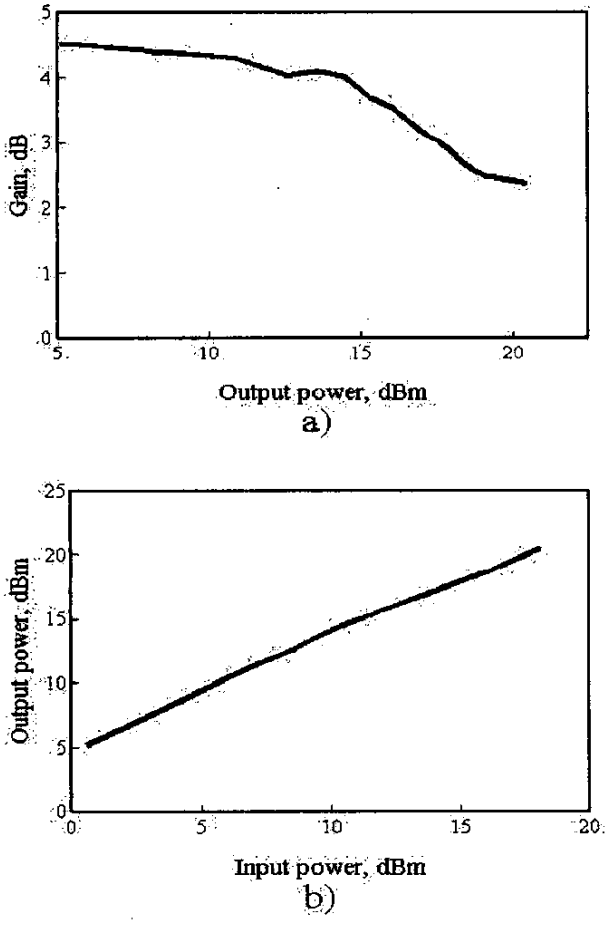

Fig. 8. Measured, a) gain saturation and b) output power curve at 82GHz. The maximum measured output power is 110mW with 2.5dB residual gain.

V. Conclusion

We have demonstrated a W-band monolithic two-stage Grid Amplifier packaged in waveguide. The measured small-signal gain is 5.5 dB at 82 GHz with 3-dB bandwidth of 400 MHz. The measured maximum output power is 110mW. This is the first demonstration of a two-stage Grid Amplifier cell as well as the first demonstration of a packaged Grid Amplifier at W-band.

Acknowledgements The authors appreciate the support from the Army Research Office through the Caltech Quasi-Optic Power Combining MURI program and Lee Center for Advanced Networking. The authors would also like to thank Professor Sander Weinreb for lending measurement equipment to facilitate the power measurement.

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