The First Asynchronous Microprocessor: The Test Results

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We have designed the first entirely asynchronous (also called *self-timed* or *delay-insensitive*) microprocessor. The design was reported at the *Decennial Caltech Conference on VLSI*, last March. The conference paper is included here as an appendix. Since the chips had not yet been fabricated at the moment of writing the conference paper, the paper does not include the results of the experiment. The purpose of this note is to publish these results, which are quite remarkable because of the speed reached on this first design, and, as importantly, because of the surprising robustness of the chips to variations in temperature and *VDD* voltage values.

The processor has a 16-bit, RISC-like, instruction set. It has sixteen registers, four buses, an ALU, and two adders. Instruction and data memories are separate. The chip size is about 20,000 transistors. Two versions have been fabricated: one in $2\,\mu m$ MOSIS SCMOS, and one in $1.6\,\mu m$ MOSIS SCMOS. (On the $2\,\mu m$ version, only 12 registers were implemented in order to fit the chip on the 84-pin $6600\,\mu m \times 4600\mu m$ pad frame.)

With the exception of *isochronic forks* (see attached paper), the chips are entirely delay-insensitive, i.e., their correct operation is independent of any assumption on delays in operators and wires except that the delays be finite. The circuits use neither clocks nor knowledge about delays.

The only exception to the design method is the interface with the memories. In the absence of available memories with asynchronous interfaces, we have simulated the completion signal from the memories with an external delay. For testing purposes, the delay on the instruction memory interface is variable.

Although this is the first processor this team has ever designed, it was completed in five months, and the chips were functional on first silicon. In spite of the presence of several floating n-wells, the $2\,\mu m$ version runs at 12 MIPS. The $1.6\,\mu m$ version runs at 18 MIPS. (Those performance figures are based on measurements from sequences of ALU instructions without carry. They don't take advantage of the overlap between ALU and memory instructions.) Those performances are quite encouraging given that the design is very conservative: It uses static gates, dual-rail encoding of data, completion trees, *etc.*

Only two of the 12 $2\,\mu m$ chips passed all tests, but 34 out of the 50 $1.6\,\mu m$ chips were found to be entirely functional. (However, within a certain range of values for the instruction memory delay, the $1.6\,\mu m$ version is not entirely functional. We cannot explain the phenomenon yet.) It takes less than 700 instructions to test the processors for stuck-at faults. The program counter is the only part that was not tested exhaustively because the memory used for the test did not contain the address required for testing the most significant bit of the program counter.

We have tested the chips under a wide range of *VDD* voltage values. At room temperature, the $2\,\mu m$ version is functional in a voltage range from 7V down to 0.35V! And it reaches 15 MIPS at 7V. We have also tested the chips cooled in liquid nitrogen. The $2\,\mu m$ version reaches 20 MIPS at 5V and 30 MIPS at 12V. The $1.6\,\mu m$ version reaches 30 MIPS at 5V. Of course, the measurements are made without adjusting any clocks (there are none), but simply by connecting the processor to a memory containing a test program and observing the rate of instruction execution. The results are summarized in Figure 1. Figure 2 shows that the optimal *power-delay product* is obtained at 2V at room temperature.

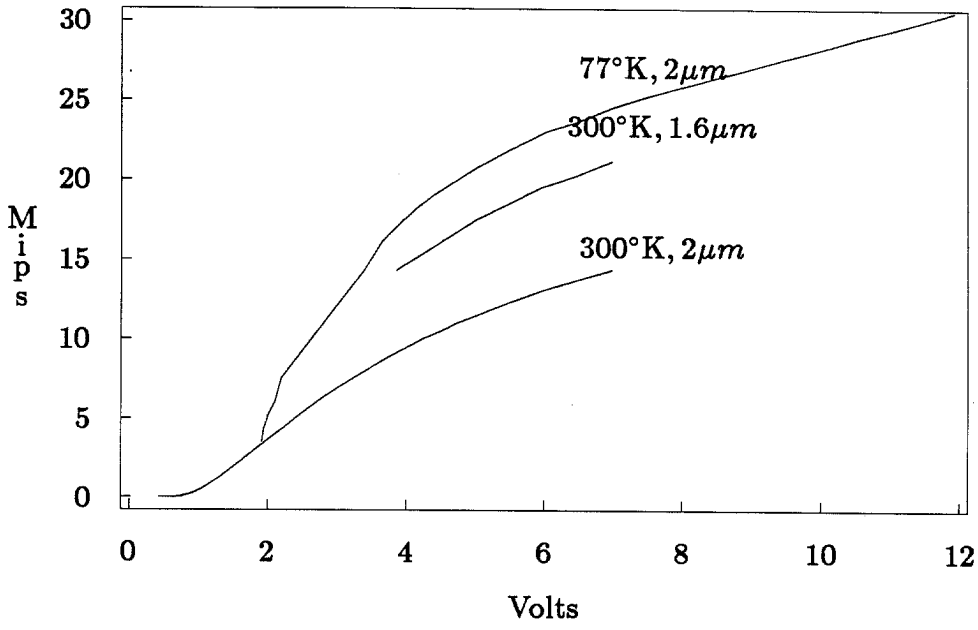

Figure 1: MIPS as a function of VDD

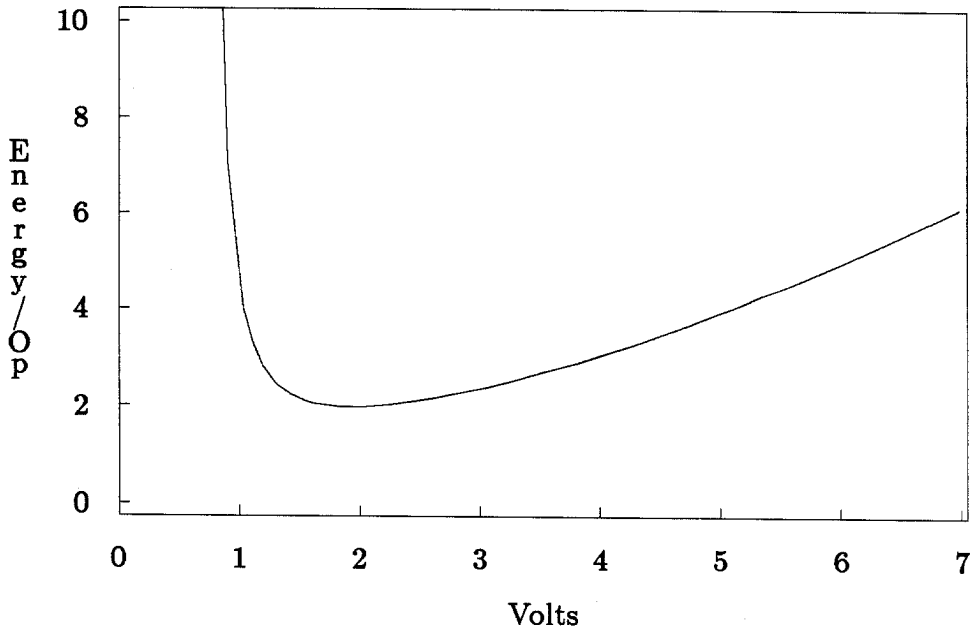

Figure 2: Power-delay product as a function of VDD