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The Role of the Substrate on Pattern-Dependent Charging

Gyeong S. Hwang and Konstantinos P. Giapis

Division of Chemistry and Chemical Engineering, California Institute of Technology, Pasadena, California 91125, USA

ABSTRACT

Monte Carlo simulations of charging and profile evolution during plasma etching reveal that the substrate can mediate current imbalance across the wafer. This function couples patterned areas, where the electron shading effect dominates, to substrate areas directly exposed to the plasma. When a net positive current flows through the pattern features to the substrate, increasing the exposed area decreases the substrate potential, thereby causing notching at the connected feature sidewalls to worsen, in agreement with experimental observations.

When plasma-etching patterned wafers, the sheath-induced directionality difference between ions and electrons at the wafer causes differential microstructure charging,[1] which affects the current balance at the bottom of trenches, can lead to profile distortion (notching),[2,3] and may induce electron tunneling through thin gate oxides.[1,4] Charging damage ensues when large tunneling currents cause electrical degradation or even breakdown of the oxide.[5] The magnitude and direction of the tunneling current depends critically on the substrate potential.[1,4] When exposed to the plasma, the substrate, even when lightly doped, can provide a path to plasma electrons to reach patterned areas from below, change the potentials of features connected to it, and thereby influence the in-trench ion dynamics. Since the substrate connects electrically all chips on a wafer, it can profoundly influence charging damage, especially in the presence of plasma nonuniformities or variations in the pattern geometry. The confusion surrounding charging effects[6] has thus far prevented understanding of the role of the substrate in mediating current balance across the wafer.

Often in real processing, a wafer has an SiO_2 layer on its back side that wraps over to the front edge;[6] then, electrical contact of the substrate with the plasma can occur only through patterned areas or places where the oxide has been removed. Any current imbalance at a patterned area, where polysilicon or metal gates are connected to the substrate directly or through thin (< 10 nm) oxide, influences the substrate potential, thus affecting the current balance at other patterned regions or exposed areas. This possibility was recognized early on by Hashimoto[1] and was investigated more thoroughly by Ogino *et al.*[7,8] The latter used special line-and-space (L&S) structures of masked polysilicon gates, electrically connected to the substrate through a narrow via underneath. Notch occurrence was used as an indication of the gate and substrate potentials. A key result of this study was a linear increase in notch depth with exposed substrate area. It was suggested that more plasma electrons entering through the larger exposed area were able to reach the gates, decrease their potential, perturb the in-trench ion dynamics, and cause the notch to deepen. Although these suggestions provide a reasonable interpretation of the experimental results, they remain heuristic. In this article, we attempt to quantify the role of the substrate potential on pattern-dependent charging through simulations.

The Monte Carlo based simulation, described in detail elsewhere,[3] couples sheath dynamics, charged particle dynamics, topography charging, surface chemistry, and scattering effects. Ion and electron trajectories are followed as they cross local electric fields which are self-consistently modified as charge accumulates on various surfaces. The substrate is treated as a conductor whose potential changes in response to any imbalance in the ion and electron currents, reaching it through patterned surfaces and/or areas directly exposed to the plasma.

Typical high-density plasma conditions are assumed: plasma density of 1×10^{12} cm^{-3}, electron temperature of 0.5 V. The wafer electrode is biased at 1 MHz with a peak-to-peak voltage of 50 V. The pattern consists of four isolated 0.3 μm lines separated by 0.3 μm spaces (trenches). At the onset of overetching, each feature consists of a 0.6 μm photoresist mask onto 0.3 μm n^+-poly-Si, formed on top of a thick (> 100 nm) layer of SiO_2. A narrow poly-Si conduit under each line allows for electrical connection to the substrate. Identical patterns are separated by large open areas, in the middle of which the substrate is exposed to the plasma (Fig. 1). The ratio R of the exposed area (A_o) to the patterned area (A_p) is a simulation parameter.

We begin by performing a simplistic calculation, where the patterned area is neglected, to reveal how the substrate potential influences the balance of the ion and electron currents arriving at the exposed area. The substrate potential is artificially increased while the relative steady-state flux of ions and electrons impinging at the open area is monitored (Fig. 2), taking into account the electric field perturbation above the exposed area.[a] As soon as the substrate potential is increased, the balance between the electron and ion flux is perturbed. More electrons are attracted by the larger potential, and more ions are repelled, but the flux of ions repelled is less than the flux of electrons attracted as a result of the differences in the translational energy of the ions and electrons exiting the sheath. While a small positive potential (≤ 5 V) perturbs the trajectories of many electrons, it hardly influences the more energetic ions. At a substrate potential of 10 V, the electron flux increases by about 45% of the flux to the 0 V surface, while the ion flux decreases by only 25%. Little change occurs to the electron

[a] The electric field above the open area is calculated by solving iteratively the Laplace equation, $\nabla^2 V = 0$, subject to boundary conditions: constant potential at the exposed substrate ($V = V_s$), $V = 0$ at a plane located 3.5 μm above the surface, $\Delta V = 0$ at vertical boundaries located to the left and right of the exposed segment at approximately 20 times its length. The surface around the open area is flat and perfectly insulating. Its potential is modified self-consistently until steady-state charging is reached.

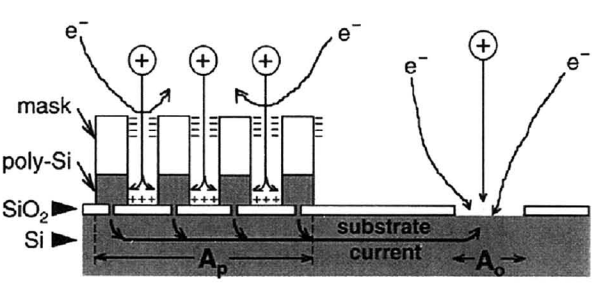

Fig. 1. Schematic of the simulated structure and the charged particle balances.

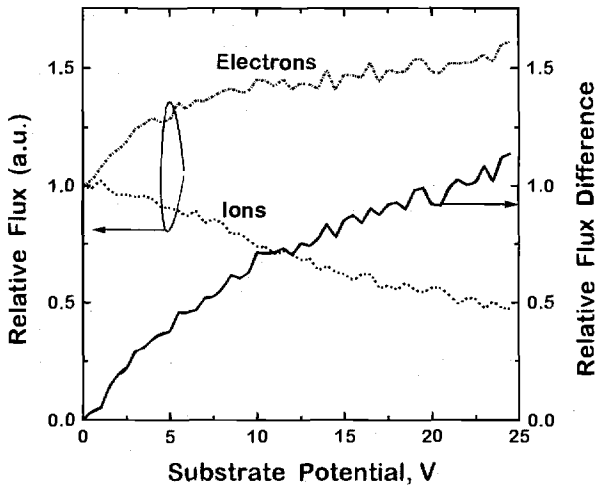

Fig. 2. The relative flux of electrons and ions, arriving at an exposed substrate area, as a function of the substrate potential (varied artificially). The difference between the two fluxes is also shown.

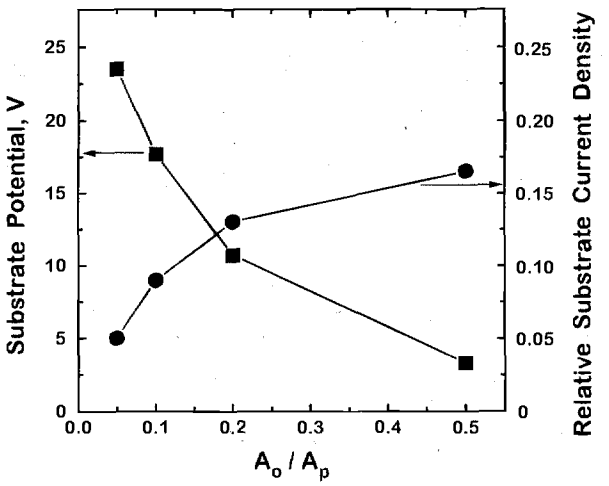

Fig. 3. The substrate potential and the relative substrate current density dependence on the ratio R of the exposed substrate area (A_o) to the patterned area (A_p); for definitions, see Fig. 1.

flux between 10 and 25 V, while the ion flux continues to decrease significantly. As a result, the net negative current to the exposed substrate increases considerably, even beyond the point where the electron current appears to saturate. Although the absolute values of changes in currents are plasma-parameter-dependent, the trends should be universal.

When the patterned area is considered, electron shading results in a net ion current to the poly-Si gates and, through the connection, to the substrate. The gate/substrate equipotential increases; more plasma electrons are attracted to the open area, closing the circuit. In the calculation, the equipotential is allowed to vary in response to the influx of charged particles by implementing a self-consistent iterative procedure, where small sequential increases caused by excess ion current through the patterned area are followed by increases in the electron current to the open area, until the currents balance perfectly. At that point, charging reaches steady state; the potentials of all surface segments and the in-trench electric fields no longer vary.[b]

For a given substrate potential, increasing the exposed area increases the absolute negative current to the substrate. Assuming, for an instant, a constant net ion current to the bottom of the patterned area, the latter observation implies that a current imbalance would ensue, unless the substrate potential is decreased. However, a lower substrate/gate potential increases the ion flux to the sidewalls and to the substrate. This feedback mechanism leads to a new steady state. Results from iterative charging calculations, repeated for increasing ratios R of the exposed substrate area to the patterned area, are plotted in Fig. 3. The substrate potential does indeed decrease with R, approaching 0 V for very large values of R. Simultaneously, the substrate current, equal to the net ion current through the patterned area, increases significantly,[c] as expected by the perturbation to the steady-state in-trench charging potential distributions (Fig. 4), induced by the decrease in the gate/substrate equipotential. Gradients on such potential surfaces are a measure of the electric field that influences ion motion. As previously shown,[3] potential peaks near the sidewall feet of the gates, lead to notches. When the exposed substrate area is very small (Fig. 4a), so are the peaks. The sidewalls acquire a potential (≈23 V) larger than the potential surface in the trench, except near the peaks. Then, the ion energy-flux to the sidewalls is small, causing minute notches to form at long overetching times. Upon increasing R from 0.05 to 0.20 and 0.50, the peaks grow dramatically and move toward the trench middle. This behavior is simply a consequence of the decrease in the potential of the sidewalls (see Fig. 3); fewer plasma electrons are attracted into the trench, forcing the bottom potential to increase. Note how the potential surface away from the peaks is curved toward the sidewalls (Fig. 4c). The ion energy-flux to the sidewalls increases significantly, forecasting the appearance of larger and deeper notches.

Notch profiles for various values of R have been generated, as described elsewhere,[3] and some profiles are shown as insets in Fig. 5. In the same figure, the notch depth is shown to increase linearly with the substrate area exposed to the plasma, capturing the experimental results of Ogino *et al.*[7] (see their Fig. 10).[d] The linear relationship is expected to break down upon further increase of R, as the substrate potential decreases more slowly beyond $R = 0.5$.

Additional proof for the role of the substrate as a mediator of current balance between patterned and exposed areas is provided by experiments where the resistivity of the contact between gate (especially when metallic) and substrate is increased or where a thin oxide separates the gate from the substrate. Tabara[9] reported that when metal (Ti) gates were connected to a p-type substrate ($p = 10^{15}$ cm^{-3}), yielding nonohmic contacts of high resistivity, the notch depth was significantly smaller than in other samples, where the same gates were connected to n-type substrates or an n^+ or p^+ layer. Clearly, the nonohmic contact behavior impedes the rapid transfer of charge from the gates to the substrate, allowing for a higher gate potential, and thus a smaller ion energy-flux to the sidewalls. Moreover, Ogino *et al.*[8] also demonstrated that the notch depth decreased with the thickness of an oxide layer, grown at the bottom of the connection. Sufficiently thin oxides (≤ 10 nm) yielded the same notch depth as the case without oxide, a result explained by electron tunneling from the substrate to the gates, which occurs readily at such ultrathin oxides. However, the notch depth decreased exponentially with oxide thickness (> 10 nm) to become negligible at thicknesses > 50 nm, as expected from the dependence of the Fowler-Nordheim tunneling mechanism on oxide thickness.[10] These results apply only to intermediate gates. The edge gates showed classic notching at the inner sidewall, as expected.[2]

How can one minimize notching in such structures? In addition to the chemical routes proposed elsewhere,[3] the role of the substrate can be exploited: the area of the substrate exposed directly or through interconnections to the plasma must be minimized. This idea was first suggested by Ogino *et al.*,[8] but was later recanted by the same authors[7] when multiple patterns connected to the sub-

[b] As notching evolves, charging of the etched SiO_2 perturbs the local electric field in the vicinity of the notch. In spite of its importance for notching, this perturbation affects minutely the ion current to the substrate.

[c] For fixed plasma parameters and pattern geometry, the substrate current saturates for sufficiently large R, since the maximum net current to the trench bottom is controlled by the electron shading effect, which is independent of the open area size.

[d] In the same Fig. 10 of Ref. 7, the notch depth is also shown to decrease with the area of the exposed Si substrate. In this case, multiple patterns were separated by large SiO_2-covered open areas, providing a large perimeter for the collection of electrons. The electron supply was large enough to make the substrate potential slightly negative. Then, exposing the substrate to the plasma repels electrons, resulting in a net positive current through the exposed area to balance the net electron current through the pattern. As the exposed substrate area increases, the substrate potential becomes less negative (increases), thereby decreasing the notch depth.

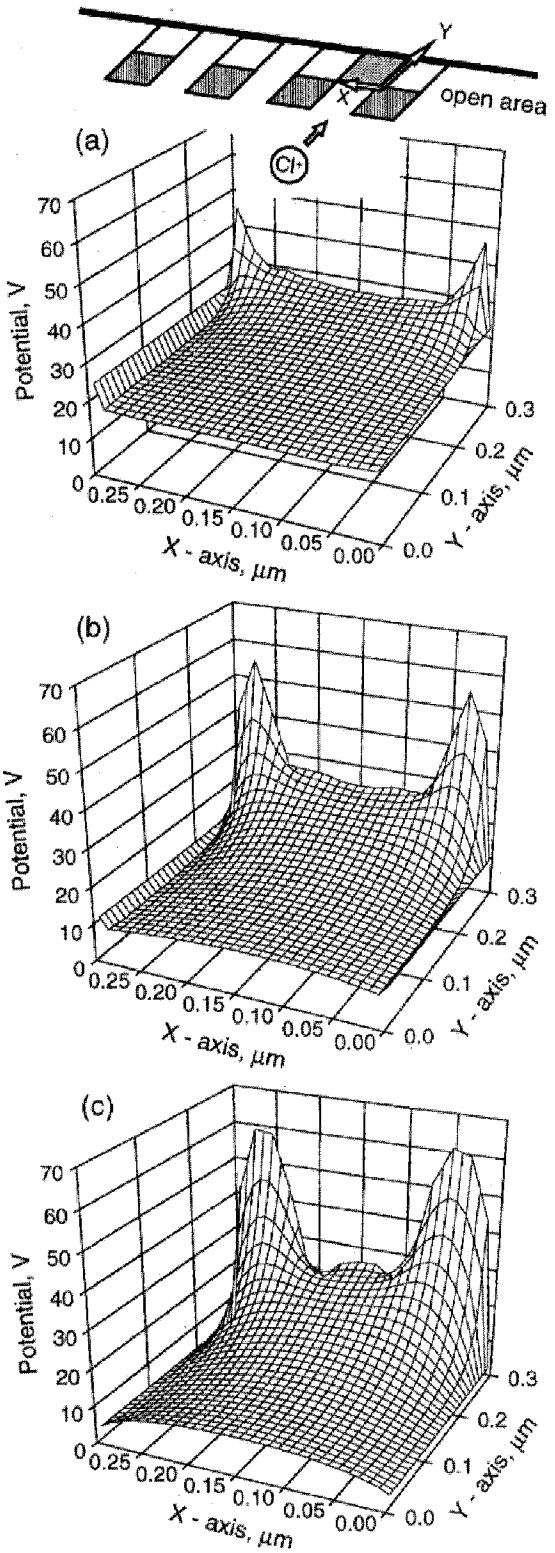

Fig. 4. Three-dimensional charging potential distributions in the trench area between any two gates for R values of (a) 0.05 (b) 0.20 and (c) 0.50. The inset illustrates the area of interest and defines the origin for the potential surface for the edge trench. The microstructure has been rotated to allow for a more convenient description of ion motion in the trench. The arrows show the direction of ions as they approach the potential surface.

strate showed significant notching with no exposed substrate area. However, this result does not contradict the original idea; the multiple patterns were separated by large spaces, thus offering a large perimeter for the collection of charge at edge lines,[2] resulting in a negative substrate potential. (See footnote d.) If the edge gates

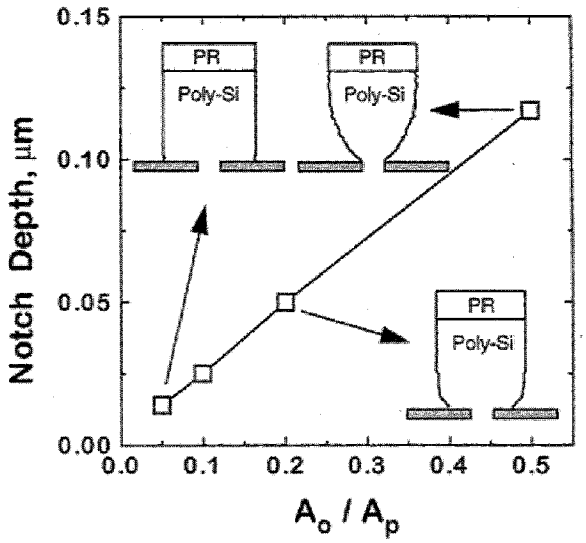

Fig. 5. Notch depth dependence on the ratio R of the exposed substrate area (A_o) to the patterned area (A_p). Simulated notch profiles at the sidewalls of any gate after 100% overetching are shown as insets. The mask has been truncated to save space; the gate aspect ratio has been preserved.

were not connected to the substrate, no notching would have occurred at intermediate lines. Elimination of all reasons for pinning the substrate potential low also has important implications in the reduction of tunneling current transients through thin gate oxides.[11]

In conclusion, simulations of charging and profile evolution during plasma etching of patterned structures suggest that the substrate plays an important role in mediating current imbalance at various regions across the wafer. Open areas directly exposed to the plasma are particularly effective in establishing a net current influx of the opposite charge than that caused by electron shading at patterned regions. The substrate potential that facilitates the current balance can affect notching at gates connected to the substrate. For notch reduction to intermediate lines of a pattern, both the substrate area directly exposed to the plasma and the perimeter of edge lines connected to the substrate should be minimized.

Acknowledgment

This work was supported by an NSF-Career Award and a Camille Dreyfus Teacher-Scholar Award to K.P.G. An Applied Materials Scholarship in partial support of G.S.H. is gratefully acknowledged.

Manuscript received Aug. 25, 1997.

California Institute of Technology assisted in meeting the publication costs of this article.

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