

# Modeling of charging damage during interlevel oxide deposition in high-density plasmas

Gyeong S. Hwang and Konstantinos P. Giapis<sup>a)</sup>

*Division of Chemistry and Chemical Engineering, California Institute of Technology, Pasadena, California 91125*

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Monte Carlo simulations of pattern-dependent charging during interlevel dielectric (ILD) deposition in high-density plasmas reveal that the initial conformality of the ILD film plays a crucial role in metal line charging up and the subsequent degradation to the buried gate oxide to which the metal line is connected. Line charging occurs when the top dielectric is thick enough to prevent tunneling currents while the sidewall dielectric thickness still allows tunneling currents to flow to the metal line; the differential charging of the sidewalls, which induces the latter currents, is caused by electron shading. The results suggest that charging can be reduced by depositing a more conformal ILD film around the metal line and/or by increasing the ability of the film surface to dissipate charge. © 1998 American Institute of Physics. [S0021-8979(98)08813-6]

## I. INTRODUCTION

Pattern-dependent charging<sup>1</sup> is a serious problem in high-density plasma (HDP) etching of gate electrodes and metal interconnect lines because it can cause apparent sidewall irregularities (notching, bowing, etc.) and latent gate oxide degradation.<sup>2,3</sup> Since such forms of damage are feared to impede progress towards smaller critical dimensions, the topic has attracted considerable interest in the past few years. Pattern-dependent charging originates in the directionality difference between ions and electrons as they cross the plasma sheath and, subsequently, interact with mixed conducting and insulating microstructures.<sup>1</sup>

Thus far, the vast majority of studies have been focused on metal or polysilicon etching and resist ashing, where large aspect ratio features make observation of charging damage a facile undertaking. Very few reports of charging damage during plasma-assisted deposition have been published up to now; all of them center on interlevel dielectric (ILD) deposition in both conventional and high-density plasmas. Cheung and Pai<sup>4</sup> reported serious charging damage during plasma-enhanced tetraethylorthosilicate (PETEOS) deposition of interlayer oxide at the metal-1 level. Contrary to the expectation that charging damage would saturate as the oxide layer got thicker, they discovered that it actually became worse. The surprising trend was attributed to photoconduction caused by vacuum ultraviolet photons from the plasma, which could allow the metal line to receive more charge through the oxide. Stamper *et al.*<sup>5</sup> observed significant charging damage only during PETEOS of *doped* oxide; “no measurable charging (damage) occurred during silane-based or undoped TEOS depositions.” It was speculated at the time that the introduction of dopant gas (trimethylphosphine) increased the plasma nonuniformity which has been linked to charging damage.<sup>6</sup> The degree of plasma nonuniformity required for damage to occur in commercial

plasma tools renders the proposed explanation unlikely.<sup>7</sup> Sporadic charging during undoped oxide deposition in conventional plasmas has been reported by Hook *et al.*<sup>8</sup> The inconsistent charging from run-to-run, combined with a tool dependence that did not correlate with other insulator characteristics (such as gap fill), preventive maintenance, or any other known activity on the tool, led these authors to conclude that their “wafers were experiencing sporadic arcing events caused by virtually immeasurable differences in the individual tools at different times.” Remarkably, deposition at higher pressure completely eliminated the charging damage in agreement with observations by Stamper *et al.*<sup>5</sup> Hook *et al.*<sup>8</sup> also used a HDP deposition process (at unspecified conditions) and found no evidence of charging damage. Earlier, Bothra *et al.*<sup>9</sup> compared conventional plasma-enhanced versus HDP oxide deposition and reported significant charging damage only for unoptimized HDP deposition processes performed at high plasma power. Interestingly, they also found that the damage in the unoptimized HDP could be prevented when a thin oxide layer was deposited first by the nondamaging PETEOS process.

The conflicting nature of the aforementioned observations suggests that charging damage during plasma-enhanced deposition is, perhaps, more complex than during plasma etching. The migration towards HDP intermetal dielectric deposition to improve gap-fill capabilities of higher aspect ratio trenches at lower temperature,<sup>10</sup> bears the risk of increased charging damage and warrants a theoretical study to understand how charging is brought about; only then possible pitfalls and limitations of HDP tools and processes can be uncovered in a timely manner.

## II. MODELING CONSIDERATIONS AND ASSUMPTIONS

We report here our initial efforts to model charging during ILD deposition, aiming to uncover when and how charging occurs on a metal line which is progressively coated with thicker dielectric. The problem is fairly complex requiring

<sup>a)</sup>Electronic mail: giapis@cheme.caltech.edu

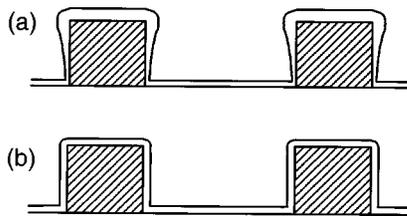


FIG. 1. Profiles of the deposited oxide by the two models considered: (a) neutral-flux-limited growth (nonconformal), and (b) reaction-rate-limited growth (conformal). Most of the charging damage occurs before the oxide grows to the thickness shown.

modeling of a variety of phenomena occurring simultaneously across disparate time and length scales. We have developed tools to handle charged particle dynamics in local electric fields,<sup>11</sup> surface charging,<sup>11</sup> electron tunneling,<sup>12</sup> and surface charge dissipation.<sup>13,14</sup> We shall assume a simple oxide deposition model that describes two extreme situations, schematically shown in Fig. 1: (a) neutral-flux-limited oxide growth, where the film thickness increases proportionally to the flux of neutral precursors arriving at a surface segment of the pattern (nonconformal step coverage), and (b) reaction-rate-limited oxide growth, where the film thickness is independent of the neutral precursor flux and the same on all surfaces at all times (conformal step coverage). In the former case, the oxide layer is thicker on top of the metal lines than at the bottom of the trench or at the sidewalls, a consequence of geometric shadowing of the isotropic neutral precursors by the topography. The realistic deposition process is expected to be somewhere in between the two extreme cases.<sup>10</sup> The detailed mechanism of the oxide growth is neglected; this should not alter conclusions about charging damage, as long as the oxide quality is not affected. We assume that electron tunneling through the deposited oxide layer occurs like in very good quality oxide,<sup>1,12</sup> however, surface charge dissipation is controlled by a threshold electric field,  $\tilde{E}_s$ , for subsurface conduction or surface discharging,<sup>13,14</sup> which depends on dielectric quality, surface roughness, and surface adsorbates.<sup>15</sup> Photoconduction is neglected.

A cross section of the structure to be simulated is depicted in Fig. 2. Metal lines of square cross section ( $0.3 \times 0.3 \mu\text{m}^2$ ) extend in the direction perpendicular to the figure to a length such that the ratio of the area of the metal line (footprint) to the area of the gate oxide is 20 000:1 (antenna ratio). The trenches are  $0.6 \mu\text{m}$  wide (aspect ratio=0.5). Each metal line is electrically connected to a polysilicon gate at a lower level, which is separated from the substrate by a 3.0-nm-thick gate oxide. The substrate is grounded.<sup>16</sup> Typical parameters for HDP are assumed: low pressure ( $<10$  mTorr), electron density= $5 \times 10^{12} \text{ cm}^{-3}$ , electron

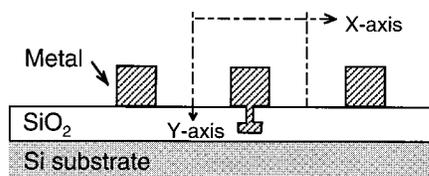


FIG. 2. Schematic of the structure considered and the simulation domain.

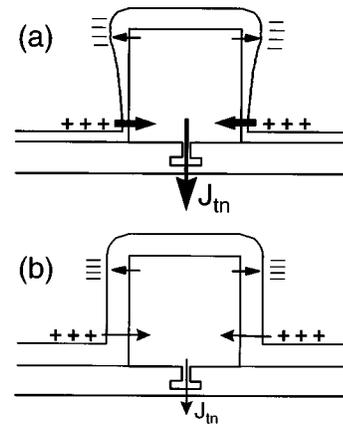


FIG. 3. Schematic of the charging mechanism suggested by the simulations. Examples are shown for (a) nonconformal, and (b) conformal step coverage. Thicker arrows represent larger tunneling currents; arrow direction is for positive current flow (conventional). The oxide thickness is grossly exaggerated for illustration purposes.

temperature= $4 \text{ V}$ , ion temperature= $0.5 \text{ V}$ , no applied rf bias. As the deposition time is increased, the oxide thickness on the top surface and the sidewalls changes according to the two simple models described earlier. Monte Carlo based charging calculations, described in detail elsewhere,<sup>11</sup> are performed anew for each thickness considered; the results will be plotted as a function of the top oxide thickness (a measure of the deposition time).

### III. SIMULATION RESULTS

#### A. Charging mechanism

Charging of each metal line occurs as a result of a complex balance between tunneling currents through the oxide at the top and the sidewalls, surface currents along the sidewall and the bottom surface, and electron tunneling through the gate oxide from the substrate. Figure 3 illustrates how current balance is accomplished for the two oxide growth models considered. The example applies to the simpler case when the top oxide is just thick enough to prevent tunneling currents to or from the top surface. The directionality difference between ions and electrons as they cross the sheath results in differential charging of the pattern.<sup>1</sup> Electron shading leads to a negative charge at the upper sidewalls, while the directional ions charge positively the bottom surface of the trench. The combination of a negative potential at the upper sidewall with a positive potential at the trench bottom causes deflection of the less energetic ions towards the sidewall; as a result, the lower part of the sidewall charges up positively as well. Surface currents ensure that no surface potential gradients larger than a threshold value exist.<sup>14</sup> However, large electric fields may exist in the oxide layer, especially near the top and bottom of the sidewalls, where the surface potentials approach extreme values (*vide infra*). Obviously, the oxide field also depends on the metal line potential and the oxide thickness at each point. It is the latter dependence that makes a nonconformal oxide more prone to causing metal line charging and subsequent gate oxide damage, as shown in Fig. 3(a). At steady state, a large positive current flows to the metal line through the sidewall bottom region, where the oxide is thinner. At early stages of oxide

growth, this current is compensated mostly by electron tunneling from the upper sidewall region; the current through the gate oxide is comparatively smaller. As the oxide thickness at the upper sidewalls increases, electron tunneling through that region decreases thereby causing the electron current through the thin gate oxide to increase. For conformal oxide [Fig. 3(b)], the film gets thicker at the same rate along the sidewall, causing a simultaneous decrease in the positive and negative current through the sidewall. Thus, the compensating current through the gate oxide is kept small. As the potential distributions will manifest in the next section, the process of charging is more complicated than what is depicted in Fig. 3; the schematic should serve as a starting point to understand the charging dynamics.

### B. Conformal versus nonconformal oxide deposition

The steady state charging potential distribution around each metal line reveals the perturbation in the local ion dynamics occurring as a result of surface charging. Gradients on this potential surface are a measure of the electric field that influences ion motion. Figure 4 and Fig. 5 illustrate such distributions for the nonconformal and conformal oxide deposition cases, respectively, assuming a threshold for surface charge dissipation of 1.0 MV/cm. For nonconformal step coverage, when the film thickness on the top surface is 3.0 nm [Fig. 4(a)], the potential of the line is positive at 2.0 V. This potential develops as a result of a complex balance between tunneling and surface currents, as explained in the preceding section. Note the negative potential (dips) at the upper sidewalls and the positive potential at the lower part of the sidewalls. The combination of ion trajectory bending with the maximum electron shading near the sidewall foot result in a potential maximum of 7.0 V at that location. When the top oxide thickness is increased to 7.5 nm [Fig. 4(b)], the metal line potential increases to 4.8 V, while the potential maximum near the sidewall foot increases to 8.2 V. Further increase in the top oxide thickness to 15.0 nm [Fig. 4(c)], causes the metal line potential to decrease slightly to 4.4 V, while the potential maximum at the trench bottom increases even more to 9.5 V. We shall see later that the drop in the potential of the metal line is caused by the increase in the oxide thickness at the lower part of the sidewalls which decreases the tunneling current to the metal line.

The behavior of the charging potential distribution for oxide deposition with perfectly conformal step coverage is generally similar (Fig. 5). When increasing the oxide thickness from 3.0 to 7.5 nm, the metal line potential increases only slightly from 2.7 to 3.1 V, respectively, [Figs. 5(a) and 5(b)]. However, further increase of the oxide thickness to 15.0 nm [Fig. 5(c)] causes the line potential to become almost zero ( $\approx 0.1$  V). This result hints towards a significant reduction in tunneling currents through the gate oxide to which the line is connected. The smaller value of the metal line potential for the 7.5 and 15.0 nm oxides, as compared to the nonconformal growth case with the same oxide thickness on the top surface, is justified by the thicker oxide at the lower part of the sidewall (see Fig. 1). Note that the potential distribution in the vicinity of the line does not change sig-

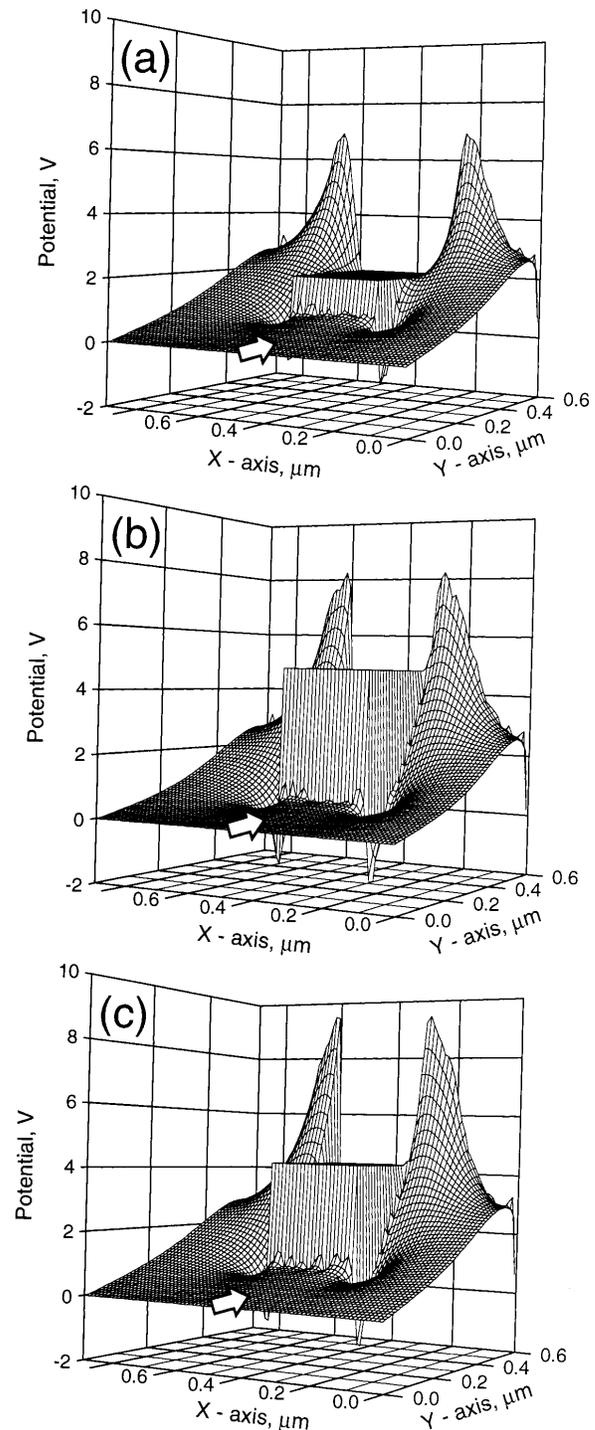


FIG. 4. Three-dimensional charging potential distributions around the metal line for oxide growth with nonconformal step coverage, when the trench aspect ratio equals 0.5. Results are shown for a top oxide thickness of (a) 3.0, (b) 7.5, and (c) 15.0 nm. The sidewall oxide thickness is proportional to the flux of isotropic precursors arriving from the plasma. The arrows show the direction of ions as they approach the potential surface. The axes are defined in Fig. 2.

nificantly; charging along the oxide surface is controlled solely by surface currents for oxide thickness  $\geq 7.5$  nm.

The variation in the potential of the metal line during interlevel oxide deposition is shown in Fig. 6(a) for both conformal and nonconformal step coverage. The results are plotted as a function of top oxide thickness (a measure of

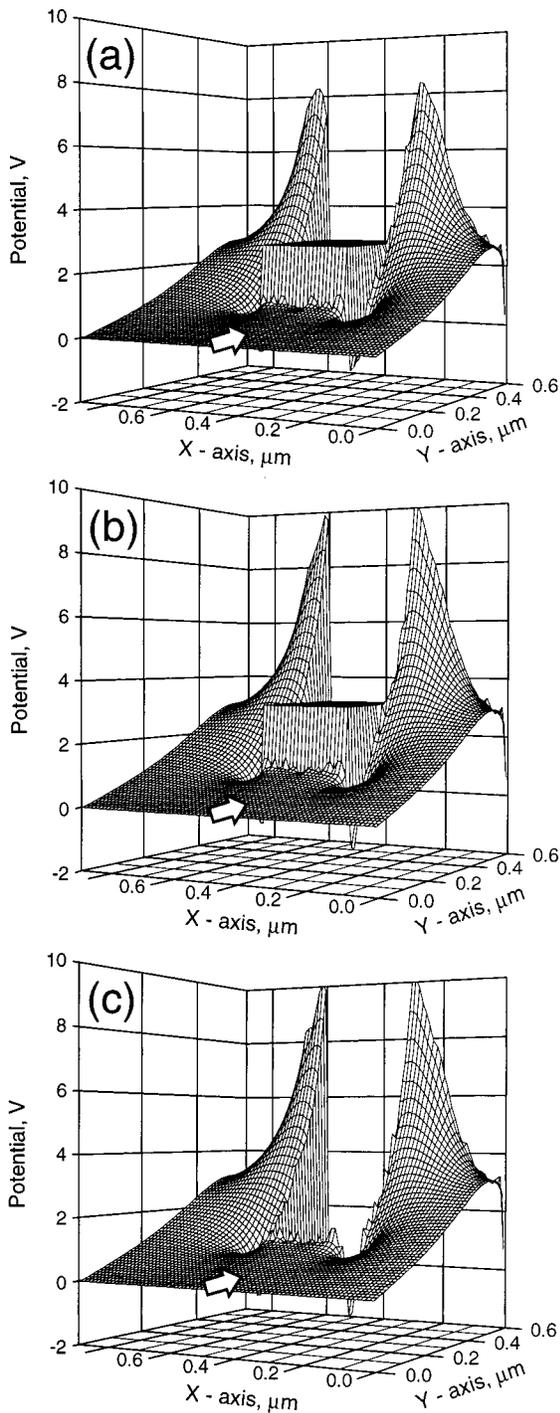


FIG. 5. Three-dimensional charging potential distributions around the metal line for oxide growth with conformal step coverage, when the trench aspect ratio equals 0.5. Results are shown for oxide thickness of (a) 3.0, (b) 7.5, and (c) 15.0 nm. The arrows show the direction of ions as they approach the potential surface. The axes are defined in Fig. 2.

deposition time) so that meaningful comparisons can be made. In both cases, the line potential first increases with oxide thickness, reaches a maximum, and then decreases. However, two important differences exist: (1) the magnitude of the potential maximum is larger in the case of nonconformal oxide; and (2) the potential decreases a lot faster in the case of conformal oxide. These observations can be explained as follows. When the oxide deposited on the metal

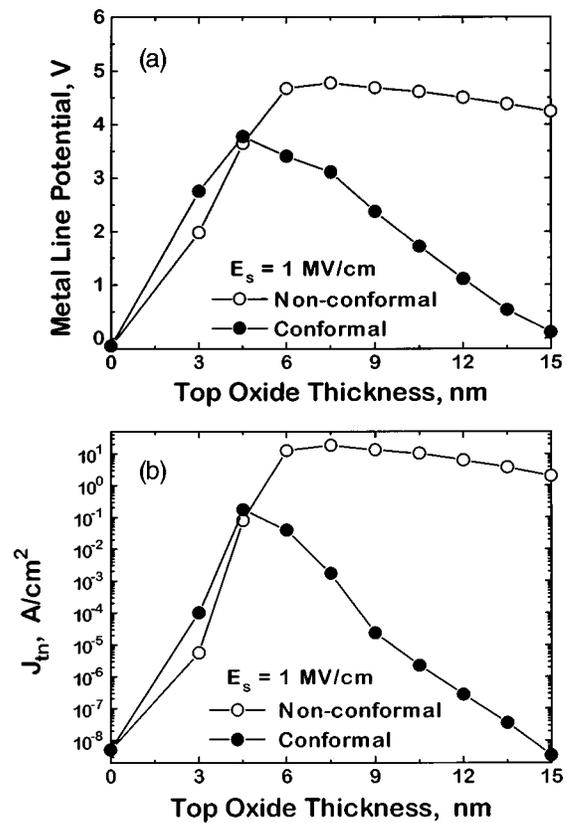


FIG. 6. (a) Charging potential of the metal line and (b) tunneling current density through the underlying gate oxide, as a function of the top oxide thickness (a measure of deposition time) for conformal and nonconformal oxide growth.

surfaces is very thin, tunneling currents flow readily from all sides maintaining a low line potential. As the oxide thickness increases, tunneling becomes more difficult requiring larger potential differences to commence. Such differences build up at the lower part of the sidewall (positive potential) because electron shading prevents neutralization; the top surface is readily accessible by electrons which help maintain a low potential there. Thus, tunneling can still take place from the sidewalls but not from the top surface; as a result, the metal line potential increases until enough electrons are supplied from the substrate to establish current balance to the metal line. In nonconformal deposition, the oxide film is thinner at the lower part of the sidewalls, permitting larger tunneling currents to the metal line, which cause the line potential to increase until electron tunneling from the substrate forces a new dynamic current balance. Since the oxide deposition rate is smaller at the lower part of the sidewalls, tunneling current flow is prolonged; thus, the metal line potential will decrease much slower than when the oxide is growing conformally.

Since the tunneling current through the 3.0 nm gate oxide depends exponentially on the metal line voltage, these observations suggest that the probability for oxide degradation due to large tunneling currents sustained over a longer period of time will be dramatically increased in the nonuniform oxide. The steady state tunneling current ( $J_{tm}$ ) through the 3.0 nm gate oxide is plotted in Fig. 6(b) as a function of the top oxide thickness. Not only are the tunneling currents

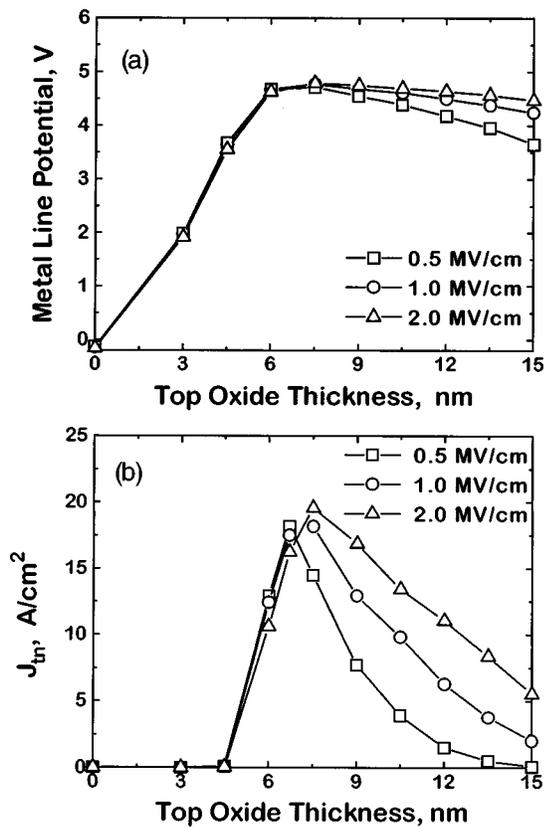


FIG. 7. (a) Charging potential of the metal line and (b) tunneling current density through the underlying gate oxide, as a function of the top oxide thickness for three values of the threshold for surface charge dissipation, as indicated. Results are shown only for nonconformal oxide growth.

larger for the nonconformal deposition, but they also reach values suggestive of catastrophic failure, e.g., 18 A/cm<sup>2</sup> for antenna ratio of 20 000:1 when the top oxide is 7.5 nm thick! Moreover, the tunneling current decreases very slowly for thicker oxides, an indication that cumulative damage will be severe. Remarkably, when the oxide is growing conformally, the calculated peak tunneling current is orders of magnitude smaller at 0.04 A/cm<sup>2</sup>, and decreases exponentially for thicker oxides; thus, the reduction in charging damage should be impressive. These results reveal the importance of achieving conformal step coverage in the initial stages of the deposition.

### C. The role of surface charge dissipation

The dielectric quality of the deposited oxide influences the ability to sustain electric fields along the surface and, thus, charge build up and dissipation. If surface discharging contributes to charge dissipation, it may be influenced by light (UV photons, x-rays) irradiation and/or surface adsorbates,<sup>15</sup> which depend on plasma parameters, chamber condition, and feedstock. This dependence may account for variability in charging damage from run-to-run or in otherwise identical tools.<sup>8</sup> Surface charge dissipation has been modeled as a process requiring a threshold electric field ( $\tilde{E}_s$ ) to commence;<sup>14</sup> a surface electric field larger than threshold initiates surface currents that flow readily until there are no more surface potential gradients exceeding  $\tilde{E}_s$  anywhere

along the surface. Figure 7 illustrates the influence of  $\tilde{E}_s$  on the charging potential of the metal line and on the resulting tunneling current through the 3.0 nm gate oxide. Only the case with nonconformal step coverage is discussed here. When the oxide is thin ( $\leq 7.5$  nm on the top surface), no effect is observed, as manifested by the coalescence of the potential curves in Fig. 7(a); tunneling dominates and prevents the surface electric fields from reaching the threshold value. As the oxide gets thicker, surface potentials increase; when the surface electric field exceeds  $\tilde{E}_s$ , surface currents begin to flow. Since surface potentials are thus kept in check, tunneling currents to the metal line and the resulting potential both decrease. The smaller the value of  $\tilde{E}_s$ , the larger the drop in the charging potential of the metal line [Fig. 7(a)]. Calculation of the tunneling current through the 3.0 nm gate oxide corroborates this interpretation. As illustrated in Fig. 7(b), the tunneling current is lower for smaller  $\tilde{E}_s$ . Note that the tunneling current decreases much faster with time for more facile surface charge dissipation. This observation implies a lower cumulative damage for smaller  $\tilde{E}_s$  and suggests a strategy for decreasing charging damage. Remarkably, the dramatic change in the value of  $\tilde{E}_s$  from 2.0 to 0.5 MV/cm does not change significantly the peak tunneling current. This result increases our confidence in the simulation: despite the lack of measurements of charge dissipation on the evolving oxide surface, its influence on charging damage during ILD deposition can be estimated.

### D. Aspect ratio dependence

Aspect ratios are increasing continuously in the quest for denser packing of logic devices. In plasma etching, charging damage worsens considerably at larger aspect ratios as a result of increased electron shading.<sup>17</sup> In plasma-assisted ILD deposition, such dependence has not yet been documented, probably because of the relatively low aspect ratios used on the various metal levels. The uniformity of the deposited dielectric film generally degrades with aspect ratio as neutral shading of the trench bottoms and sidewalls increases. More time will be required to increase the oxide thickness at the lower part of the sidewalls to the point when tunneling currents become insignificant. However, whether charging damage will worsen depends on both the magnitude and duration of the current through the gate oxide.

Charging calculations for a trench aspect ratio of 1.0 have been performed to evaluate the tunneling current and the concomitant probability for damage. All plasma conditions and other microstructure parameters have been kept unchanged;  $\tilde{E}_s$  has been set equal to 1.0 MV/cm. Neutral-flux-limited oxide growth was assumed to simulate a worst-case scenario. Figure 8 compares the oxide thickness distribution along the sidewall for aspect ratio of 1.0 to that for 0.5, normalized to the same top oxide thickness (arbitrarily chosen to make the point). Clearly, the oxide layer at the lower part of the sidewall is significantly thinner for the higher aspect ratio case. Three-dimensional charging poten-

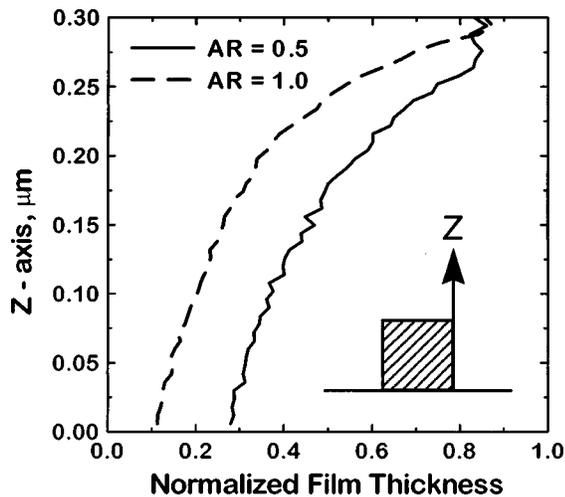


FIG. 8. Film thickness distribution along the sidewall of the metal line for nonconformal oxide growth; the two cases shown correspond to trench aspect ratios of 0.5 and 1.0. The distributions are compared after grown to the same film thickness at the top metal surface, which thickness is used as the normalization constant.

tial distributions around the metal line, illustrated in Fig. 9, show two important differences when compared to the nonconformal deposition case for aspect ratio=0.5 (see Fig. 4): (1) the potential in the trench center is considerably larger, and (2) the metal line potential increases when the top oxide thickness is changed from 7.5 to 15.0 nm. The first observation is consistent with increased electron shading at the larger aspect ratio. The ion and electron dynamics are such that a larger potential forms along the lower part of the sidewalls, where the oxide is thinner. When plotting the metal line potential as a function of the top oxide thickness in Fig. 10(a), we find that the potential peaks at 12 nm for the larger aspect ratio. The maximum value is now 5.4 V; the increase is significant, given the exponential dependence of the tunneling current through the 3.0 nm gate oxide. Assuming that the gate oxide could preserve its integrity, we calculate a tunneling current density exceeding 100 A/cm<sup>2</sup>! The (hypothetical) dependence of the tunneling current density on top oxide thickness, shown in Fig. 10(b), matches the metal line potential and demonstrates the significant increase in charging damage that is expected to accompany the change in the aspect ratio. The calculated tunneling currents for damage during plasma etching<sup>18,19</sup> pale next to these currents. The results suggest that charging damage may become a problem more serious in HDP chemical vapor deposition than in HDP etching of future generations of devices. The importance of conformal step coverage during the early stages of ILD deposition for reducing charging damage cannot be overemphasized.

IV. DISCUSSION OF A KEY ASSUMPTION

An important factor affecting charging damage through the gate oxide is the quality of the deposited interlayer oxide. We have assumed that the bulk dielectric properties of the interlayer oxide are equivalent to those of perfect thermal oxide, a clear oversimplification. Defects in the oxide could allow bulk conduction at lower surface potentials; then, sub-

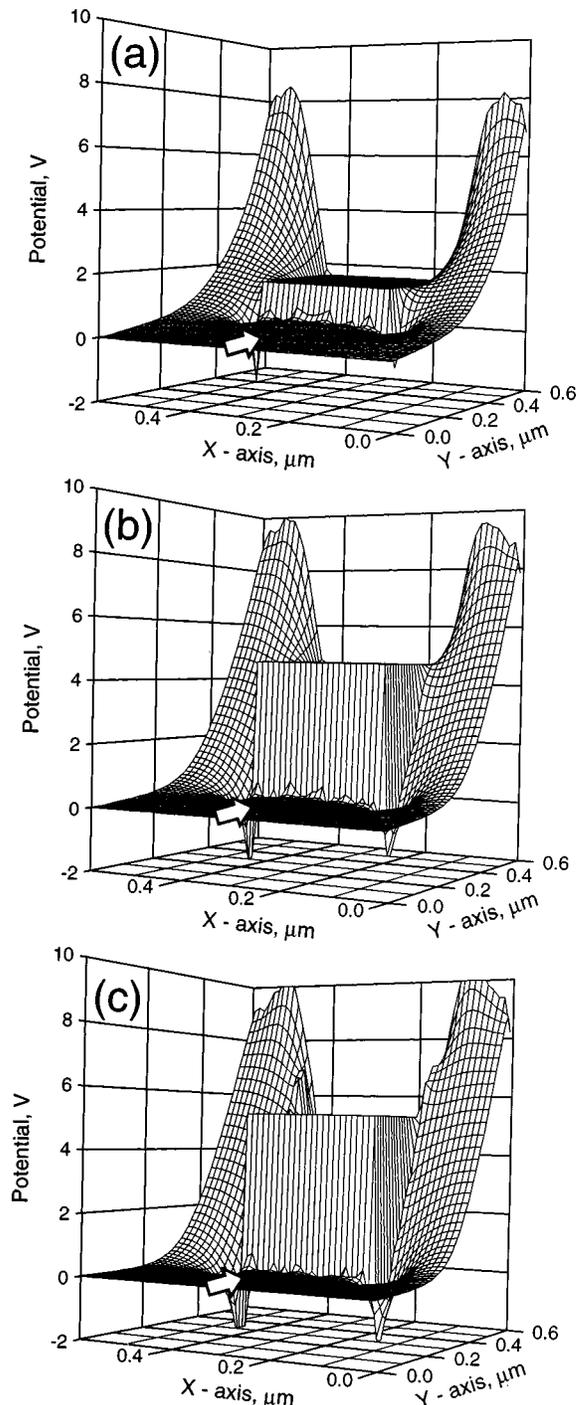


FIG. 9. Three-dimensional charging potential distributions around the metal line for oxide growth with nonconformal step coverage, when the trench aspect ratio equals 1.0. Results are shown for a top oxide thickness of (a) 3.0, (b) 7.5, and (c) 15.0 nm. The sidewall oxide thickness is proportional to the flux of isotropic precursors arriving from the plasma. The arrows show the direction of ions as they approach the potential surface. The axes are defined in Fig. 2.

stantially thicker oxides would be required to observe a behavior similar to the one described. However, even in this case, a nonuniform oxide will result in more charging damage, as the oxide will still be thinner at the lower part of the sidewall near the potential maximum. There is also a possibility that the tunneling currents “burn” a path through the oxide allowing for sustained tunneling currents even as the

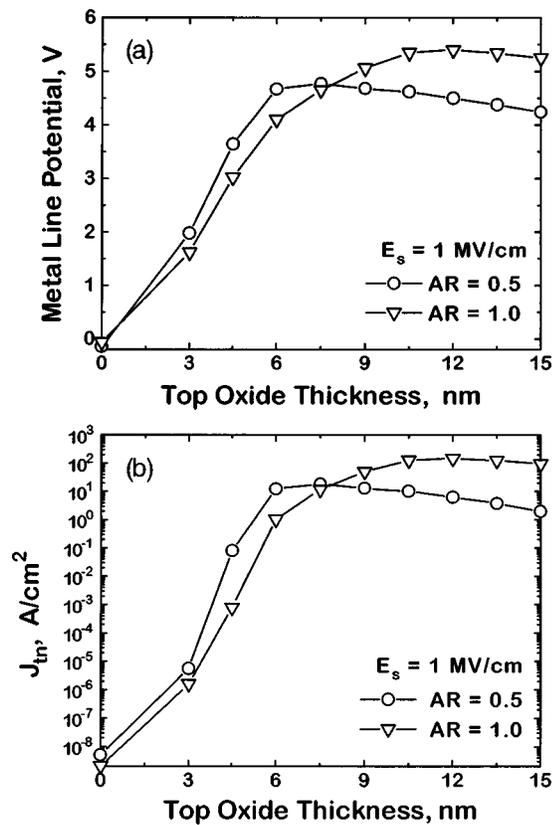


FIG. 10. (a) Charging potential of the metal line and (b) tunneling current density through the underlying gate oxide, as a function of the top oxide thickness for aspect ratio of 1.0 and 0.5. Results are shown only for non-conformal oxide growth.

oxide gets significantly thicker. Then, cumulative damage should increase with oxide thickness, without requiring photoconduction to generate charges in the oxide.<sup>4</sup> The importance of these and other mechanisms will be uncovered only when a detailed description of electron transport through HDP oxides becomes available. Note that bulk conduction would decrease the significance of surface charge dissipation.

## V. SUMMARY AND CONCLUSIONS

In summary, we have presented a theoretical study of charging damage during interlayer oxide deposition in high-density plasmas. The difference between the ion and electron angular distributions at the patterned wafer led to differential charging of the surface of the deposited dielectric film. When the film was thin enough to permit tunneling from the dielectric surface to the metal line, charging of the latter ensued which, in turn, induced electron tunneling from the substrate through the gate oxide. Tunneling currents capable of causing gate oxide degradation and breakdown were calculated for nonconformal film growth; the tunneling current density

peaked when the oxide deposited on the top surface of the metal line was thick enough to block electron tunneling while the thinner oxide along the lower part of the sidewall still allowed tunneling to occur. The results revealed that conformal step coverage during the early stages of oxide deposition is extremely important for reducing charging damage. The increase in trench aspect ratio, as the metal lines are brought closer together for denser integrated circuits, is expected to worsen ILD conformality and charging damage. It appears that a two-step process may be required, where a thin dielectric is first deposited by a nondamaging process (e.g., conventional plasma-enhanced TEOS process or chemical vapor deposition) and is then followed up by dielectric deposition and gap filling in a high-density plasma. Surface charge dissipation was also found to influence charging damage by controlling the magnitude of the charging potentials on the surface of the deposited dielectric. The results suggest that charging from dielectric deposition may become a more serious problem than charging from etching. From this perspective, low- $\kappa$  dielectric materials proposed for ILD oxide replacement must meet film conformality and charge leakage requirements more stringent than previously thought.

## ACKNOWLEDGMENTS

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- <sup>16</sup> The substrate is "grounded" when its potential remains constant despite the current injection. This situation occurs when large "patches" of substrate are directly (or through a thin oxide) exposed to the plasma, e.g., at wafer edges, at scribe lines (separating dyes), or at open areas separating dense patterns.
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