CALIFORNIA INSTITUTE OF TECHNOLOGY

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Electrical Engineering Department

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ABSTRACT

Some results are presented for optimum noise performance of transistor input stages when fed from resistive or reactive sources. Standard theory has shown that a common-emitter transistor fed from a resistive source presents a minimum noise figure F_m when the source resistance has a certain value R_{gm} in the order of $1k\Omega$. In this paper, expressions are developed for minimum noise figure and optimum source resistance in the presence of base bias resistors, emitter degeneration resistance, and various kinds of feedback. Results are in terms of F_m and R_{gm} only, and do not contain other functions of the transistor internal noise sources. It is shown that the minimum noise figure is never less than F_m, but the optimum source resistance can be either greater or less than R_{gm}.

In the case of reactive sources, noise figure is meaningless and the quantity of interest is signal-to-noise ratio over the passband. It is shown that for an inductive source, such as a magnetic tape head, there is a maximum signal-to-noise ratio obtainable with an optimum source inductance, and that a Figure of Merit can be assigned to the source which is independent of its inductance.

Experimental results presented for both resistive and inductive sources show good agreement with the theoretical predictions.

I. Introduction

The noise performance of any electronic circuit, whether measured in terms of noise figure or signal-to-noise ratio, is dependent on two classes of properties: first, the physical sources of noise within the circuit components, and second, the way in which the components are interconnected. This paper is concerned with the second of these, and in particular, with the effects on the overall noise performance of various circuit arrangements of transistors and passive elements with given noise properties.

It has been shown by Bargellini and Herscher[1] that a transistor fed from a resistive source exhibits a noise figure F which is a function of the transistor internal parameters and noise sources and of the external signal source resistance R_g. It was also shown that the noise figure exhibits a minimum value F_m when the source resistance has an optimum value R_{gm} in the order of $1k\Omega$, and that the values of F_m and R_{gm} are essentially the same whether the transistor is in CE, CB, or CC connection.

It will be shown in the following work that the noise figure of a circuit containing a CE transistor and a resistive signal source exhibits a minimum noise figure F_m' for an optimum source resistance R_{gm}' in the presence of bias resistors, emitter degeneration resistors, and feedback. Expressions for F_m' and R_{gm}' are presented in terms of F_m and R_{gm} as defined above. It will be shown that F_m' is always equal to or greater than F_m, and that R_{gm}' may be either greater than or less than R_{gm}. However, it is easy to design circuits in which F_m' exceeds F_m by only a small amount.

In many practical applications the signal source feeding a transistor amplifier is not purely resistive. In these circumstances the noise performance of the entire circuit is more conveniently expressed in terms of signal-to-noise ratio at the output rather than in terms of noise figure. Indeed,

noise figure becomes meaningless if the signal source is purely reactive, a condition approximated in magnetic tape heads. It is obvious that the noise performance in such cases is intimately connected not only with the properties of the transistor and associated circuitry, but also with the properties of the signal source or transducer.

Since the design of transistor amplifiers to be fed from magnetic tape heads or other inductive sources is of some practical importance, it is of interest to inquire whether an optimum source inductance exists which would maximize the output signal-to-noise ratio of the whole circuit. It will be shown in the following work that under certain conditions an optimum source inductance does in fact exist, and expressions for this quantity and for the maximum attainable signal-to-noise ratio will be given. These expressions are in a convenient form for practical use, since they are in terms of quantities easily measurable or calculable from the noise properties of the first-stage transistor, the overall gain versus frequency characteristic, and certain circuit parameters concerned with the biasing arrangements of the first-stage transistor. It will further be shown that a Figure of Merit can be ascribed to an inductive signal source, to which the signal-to-noise ratio of the complete amplifier is proportional. Experimental results presented for both resistive and inductive sources show good agreement with the theoretical predictions.

II. Amplifier Noise Figures with Resistive Sources

The equivalent circuit to be used to represent a noisy transistor is shown in Fig. 1. This representation is stripped to the bare essentials since the present concern is with the circuit properties of the transistor and not with its internal performance. The simpler the equivalent circuit of the transistor, the simpler and more illuminating will be the desired results, and the justification for such simplicity will be found in the

validity of the results for practical purposes. Thus in the tee equivalent circuit of Fig. 1, the emitter and base resistances are assumed negligibly small, the collector resistance negligibly large, and frequencies of interest are assumed to be such that collector capacitance and variations of the current gain α may be ignored. The internal mechanisms of noise generation are here of no interest, and the simplest valid representation of the noise is by means of an emitter noise voltage generator v_{ne} and a collector noise current generator i_{nc}. The polarities shown in Fig. 1 are of course arbitrary, since ultimately only noise powers are of interest. The quantities v_{ne} and i_{nc} are defined as rms noise voltage and current in 1 cps bandwidth, and in the present work are considered to be the same at all frequencies; thus "1/f noise" is neglected. However, this limitation is not necessary, and the principles of most of the calculations described herein are equally valid if this restriction is removed, although the complexity of the results is considerably increased.

For future purposes, it is convenient to suppose that the emitter noise voltage is due to a fictitious "emitter effective noise resistance" R_{ne} defined by $v_{ne}^2 = 4kTR_{ne}$, where k is Boltzmann's constant and T is the absolute temperature.

If a noisy transistor is connected as a CE amplifier to a signal source of internal resistance R_g, and thermal noise voltage $v_{ng} = (4kTR_g)^{1/2}$ in 1 cps bandwidth, as in Fig. 1, it is easily shown that the noise figure F of the circuit is given by

$$F = 1 + \frac{v_{ne}^2 + R_g^2 i_{nc}^2/\alpha^2}{4kTR_g} \qquad (1)$$

The noise figure is therefore a function of the generator resistance R_g, and exhibits a minimum value F_m when the generator resistance has an

optimum value R_{gm}, where

$$R_{gm} = \frac{\alpha v_{ne}}{i_{nc}} \tag{2}$$

$$F_m = 1 + \frac{2v_{ne}^2}{4kTR_{gm}} = 1 + \frac{2R_{ne}}{R_{gm}} \tag{3}$$

The above equations may be obtained from the work of Bargellini and Herscher[1] by appropriate simplification.

Figure 2 shows the general form of the variation of the noise figure F as a function of the generator resistance R_g for the circuit of Fig. 1. For a low-noise transistor, F_m is of the order of 2.5 (4 db) and R_{gm} in the region of 1kΩ. These two quantities are readily measured, and from them the parameters v_{ne}, i_{nc}, and R_{ne} can be determined from Eqs. (2) and (3). From the applications point of view, the circuit measurements are more appropriate than the internal generators v_{ne} and i_{nc}, and hence in the following work results will be expressed in terms of F_m and R_{gm}.

Practical transistor amplifiers are rarely as simple as that shown in Fig. 1. It is, therefore, of interest to consider the effects on noise performance of typical associated circuitry. Figure 3 shows the equivalent circuit of a generalized transistor amplifier input stage which contains most of the features likely to be encountered in a realistic amplifier: the input signal voltage E_g may arise in a reactive source of impedance $Z_g = R_g + jX_g$ and with thermal noise $v_{ng} = (4kTR_g)^{1/2}$; the resistor R_1 and its thermal noise $v_{n1} = (4kTR_1)^{1/2}$ accounts for any biasing arrangement to the base of the first-stage transistor, such as the usual potential divider; the resistor R_2 and its thermal noise $v_{n2} = (4kTR_2)^{1/2}$ accounts for any emitter degeneration caused by un-bypassed emitter resistance; and

the generators U_a, U_b, and U_c account, respectively, for bias resistor bootstrapping, feedback to the base, and feedback to the emitter, all proportional to the complete amplifier output voltage E. It is assumed that all noise sources following the first-stage transistor may be neglected.

Let it first be supposed that the signal source is purely resistive, thus $X_g = 0$. The noise figure F' of the complete amplifier may be computed with greater complexity than difficulty, and is found to show a minimum value F_m' when the source resistance has an optimum value R_{gm}'. These quantities may be expressed in terms of the corresponding quantities F_m and R_{gm} for the simple CE transistor (defined above) as

$$\frac{R_{gm}'}{R_{gm}} = \left[\frac{1 + (R_2/R_{gm})^2 + R_2/R_{ne}}{(1 + R_2/R_1)^2 + (R_{gm}/R_1)^2 + (1 + R_2/R_1)R_{gm}^2/R_1R_{ne})} \right]^{1/2} \qquad (4)$$

$$\frac{F_m' - 1}{F_m - 1} = \frac{R_2}{R_{gm}} + R_{gm}\left(1 + \frac{R_2^2}{R_{gm}^2} + \frac{R_2}{R_{ne}} \right)\left(\frac{1}{R_1} + \frac{1}{R_{gm}'} \right) \qquad (5)$$

Although interpretation of the above equations is somewhat laborious, one conclusion is immediately obvious: neither R_{gm}' nor F_m' depends on any of the feedback generators U. The importance of this result may be emphasized by stating it in other words: the input impedance and the gain characteristic of the amplifier are strongly dependent on any feedback, but the minimum noise figure attainable and the optimum source resistance to provide it are unaltered by feedback and remain the same as when no feedback is applied.

It is seen from Eqs. (4) and (5) that the only elements causing R_{gm}' and F_m' to differ from R_{gm} and F_m are the resistors R_1 and R_2. In order to obtain a clearer understanding of their effects, it is convenient to consider the modifications introduced by R_1 and R_2 separately. If, first, $R_2 = 0$, Eqs. (4) and (5) reduce to

$$\frac{R_{gm}}{R_{gm}'} = \left[1 + \frac{R_{gm}^2}{R_1^2}\left(1 + \frac{R_1}{R_{ne}}\right)\right]^{1/2} \tag{6}$$

$$\frac{F_m' - 1}{F_m - 1} = R_{gm}\left(\frac{1}{R_1} + \frac{1}{R_{gm}'}\right) \tag{7}$$

It is seen from the above results that $R_{gm}' \leqslant R_{gm}$ and $F_m' \geqslant F_m$, that is, the presence of R_1 always increases the minimum noise figure and decreases the optimum source resistance necessary to achieve it.

If, next, $R_1 = \infty$, Eqs. (4) and (5) reduce to

$$\frac{R_{gm}'}{R_{gm}} = \left(1 + \frac{R_2^2}{R_{gm}^2} + \frac{R_2}{R_{ne}}\right)^{1/2} \tag{8}$$

$$\frac{F_m' - 1}{F_m - 1} = \frac{1}{R_{gm}}(R_2 + R_{gm}') \tag{9}$$

from which it is seen that $R_{gm}' \geqslant R_{gm}$ and $F_m' \geqslant F_m$, that is, the presence of R_2 always increases the minimum noise figure and increases the optimum source resistance necessary to achieve it.

The similarity between the pairs of equations (6), (7), and (8), (9) suggests that a single graph with appropriate variables could be drawn for the corresponding equations in each pair. Curve 1 in Fig. 4 shows Eq. (6) or (8) plotted for the special case of a transistor with $F_m = 2$ (3 db) and $R_{gm} = 1\text{k}\Omega$, for which $R_{ne} = 0.5\ \text{k}\Omega$ from Eq. (3). Curve 1 in Fig. 5 shows Eq. (7) or (8), for the same transistor, plotted to show the excess of F_m' over F_m as a function of R_1 or of R_2.

Equations (6) and (8) may be simplified if the thermal noise generated by R_1 and R_2 is neglected. This approximation is equivalent to omitting

the terms in R_{ne} in Eqs. (6) and (8), and is easily shown to be valid if $R_{ne} \gg R_{gm}/2$ or if $F_m \gg 2$ (3 db) which is the same condition. To indicate the error introduced by this approximation, curves 2 in Figs. 4 and 5 show how curves 1 are modified when the terms in R_{ne} are neglected in Eqs. (6) and (8). It is seen that the error is worst when R_{gm}/R_1 or R_2/R_{gm} is equal to 1, and that the maximum error is 30% in R_{gm}/R_1 or R_2/R_{gm}, and 0.7 db in $(F_m' - F_m)$. It should be noted that curves 1 and 2 in both Figs. 4 and 5 are for $F_m = 2$ (3 db) which hardly satisfies the validity condition for the approximation, and even so the error is tolerable. It may be concluded, therefore, that in most practical cases the thermal noise due to R_1 and R_2 may be neglected in computing the noise figure of the circuit, in which case Eqs. (6) and (8) reduce to

$$\frac{R_{gm}}{R_{gm}'} = \left(1 + \frac{R_{gm}^2}{R_1^2}\right)^{1/2} \tag{10}$$

for $R_2 = 0$, and

$$\frac{R_{gm}'}{R_{gm}} = \left(1 + \frac{R_2^2}{R_{gm}^2}\right)^{1/2} \tag{11}$$

for $R_1 = \infty$. A further advantage of making the approximation is that curve 2 in Fig. 4 is now independent of F_m and R_{gm}, and is hence a universal curve for all transistors, and curve 2 in Fig. 5 is independent of R_{gm}.

Some further conclusions may be drawn from Figs. 4 and 5: if $R_1 \gg R_{gm}$ or if $R_2 \ll R_{gm}$, R_{gm}' is little different from R_{gm}, and F_m' is little greater than F_m. Since R_{gm} is usually of the order of 1kΩ, these conditions are usually realized in practice and the minimum noise figure is not much greater than the minimum possible. If $R_1 \ll R_{gm}$ or if $R_2 \gg R_{gm}$,

R_{gm}' tends to R_1 or to R_2 as appropriate, and the minimum noise figure is appreciably greater than the minimum possible. Further, as shown in curves 3 and 4 of Fig. 5, the greater the value of F_m for the transistor, the greater is the increase above F_m in the noise figure of the complete circuit.

To check the validity of the results described, experimental measurements of the 1 kc noise figure were made for various values of R_1 and R_2 and compared with the predicted values. The procedure was as follows. Measurements of the noise figure F of a single CE transistor as shown in Fig. 1 were made as a function of source resistance R_g. These points should satisfy the relation

$$F = F_m + \frac{(F_m - 1)}{2} \frac{(R_g - R_{gm})^2}{R_g R_{gm}} \tag{12}$$

The line shown in Fig. 6 (for $R_1 = \infty$) or in Fig. 7 (for $R_2 = 0$) is the best fit with the experimental points which also satisfies Eq. (12). From this "best fit" line, the values of F_m and R_{gm} for the experimental transistor at the particular operating point chosen were found to be $F_m = 5.62$ (7.5 db) and $R_{gm} = 0.63$ kΩ.

In the presence of R_1, the noise figure F' as a function of source resistance R_g should satisfy the relation

$$F' = F_m' + \frac{(F_m' - 1)}{2(1 + R_{gm}'/R_1)} \frac{(R_g - R_{gm}')^2}{R_g R_{gm}'} \tag{13}$$

where F_m' and R_{gm}' are given by Eqs. (7) and (10) respectively. Figure 6 shows Eq. (13) plotted for three values of R_1, and it is seen that the experimental points agree quite well with the predicted curves. It should be noted that thermal noise in R_1 was neglected in computing the curves,

and the agreement between the measured and predicted results is further evidence of the validity of the approximation.

In the presence of R_2, the noise figure F' as a function of source resistance R_g should satisfy the relation

$$F' = F_m' + \frac{(F_m' - 1)}{2(1 + R_2/R_{gm}')} \frac{(R_g - R_{gm}')^2}{R_g R_{gm}'} \qquad (14)$$

where F_m' and R_{gm}' are given by Eqs. (9) and (11) respectively. Figure 7 shows Eq. (14) plotted for two values of R_2, and again the agreement between measured and predicted results is good even though thermal noise in R_2 is neglected.

III. Amplifier Signal-to-Noise Ratios with Reactive Sources

If the signal source impedance contains a reactive component, the spot noise figure of the complete amplifier will vary with frequency. Indeed, if the source is purely reactive, noise figure becomes meaningless. In such cases a more useful measure of noise performance is the signal-to-noise ratio S_0 at the amplifier output. More precisely, S_0 may be defined as the ratio of the signal power in the load to the total noise power in the load. In general, the signal power in the load will depend on the chosen frequency f_0, the source voltage at f_0, and the overall amplifier gain at f_0. The total noise power in the load will depend on the noise properties of the first-stage transistor and associated circuit elements, any noise from the signal source such as its own resistive thermal noise and noise brought into the system along with the signal, and on the overall gain versus frequency response of the complete amplifier.

The equivalent circuit of the generalized amplifier shown in Fig. 3 will again provide a suitable foundation for discussion, except that the

complex character of the source impedance $Z_g = R_g + jX_g$ will be retained, and in accordance with the results of the previous section the thermal noise generators v_{n1} and v_{n2} will be omitted. An input transformer may also be included in which case E_g, v_{ng}, and Z_g are source parameters referred to the secondary. The output signal-to-noise ratio S_0 at a frequency f_0 may be shown to be

$$S_0 = \frac{\left(\frac{2E_{g0}^2}{4kTR_{gm}(F_m - 1)}\right)}{\int_0^\infty \left[\frac{R_g}{R_{ne}} + \left|1 + \frac{Z_g}{R_1}\right|^2 + \frac{1}{R_{gm}^2}\left|Z_g + R_2\left(1 + \frac{Z_g}{R_1}\right)\right|^2\right]\left|\frac{G(f)}{G(f_0)}\right|^2 df} \qquad (15)$$

where E_{g0} is the open-circuit source voltage at frequency f_0, $G(f) = E/E_g$ is the overall voltage gain, and R_{gm}, F_m, and R_{ne} are the noise parameters of the first-stage transistor as previously defined. It is assumed in the above result that there is no noise in the signal source other than that due to its internal resistance R_g, and, as mentioned earlier, that the transistor noise generators v_{ne} and i_{nc} are independent of frequency. If desired, 1/f frequency dependence of one or both of these generators could be introduced with considerably greater complexity in the result.

It is to be noted from the above result that the output signal-to-noise ratio is independent of the amplifier input impedance and of any feedback except insofar as these parameters influence the gain characteristic $G(f)/G(f_0)$.

A special case of considerable practical interest occurs when the signal source is essentially a pure inductance, that is, $R_g \to 0$ and $X_g \to 2\pi f L_g$. A typical source of this type would be a magnetic tape reproduce head or a magnetic phonograph pickup. Under this condition, Eq. (15) may be written

$$S_0 = \frac{\left(\frac{2M}{F_m - 1}\right) 2\pi L_g R_{gm}}{R_{gm}^2 C_1^2 A_1^2 + (2\pi L_g)^2 C_2^2 A_2^2} \tag{16}$$

in which M is a "source parameter" defined as

$$M = \frac{E_{g0}^2}{8\pi k T f_0^2 L_g} \tag{17}$$

A_1 and A_2 are "gain parameters" defined by

$$A_1 = \frac{1}{f_0}\left(\int_0^\infty \left|\frac{G(f)}{G(f_0)}\right|^2 df\right)^{1/2} \tag{18}$$

$$A_2 = \frac{1}{f_0}\left(\int_0^\infty \left|\frac{G(f)}{G(f_0)}\right|^2 f^2 df\right)^{1/2} \tag{19}$$

and C_1 and C_2 are "circuit parameters" defined by

$$C_1 = \left(1 + \frac{R_2^2}{R_{gm}^2}\right)^{1/2} \tag{20}$$

$$C_2 = \left[\left(1 + \frac{R_2}{R_1}\right)^2 + \frac{R_{gm}^2}{R_1^2}\right]^{1/2} \tag{21}$$

Some properties of the "source parameter" M are of interest. Consider a magnetic tape head containing N turns of wire of negligible resistance. If the head is stimulated by a tape recorded with constant flux amplitude at all frequencies $\phi = \Phi \sin 2\pi ft$, then the open-circuit voltage of the head will be proportional to the frequency and to the number of

turns:

$$E_g \sim N\frac{d\phi}{dt} \sim Nf \tag{22}$$

However, the inductance of the head is proportional to the square of the number of turns:

$$L_g \sim N^2 \tag{23}$$

The above relations assume no leakage flux and that the head gap is small compared to the recorded wavelength. It follows from Eqs. (22) and (23) that the quantity E_g^2/f^2L_g is independent of frequency and the number of turns, and hence of the inductance, if the tape is recorded with constant flux amplitude. Similarly, for a phonograph pickup the same remarks apply if the disk recording characteristic is constant amplitude at all frequencies. Even if the recording characteristic is not constant amplitude, E_g^2/f^2L is still independent of the inductance though not of frequency.

It follows, therefore, that the "source parameter" M may be rewritten

$$M = \frac{E_g^2}{8\pi kTf^2L_g} \tag{24}$$

and may be rechristened a Figure of Merit for the source which is independent of its inductance and also, in certain circumstances, of frequency. A definition of the Figure of Merit in physical terms may be expressed as follows:

$$M = \frac{2(\text{max. available signal energy in 1 cycle})}{\text{thermal energy in 1 cycle}}$$

The source Figure of Merit is a dimensionless number which may for convenience be expressed in db.

Attention may now be returned to Eq. (16). The output signal-to-noise ratio S_0 is seen to be a function of the source inductance L_g, and since it has been shown that M is independent of L_g it follows that S_0 exhibits a maximum value S_{0m} when the source inductance has an optimum value L_{gm}, where, from Eq. (16)

$$L_{gm} = \frac{R_{gm}}{2\pi} \frac{A_1 C_1}{A_2 C_2} \tag{25}$$

$$S_{0m} = \frac{M}{(F_m - 1) A_1 A_2 C_1 C_2} \tag{26}$$

The optimum source inductance L_{gm} is, of course, independent of the frequency f_0 at which S_0 is determined, while S_0 is not, in general, independent of f_0.

It has thus been shown that an optimum source inductance exists for which a maximum output signal-to-noise ratio is realized, and expressions for these two quantities have been given in terms of a source Figure of Merit, the first-stage transistor noise parameters F_m and R_{gm}, amplifier overall gain parameters, and circuit parameters containing only the resistors R_1 and R_2 shown in Fig. 3. The results are easily applied to practical design problems to determine the maximum attainable signal-to-noise ratio and the required source inductance. For a given source, it is of course usually more convenient to match the existing source inductance to the optimum value by a transformer than to redesign the transducer.

Some typical figures will help to give insight into the magnitudes involved. Suppose a transistor amplifier is to be designed to provide constant output at all frequencies between $f_1 = 50$ cps and $f_2 = 10$ kc from a

magnetic tape recording. It is desired to find the maximum attainable signal-to-noise ratio and the optimum source inductance given that the first stage transistor has $F_m = 4$ (6 db), $R_{gm} = 1k\Omega$, and that the tape head has an inductance of 3 mh and provides an output of 0.6 mv at 1 kc.

Insertion of the given figures for the tape head into Eq. (24) leads to a value for the Figure of Merit of $M = 1.2 \times 10^9$ (91 db). It remains only to find the "circuit parameters" and the "gain parameters". To take a case worse than would probably occur in practice, suppose that in the circuit of Fig. 3 $R_1 = 5k\Omega$ and $R_2 = 1k\Omega$. Use of Eqs. (20) and (21) leads to $C_1 = 1.41$, $C_2 = 1.22$ (note that $C_1 = C_2 = 1$ if $R_1 = \infty$ and $R_2 = 0$). To find the "gain parameters", the gain characteristic must be determined. Since the tape recording is constant amplitude, the open-circuit output voltage of the head will fall as the frequency rises at 6 db per octave, and since an amplifier output voltage constant with frequency is required, the inverse characteristic must be provided in the amplifier. Hence $|G(f)/G(f_0)|^2 = (f_0/f)^2$, and if for simplicity it is supposed that sharp cutoff occurs at a low frequency f_1 and a high frequency f_2, use of Eqs. (18) and (19) leads to $A_1 = 1/ f_1^{1/2}$, $A_2 = f_2^{1/2}$. With $f_1 = 50$ cps and $f_2 = 10$ kc as given, use of Eqs. (25) and (26) leads to $L_{gm} = 260$ mh, $S_{0m} = 72$ db, where the signal-to-noise ratio is in this case independent of signal frequency chosen because of the output characteristic specified. Thus an output signal-to-noise ratio of 72 db can be realized if the number of turns on the tape head is increased to make its inductance 260 mh, or alternatively if a step-up input transformer of turns ratio $(260/3)^{1/2} = 9.3$ is used with the given head.

IV. Experimental Results for Inductive Source

An experiment was performed to verify the theoretical prediction that a maximum signal-to-noise ratio exists for an optimum value of source inductance. Since the source inductance was to be varied, a high input impedance to the transistor amplifier was desired so that the gain function $|G(f)/G(f_0)|^2$ should not change with source inductance. The signal-to-noise ratio S_0 at 1 kc as a function of source inductance L_g was determined theoretically and experimentally as follows.

A transistor feedback amplifier was constructed with a constant voltage gain between low and high frequency roll-offs of 12 db per octave, the break frequencies being approximately 100 cps and 5 kc. The first stage of the amplifier contained the same transistor, at the same operating point, whose noise characteristics are shown in Figs. 6 and 7. The input impedance was not less than 2MΩ throughout the passband. The resistor R_1 was negligibly large, and R_2 was 1kΩ. Since $R_{gm} = 0.63$kΩ and $F_m = 5.6$ (7.5 db), the circuit parameters can be found from Eqs. (20) and (21) to be $C_1 = 1.88$, $C_2 = 1$. By use of Eqs. (18) and (19) and straight-line approximations to the gain characteristic, the gain parameters may be found analytically to be $A_1 \approx 0.082\ (\text{cps})^{-1/2}$, $A_2 \approx 410\ (\text{cps})^{1/2}$ at $f_0 = 1$kc. Numerical integration of the measured gain characteristic led to more accurate values of $A_1 = 0.076\ (\text{cps})^{-1/2}$, $A_2 = 420\ (\text{cps})^{1/2}$, and it may be noted that the approximate analytical values are quite adequate for practical applications. If an inductive signal source with a Figure of Merit $M = 10^9$ (90 db) at 1 kc is assumed, Eqs. (25) and (26) predict that the amplifier should exhibit a maximum signal-to-noise ratio $S_{0m} = 65.7$ db when the source inductance has an optimum value $L_{gm} = 0.0343$ h.

Experimental measurements of output signal-to-noise ratio were made on the amplifier with a true rms voltmeter. The signal source was a simulated

magnetic tape head consisting of a variable inductance L_g in series with a 1 kc voltage E_g from an oscillator whose magnitude was adjusted to maintain a constant Figure of Merit of 90 db: thus, from Eq. (24), $E_g^2/L_g = 1.03 \times 10^{-4}\ v^2/h$. The results are shown in Fig. 8, in which the solid curve is the predicted 1 kc signal-to-noise ratio as a function of source inductance with $S_{Om} = 65.7$ db and $L_{gm} = 0.0343$ h. The points are the measured values obtained with the dummy inductive source. The agreement between predicted and measured values is quite close.

V. Conclusions

The noise performance of transistor amplifier circuits fed from resistive and reactive sources has been discussed.

For resistive sources, it has been shown that a minimum noise figure exists for an optimum source resistance, that these quantities are independent of any feedback, but dependent on equivalent input shunt resistance and on equivalent emitter degeneration resistance in the first stage CE transistor. The presence of these two resistances increases the minimum noise figure, but the degradation is only slight with resistance values easily achieved in practice.

For inductive sources, such as a magnetic tape head or a magnetic phonograph pickup, it has been shown that a Figure of Merit can be ascribed to the source which is independent of its inductance. It has further been shown that a maximum signal-to-noise ratio is attainable at the amplifier output for an optimum source inductance. Expressions for these two quantities have been given in terms of the source Figure of Merit, first-stage transistor noise properties, circuit parameters and gain parameters. Typical figures and experimental results in close agreement with theory have been presented.

It is to be emphasized that the criteria for best noise performance, whether the source is resistive or reactive, are in no way connected with the criteria for maximum power transfer from the source.

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REFERENCE

1. P. M. Bargellini and M. B. Herscher, "Investigations of noise in audio frequency amplifiers using junction transistors," Proc. IRE., vol. 43, pp. 217-226; February 1955.

FIGURE CAPTIONS

1. Simple equivalent circuit of CE transistor amplifier fed from resistive source.

2. Noise figure F vs. source resistance R_g for the amplifier of Fig. 1.

3. Generalized transistor amplifier fed from reactive source, including input (base) shunt resistance and emitter degeneration resistance with thermal noise, also feedback generators which are functions of amplifier output voltage.

4. Optimum source resistance R_{gm}' as a function of R_1 or R_2. Neglect of thermal noise generated in R_1 and R_2 introduces only small error.

5. Increase in minimum noise figure caused by R_1 or R_2. Neglect of thermal noise generated in R_1 and R_2 introduces only small error.

6. Comparison between predicted and measured noise figure curves as functions of source resistance, for resistive source and $R_2 = 0$. Thermal noise generated in R_1 was neglected in computing the predicted curves.

7. Comparison between predicted and measured noise figure curves as functions of source resistance, for resistive source and $R_1 = \infty$. Thermal noise generated in R_2 was neglected in computing the predicted curves.

8. Comparison between predicted and measured signal-to-noise ratio as functions of source inductance. Source Figure of Merit taken as $M = 10^9$ (90 db).

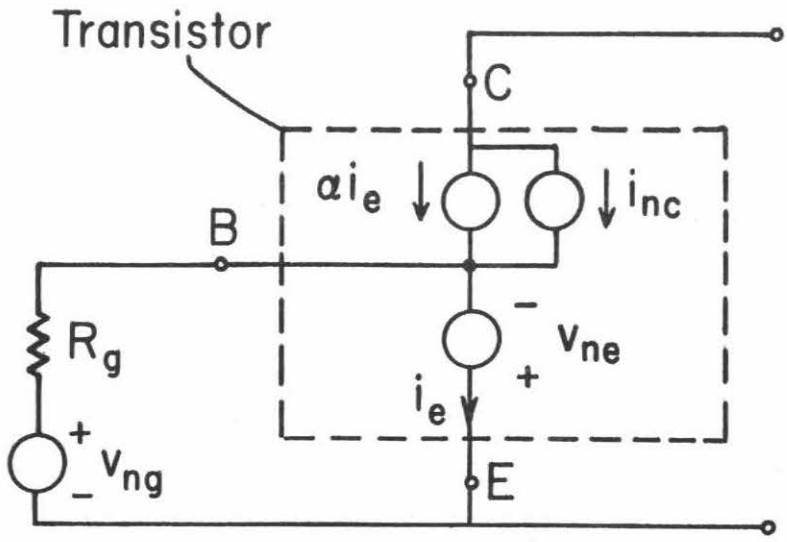

Fig. 1

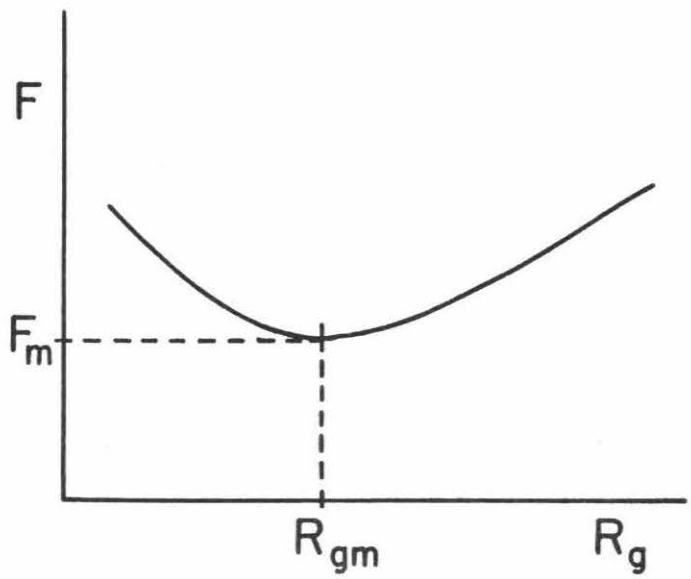

Fig. 2

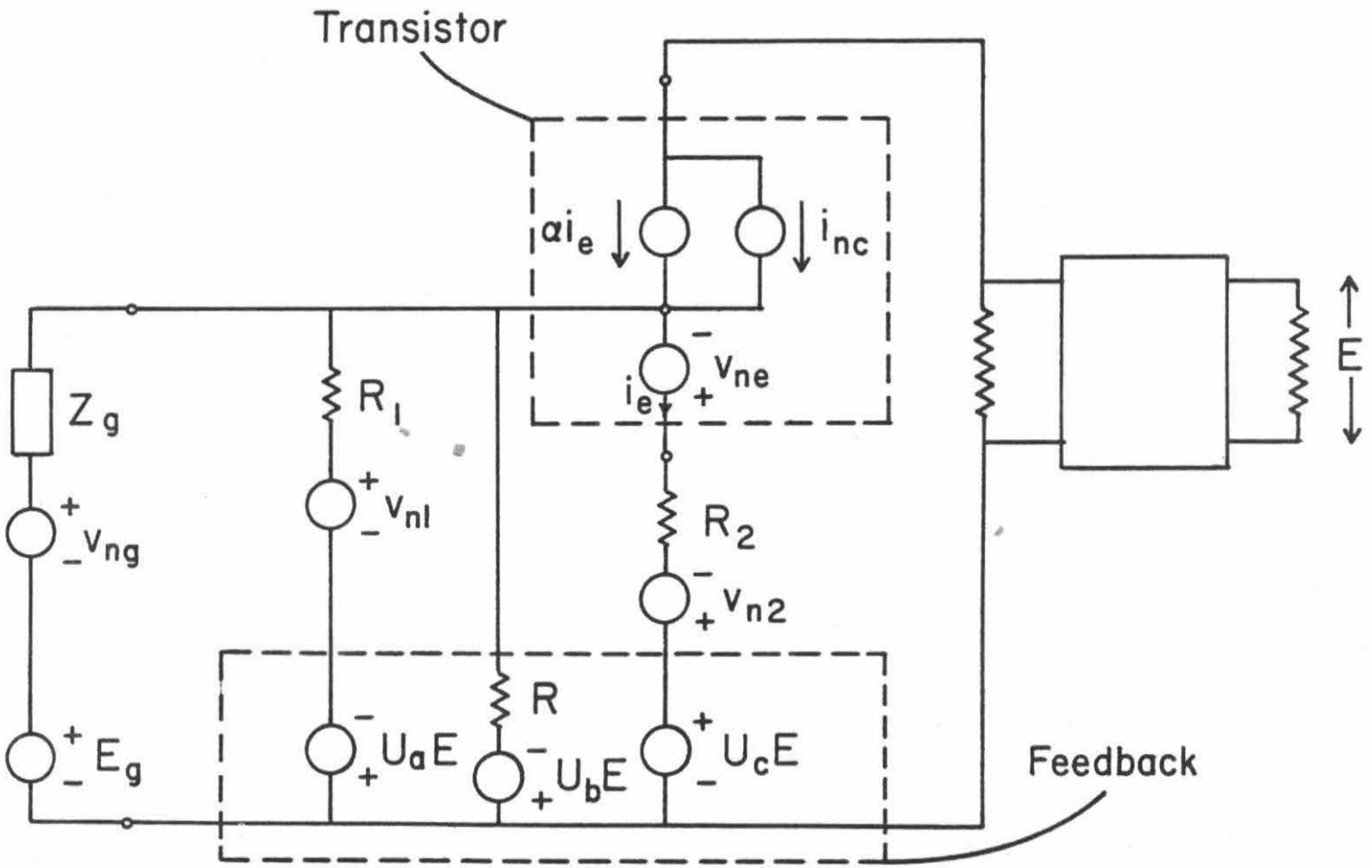
Transistor
αi_e
i_nc
i_e
v_ne
Z_g
R_1
v_nl
v_ng
R_2
v_n2
R
E_g
U_aE
U_bE
U_cE
Feedback
E

Fig. 3

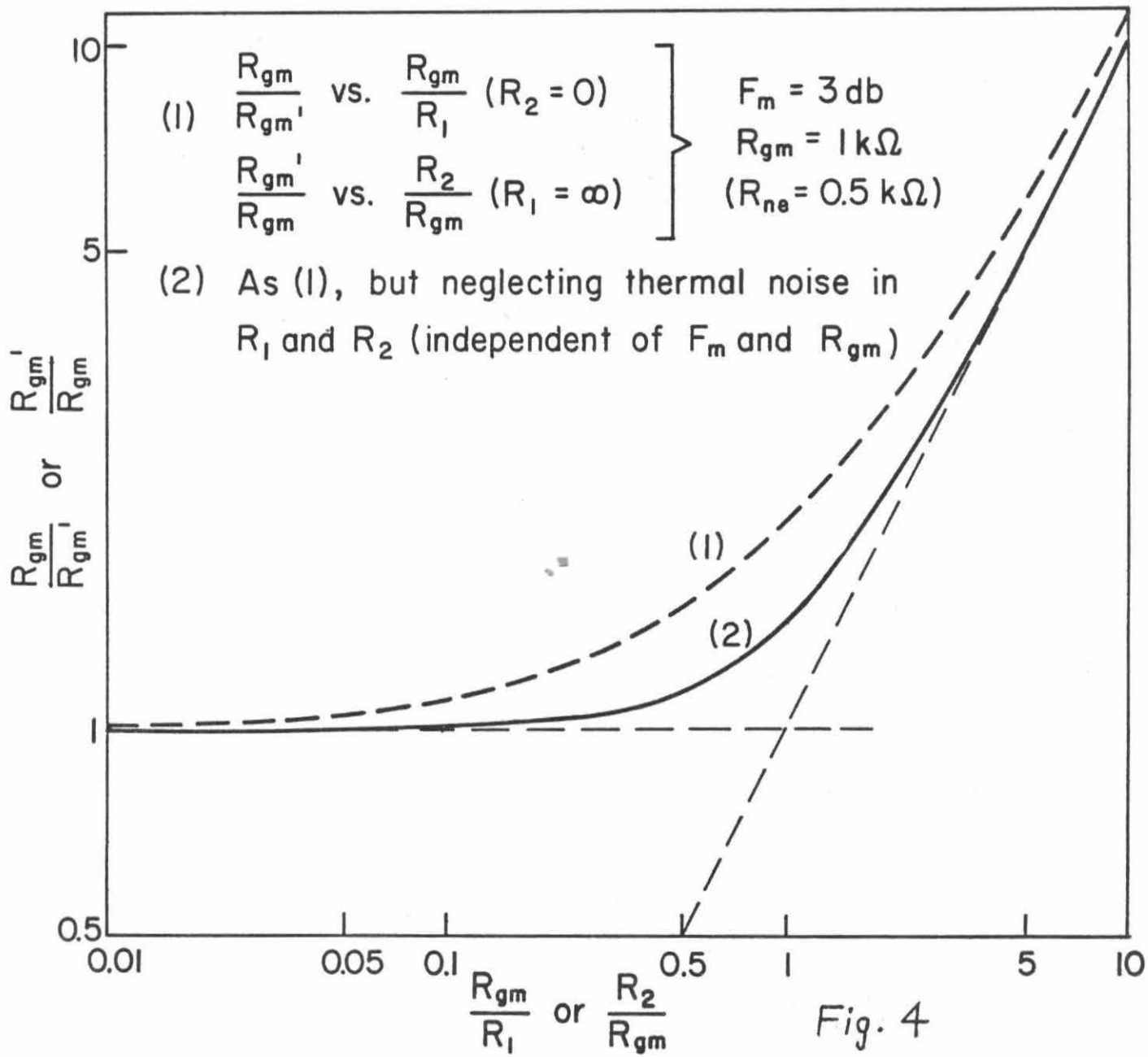
(1) $\frac{R_{gm}}{R_{gm}'}$ vs. $\frac{R_{gm}}{R_1}$ $(R_2 = 0)$
$\frac{R_{gm}'}{R_{gm}}$ vs. $\frac{R_2}{R_{gm}}$ $(R_1 = \infty)$
F_m = 3 db
R_{gm} = 1 kΩ
$(R_{ne}$ = 0.5 kΩ)
(2) As (1), but neglecting thermal noise in R_1 and R_2 (independent of F_m and R_{gm})
(1)
(2)
$\frac{R_{gm}}{R_{gm}'}$ or $\frac{R_{gm}'}{R_{gm}}$
10
5
1
0.5
0.01
0.05
0.1
0.5
1
5
10
$\frac{R_{gm}}{R_1}$ or $\frac{R_2}{R_{gm}}$

Fig. 4

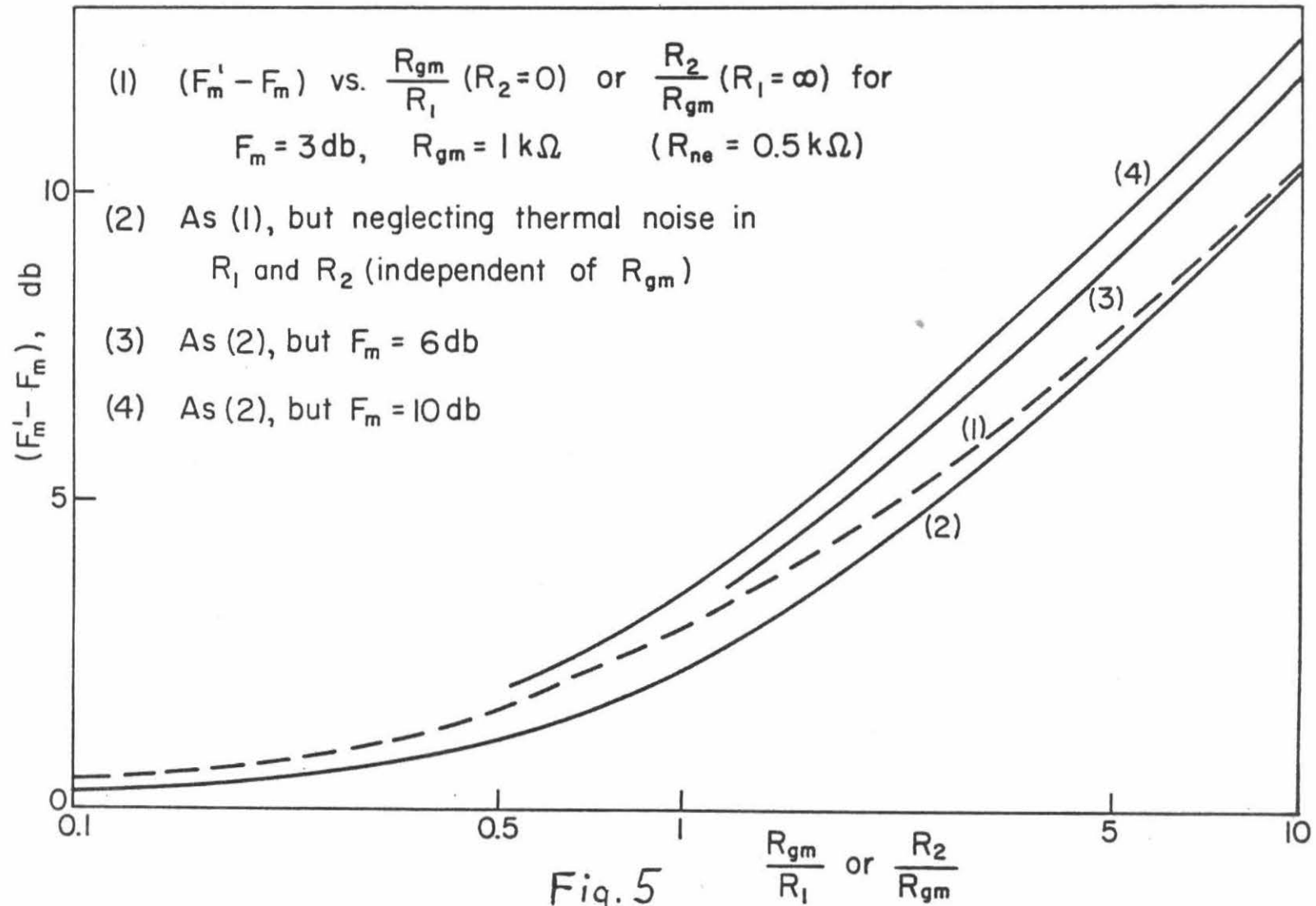
(1) $(F_m' - F_m)$ vs. $\frac{R_{gm}}{R_1}$ $(R_2 = 0)$ or $\frac{R_2}{R_{gm}}$ $(R_1 = \infty)$ for
$F_m = 3$ db, $R_{gm} = 1\,k\Omega$ $(R_{ne} = 0.5\,k\Omega)$
(2) As (1), but neglecting thermal noise in R_1 and R_2 (independent of R_{gm})
(3) As (2), but $F_m = 6$ db
(4) As (2), but $F_m = 10$ db
$(F_m' - F_m)$, db
10
5
0
0.1
0.5
1
5
10
$\frac{R_{gm}}{R_1}$ or $\frac{R_2}{R_{gm}}$
(1)
(2)
(3)
(4)

Fig. 5

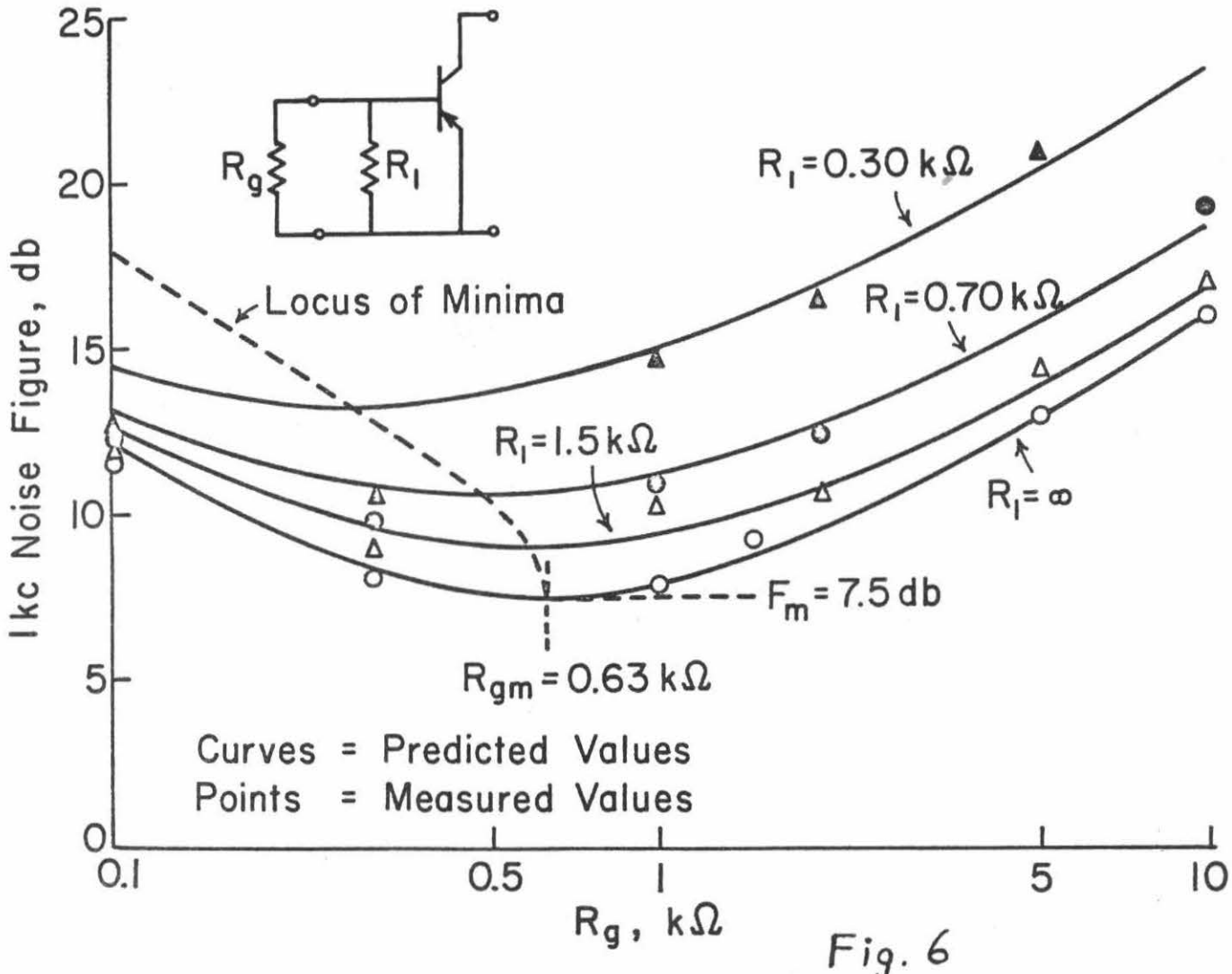
25
20
15
10
5
0
1kc Noise Figure, db
R_g
R_1
Locus of Minima
R_1=0.30 kΩ
R_1=0.70 kΩ
R_1=1.5 kΩ
R_1=∞
F_m=7.5 db
R_{gm}=0.63 kΩ
Curves = Predicted Values
Points = Measured Values
0.1
0.5
1
5
10
R_g, kΩ

Fig. 6

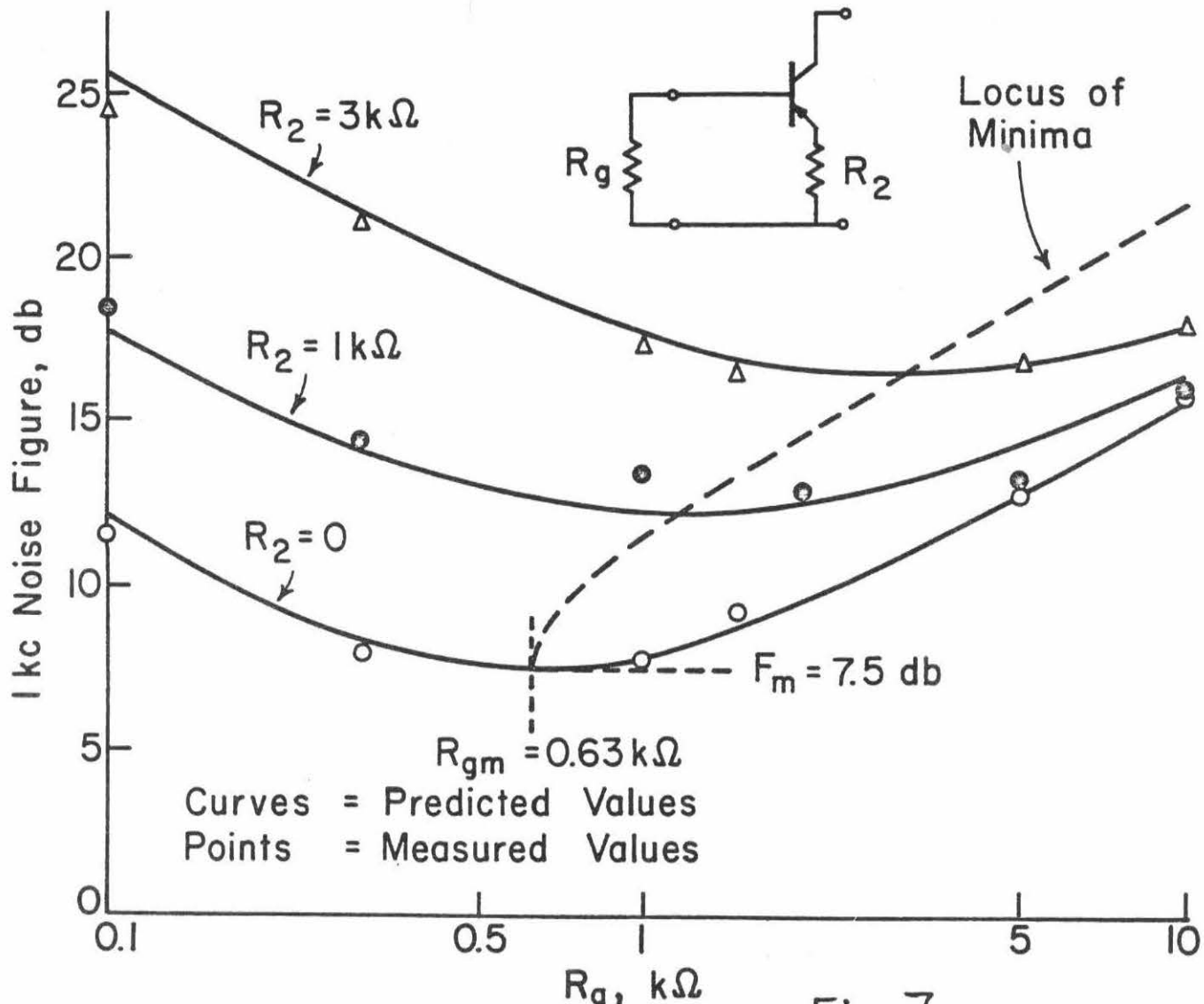
1 kc Noise Figure, db
25
20
15
10
5
0
0.1
0.5
1
5
10
R_g, kΩ
R_2 = 3kΩ
R_2 = 1kΩ
R_2 = 0
R_g
R_2
Locus of Minima
F_m = 7.5 db
R_{gm} = 0.63kΩ
Curves = Predicted Values
Points = Measured Values

Fig. 7

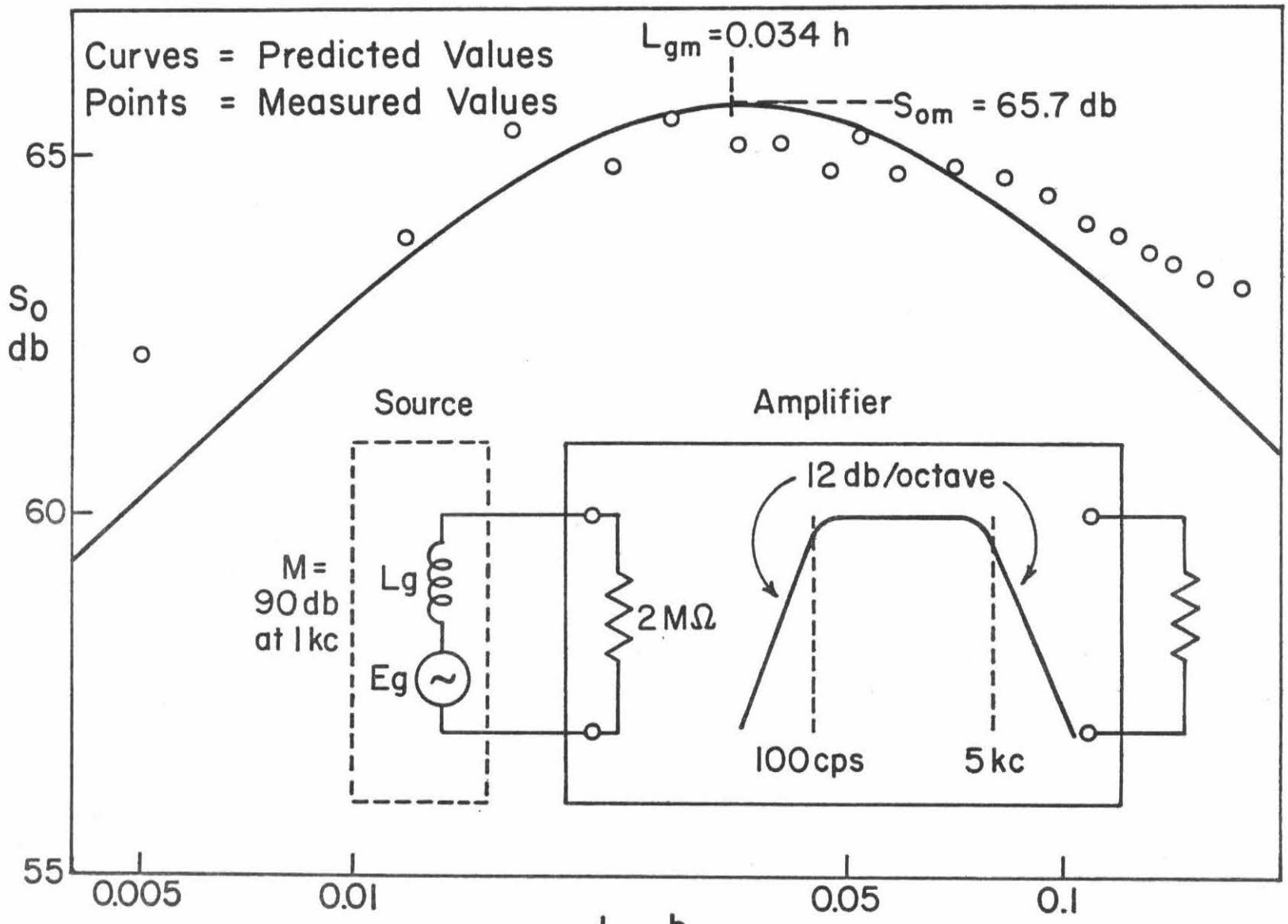
Curves = Predicted Values
Points = Measured Values
L_{gm} = 0.034 h
S_{om} = 65.7 db
65
60
55
S_o db
Source
Amplifier
M = 90 db at 1 kc
Lg
Eg
2 MΩ
12 db/octave
100 cps
5 kc
0.005
0.01
0.05
0.1
L_g, h

Fig. 8

TRANSISTOR AC AND DC AMPLIFIERS WITH HIGH INPUT IMPEDANCE

ABSTRACT

A class of transistor amplifiers is described in which high input impedance is achieved with good bias stability. Input impedances of the order of megohms shunted by one or two micromicrofarads are easily realized with simple circuits, and higher impedances may be obtained with more elaborate circuitry. Other important properties are that input shunt capacitance can be almost completely eliminated, the voltage gain is stabilized, and the output impedance is low. Typical practical measurements are given, and various illustrative circuits are shown for both ac and dc amplifiers.

I. Introduction

The inherently low input impedance of a transistor requires specific efforts on the part of the circuit designer to achieve high input impedances in transistor amplifiers. Some form of negative feedback will solve this problem; however, a high degree of bias stability is usually required, and when faced with a practical design one's first conclusion is that high input impedance and high bias stability are incompatible.

Since the emitter-follower configuration offers the highest input impedance of the three, attempts have been made to achieve high input impedances by using one or more emitter followers in cascade[1], as shown in Fig. 1. The input impedance of such a single emitter-follower stage is approximately βR shunted by the parallel combination of the collector resistance and capacitance. By operating the stage at low current, the input impedance may be made high. There are three major disadvantages of this arrangement: (1) the operating point is completely unstabilized, since the floating base forces the collector current to be approximately βI_{c0}, where I_{c0} is the collector saturation current, and hence is exponentially dependent on temperature; (2) the input resistance is shunted by the collector capacitance; (3) when driven from a high impedance source, which would often be the case when a high-impedance input is called for, the frequency response is limited by the β cutoff frequency of the transistor.

Attempts to improve the bias stability must involve setting the voltage level of the input base, which in turn requires a low-impedance bias source such as shown in Fig. 2. Thus immediately the previously high input impedance is shunted by the low impedance bias source, leading to the incompatibility mentioned above.

Many improvements can be made in the basic circuit of Fig. 2 to increase the input impedance and yet maintain adequate bias stability. Such attempts involve multi-stage amplifiers with ac negative feedback to stabilize gain, dc negative feedback to stabilize operating points, and "bootstrapping" the input bias potential divider to minimize its shunting effect on the input impedance[2]. The bootstrapping technique actually involves positive feedback with less-than-unity loop gain.

All these well-established techniques are applicable to the circuits to be described in this paper, which utilize in addition both negative and positive feedback with greater-than-unity loop gain. These circuits exhibit, even without bootstrapping, input resistances of the order of megohms with a high degree of bias and gain stability, and moreover the detrimental effects of input-stage collector capacitance and input stray capacitance can be almost completely eliminated. A typical figure for the input impedance of such an amplifier is $4M\Omega$ shunted by $1\mu\mu f$, measured at the input end of a shielded cable with $73\mu\mu f$ shunt capacitance. Examples of both ac and dc high impedance amplifiers will be given in the following sections.

II. Principles of the new high-impedance circuit

The basic form of the new high input impedance ac amplifier is shown in Fig. 3. The circuit contains a two-stage common-emitter amplifier, and bias stability is achieved by the battery-resistor combination E_b, R_b, which represents any of the many forms of bias arrangement, such as the potential divider type shown in Fig. 2.

Consider first the dc bias conditions. If R_b is small, the base current of transistor No. 1 is able to take the value required to make the voltage drop across R_1 equal to E_b. Because of the current gain

of transistor No. 2, the current through R_2 is almost the same as that through R_1. Thus the voltage across $(R_1 + R_2)$, which is the output dc level, is approximately $E_b(R_1 + R_2)/R_1$, and is hence stabilized against changes in both the β and the I_{c0} of both transistors. This is a well-known solution to the bias stability problem, but has heretofore been inapplicable to high input impedance circuits because the bias resistor R_b limits the input impedance. However, in the new circuit this difficulty is overcome by the positive feedback link through R_n and C_n, as shown below.

Consider next the ac signal conditions. A simple ac equivalent circuit of Fig. 3 may be drawn as shown in Fig. 4. Each transistor is represented by a simple equivalent circuit in which the base and emitter resistances are neglected and the collector current is β times the base current. The collector impedance of No. 2 is neglected since it is in parallel with the relatively small $(R_1 + R_2)$; however, the collector impedance of No. 1 (collector resistance r_c in parallel with the space-charge capacitance C_c) is important, and effectively appears between the input terminal A and ground (since the collector of No. 1 is effectively at ac ground through the base-emitter junction of No. 2). Also appearing between A and ground are the bias source resistance R_b and any stray capacitance C_s between the input leads. The four parallel elements r_c, C_c, R_b, C_s may all be lumped together in an admittance Y_1, and the parallel combination of R_n and C_n may be represented by an admittance Y_n.

The following approximations may be made, where the symbols are as defined in Fig. 4:

(a) $\beta_2 \gg 1$, hence the current through R_1 is essentially the same as that through R_2.

(b) $1/Y_n \gg R_1 + R_2$, hence $i_f \ll \beta_1\beta_2 i_{b1}$ and the current through R_2 (and R_1) is essentially equal to $\beta_1\beta_2 i_{b1}$.

To compute the voltage gain, consider a signal voltage $+v_1$ applied at the input. Since the base and emitter resistances of No. 1 are neglected, the voltage across R_1 is v_1. Hence, because of approximation (a), the output voltage at B is equal to $v_1(R_1 + R_2)/R_1$. Thus the voltage gain G_v is

$$G_v = \frac{v_2}{v_1} = \frac{R_1 + R_2}{R_1} \tag{1}$$

and is greater than 1 and is independent of transistor parameters.

The input impedance is by definition v_1/i_1, or the input admittance Y_{in} is

$$Y_{in} = \frac{i_1}{v_1} \tag{2}$$

By summing currents at junction A:

$$i_1 = i_{b1} + i_s - i_f \tag{3}$$

where

$$i_{b1} = \frac{v_1}{\beta_1\beta_2 R_1} \tag{4}$$

$$i_s = Y_i v_1 \tag{5}$$

$$i_f = Y_n(v_2 - v_1) = Y_n\left(\frac{R_1 + R_2}{R_1} - 1\right) v_1 \tag{6}$$

$$= Y_n\left(\frac{R_2}{R_1}\right) v_1 \tag{7}$$

Hence

$$Y_{in} = \frac{1}{\beta_1 \beta_2 R_1} + Y_i - \frac{R_2}{R_1} Y_n \qquad (8)$$

The interpretation of this result is as follows:

(a) The term $1/\beta_1\beta_2 R_1$ is the admittance at the input of the first transistor, and can easily be made many megohms.

(b) The term Y_i expresses the shunting effect of transistor collector admittance, bias supply resistance, and stray admittance across the input. The bias supply resistance R_b is essential if any attempt is made to stabilize the dc operating condition. By proper bootstrapping techniques both R_b and the collector impedance may be raised in effective value, but not eliminated. However, this approach can not reduce the effect of the stray capacitance C_s, and in general will increase its value with detrimental results.

(c) The term $Y_n(R_2/R_1)$ is a result of the feedback network Y_n and acts to reduce the effect of the other two. Clearly, by proper choice of component values, the input admittance can be made small, zero, or even negative.

It might seem that the optimum choice of Y_n would be that leading to zero admittance, or infinite impedance. However, in practice this is undesirable since the adjustment is quite sensitive to changes in $\beta_1\beta_2$. To overcome this problem it is only necessary to choose Y_n such that the second and third terms exactly cancel. This adjustment is independent of transistor parameters. For this condition

$$Y_n = \frac{R_1}{R_2} Y_i \qquad (9)$$

The input impedance Z_{in} is then

$$Z_{in} = 1/Y_{in} = \beta_1\beta_2 R_1 \tag{10}$$

which is the theoretical limit obtainable with conventional circuits assuming perfect bootstrapping and no stray input admittance. This impedance can easily be made higher than any value normally required in practice.

Under the condition $Y_n = Y_i(R_1/R_2)$ described above, the circuit exhibits the following properties:

(1) Stabilized dc operating conditions determined by the bias supply E_b, R_b and independent of transistor parameters. Various bias methods equivalent to and superior to the bias supply E_b, R_b are discussed later.

(2) Stabilized voltage gain $G_v = v_2/v_1 = (R_1 + R_2)/R_1$ which is independent of transistor parameters.

(3) The input impedance is large, i.e., $Z_{in} = \beta_1\beta_2 R_1$ and remains large up to the β cutoff frequency of transistor No. 1 or No. 2. Note in particular that the stray admittance across the input terminals and the collector admittance of No. 1 do not shunt Z_{in}: these effects have been removed in the circuit adjustment.

(4) The output impedance is low, being (R_2/β_2) if driven from a low impedance source.

Practical adjustment of the circuit to a desired input impedance is conducted as follows. The approximate value of R_n is given by

$$R_n = \frac{R_2}{R_1} R_b \tag{11}$$

which is Eq. (9) for low frequencies and in which the shunting effect of r_c is neglected. The exact value of R_n is set by a dynamic measurement: observe the output voltage v_2 when the input is fed through a source resistance R_s from an oscillator set to some midband frequency, say 1kc. Let the output voltage be v_2 when R_s is present, and v_2' when R_s is short-circuited. The input resistance is then

$$R_{in} = \frac{R_s}{(v_2'/v_2) - 1} \qquad (12)$$

and R_n can be adjusted until R_{in} reaches the desired value. For example, if the output voltage is 1v with R_s absent, then the input resistance will be 1MΩ if R_n is adjusted so that the output voltage falls to 0.5v when $R_s = 1M\Omega$ is inserted in series with the input.

The value of C_n is next adjusted so that the output voltage stays at the same value up to as high a frequency as possible, measured with R_s present and the oscillator output maintained at constant amplitude. It will be found that it is possible to increase the output voltage at higher frequencies in this way; this corresponds to over-compensation of the total shunt input capacitance $(C_c + C_s)$. Such a condition is liable to introduce instability, and C_n should be adjusted so that an acceptable degree of peaking, perhaps 10%, is achieved.

Measurements made on a typical circuit after adjustments were made in this way are given in Section III.

III. Practical ac high-impedance amplifier

Many practical embodiments of the basic circuit of Fig. 3 are possible. The most obvious modification eliminates the separate bias battery E_b by substitution of a potential divider as shown in Fig. 2: the

effective ac value of R_b is then the parallel combination of the two bias resistors.

Although the collector current of transistor No. 2 may be well stabilized, as described in the previous section, a disadvantage of the basic circuit of Fig. 3 is that the collector current of No. 1 is equal to the base current of No. 2, and is therefore small and may be widely variable from one circuit to another. A way to overcome this difficulty is shown in Fig. 5, which also contains some other improvements. The collector current of No. 1 is determined by the dc voltage across R_3 and the emitter bias resistor R_6, the base voltage of No. 2 is determined by the drop across R_8, and the collector current of No. 2 is then fixed by R_7. Overall dc negative feedback to improve the bias stability still further is obtained by returning the high end of the bias resistor R_5 to the low end of R_7, instead of to the supply voltage. It will be noted that the ac equivalent circuit of this arrangement is identical with that of the basic circuit shown in Fig. 4, except that the effective value of R_b is increased because both bias resistors R_3 and R_4 are bootstrapped to the emitter of No. 1. It will also be noticed that in Fig. 6 the blocking condenser in series with R_n and C_n has been omitted: this improves the low-frequency performance of the amplifier, but has the disadvantage that positive feedback exists at dc which tends to degrade the bias stability.

Practical design values and performance data will be given for a typical ac high impedance amplifier of the general type discussed in the previous section. The circuit is shown in Fig. 6, and contains bias arrangements somewhat less elaborate than those shown in Fig. 5. No attempt is made to bootstrap the bias resistors; however, dc negative feedback is applied to the bias resistors, and the collector current of No. 1 is fixed

at about 0.25ma by the presence of R_8. The collector current of No. 2 is stabilized at 1ma, and hence the voltage operating level of the No. 2 emitter is -10v, and that of the No. 2 collector is -5v. The common-emitter current-gains of the two transistors used were $\beta_1 = 75$, $\beta_2 = 64$. The equivalent bias resistor R_b is the value of R_3 in parallel with R_4, or 40kΩ; hence it is expected that the positive feedback resistor should be $(R_2/R_1)R_b = 160k\Omega$. Since fine adjustment of R_n is required, the circuit suitably contains a 120kΩ fixed resistor in series with a 50kΩ potentiometer.

The voltage gain of the circuit is $(R_1 + R_2)/R_1 = 4.9$, and was measured to be 5.0 at 1kc. The gain was not noticeably less at 5cps, and fell by 3db at 1.3Mc. The magnitude of the input impedance, $|Z_{in}|$, is shown in Fig. 7 as a function of frequency for various conditions. Curves 1 and 2 show $|Z_{in}|$ as a function of frequency when R_{in} at 1kc is adjusted to 4MΩ and to 1MΩ, respectively, as described in the previous section. It is observed that the high impedance is maintained to over 100kc in each case, and the decrease in $|Z_{in}|$ at higher frequencies may roughly be ascribed to the presence of an effective shunt input capacitance of 1μμf. Curve 3 shows $|Z_{in}|$ as a function of frequency when R_{in} at 1kc is adjusted to 1MΩ in the presence of an input shielded cable with 73μμf shunt capacitance. The equivalent input shunt capacitance is about 2μμf: note that this is the apparent capacitance at the <u>input</u> of the shielded cable.

The decrease in $|Z_{in}|$ at low frequencies is caused by the 0.5μf capacitor C in series with R_n and C_n. This was purposely made small in order to illustrate its effect. At first glance it would appear that $|Z_{in}|$ should be reduced by a factor of 2 at a frequency $f_0 = 1/2\pi R_n C$;

however, analysis shows that this frequency is actually $f_0 = R_{in}/2\pi R_n C R_{in}'$, where R_{in} and R_{in}' are the midband input resistances with and without R_n present. Thus the effective time constant $R_n C$ is reduced whenever positive feedback is introduced to increase the input impedance. Substitution of numerical values $R_n = 160k\Omega$, $C = 0.5\mu f$, $R_{in}' = 40k\Omega$ ($\approx R_b$) shows that f_0 is about 50cps for $R_{in} = 1M\Omega$ and about 200cps for $R_{in} = 4M\Omega$. These values are in reasonable agreement with the results of Fig. 7. The high input impedance can, of course, easily be extended to lower frequencies by increasing C, or C can be omitted altogether with consequent degradation in dc stability.

Figure 8 shows the output resistance R_{out} at 1kc of the circuit of Fig. 6, as a function of source resistance R_s. The presence of positive feedback to increase R_{in} also increases R_{out} at high values of source resistance; obviously if $R_s = 0$, R_{out} is independent of any positive feedback, and the predicted value is easily seen from Fig. 4 to be $R_{out} = R_4/\beta_2$. The curves shown in Fig. 8 were taken with a transistor No. 2 having $\beta_2 = 34$, thus $R_{out} = 3900/34 = 115\Omega$ which agrees well with the measured results for $R_s \rightarrow 0$. Although the output resistance is not large unless high values of source resistance are used, the output resistance can, of course, be reduced by addition of an emitter-follower stage to the output.

It is of interest to observe the effects of changing transistors on the operating points and on the input impedance. Table I shows the variations in the output dc voltage V_0 and in the input resistance R_{in} at 1kc as transistors were changed. It can be seen that the operating point is well stabilized, but that re-adjustment of R_n would be necessary to maintain R_{in} constant.

TABLE I

β_1	β_2	V_0	R_{in}
75	64	5.0v	1.0MΩ
52	64	4.6	0.8
75	34	5.0	0.6
52	34	4.5	0.5

It is impractical to try to adjust the input resistance to more than about 100 times the value of R_b, hence in the practical circuit of Fig. 6 4MΩ is about the highest input resistance which can be achieved with reasonable stability. However, if bootstrapping were employed as shown in Fig. 5, input resistances higher than 4MΩ could easily be achieved.

IV. Dc high impedance amplifiers

The principles outlined in the previous sections may be extended to dc amplifiers by the addition of a third transistor.

One possible basic arrangement is shown in Fig. 9. By proper choice of component values, both the input and output may be set at ground level for zero signal. Both positive- and negative-going signals can be accommodated. The voltage gain is $(R_1 + R_2)/R_1$, and the input admittance Y_{in} is

$$Y_{in} = \frac{R_1 + R_2 + R_9}{\beta_1 \beta_2 R_1 R_9} + Y_i - \frac{R_2}{R_1} Y_n \qquad (13)$$

where Y_i and Y_n are as defined in Fig. 4 and have the same significance in Fig. 9.

Another possible arrangement of a high impedance dc amplifier is shown in Fig. 10. This circuit differs from that of Fig. 9 in that transistor No. 2 is in common-collector instead of in common-emitter

connection, and to maintain correct phase relationships the base drive for No. 2 must be derived from the collector of No. 3 instead of from that of No. 1. The voltage gain is again $(R_1 + R_2)/R_1$, and the input admittance is

$$Y_{in} = \frac{R_1 + R_2}{\beta_1 R_1 R_8} + Y_i - \frac{R_2}{R_1} Y_n \qquad (14)$$

The relative merits of the circuits of Figs. 9 and 10 are as follows. In Fig. 10, the output can not be set at zero dc level, unless the output is taken from the junction of R_1 and R_2 instead of from the emitter of transistor No. 2, in which case the voltage gain is unity. The first term on the right-hand side of the equation for the input admittance is larger for the circuit of Fig. 10 than for that of Fig. 9, hence a greater degree of positive feedback through Y_n is necessary to attain a given input admittance. In the circuit of Fig. 10, all the transistors are of the same type, and also the phase shift within the feedback loop is less than in the circuit of Fig. 9, and hence greater stability results.

V. Conclusions

Principles of transistor amplifiers have been described which employ both negative and positive feedback, whth greater-than-unity loop gain, to realize high input impedance with good bias stability. Two-stage ac amplifiers and three-stage dc amplifiers are described which exhibit input impedances of the order of megohms shunted by one or two micromicrofarads. Ac bootstrapping would enable even higher ac impedances to be realized with the same degree of bias stability. Other desirable features are that input shunt capacitance, such as that of a shielded cable, can be

almost completely eliminated, the voltage gain is greater than unity and is stabilized, and the output impedance is low for low source impedances. Typical practical measurements are given, and various illustrative circuits are shown for both ac and dc amplifiers.

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2. P. J. Anzalone, "A high input impedance transistor circuit," Electronic Design, Vol. 5, June 1, 1957; pp. 38-41.

FIGURES

1. Basic emitter-follower circuit for obtaining high input impedance.

2. Bias-stabilized emitter-follower circuit.

3. Basic circuit of a high input impedance, bias- and gain-stabilized amplifier.

4. Ac equivalent circuit of the high impedance amplifier of Fig. 3.

5. Possible modifications of the basic high impedance amplifier, including dc negative feedback to increase bias stability, and bootstrapping to increase the input impedance.

6. Practical high impedance amplifier with voltage gain of 5, input impedance up to $4M\Omega$ shunted by $1\mu\mu f$.

7. Input impedance as a function of frequency for the circuit of Fig. 6.

8. Output resistance as a function of source resistance for the circuit of Fig. 6.

9. One form of high impedance dc amplifier. Both input and output can be set at ground level.

10. Another form of high impedance dc amplifier. Output can not be set at ground level except with unity voltage gain.

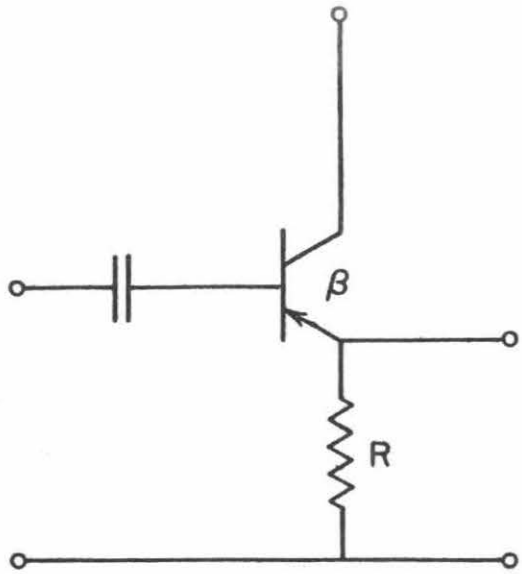

Fig. 1

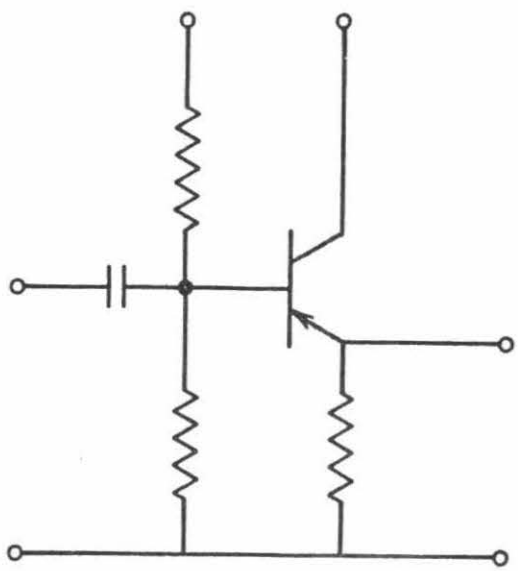

Fig. 2

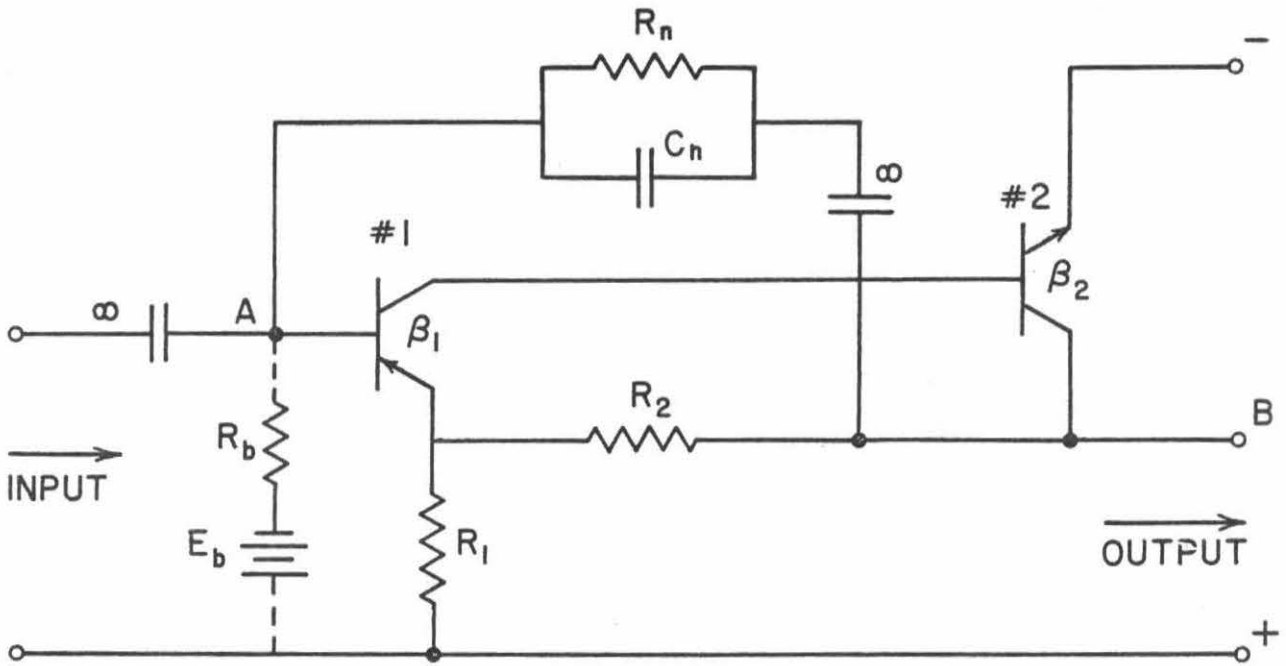

Fig. 3

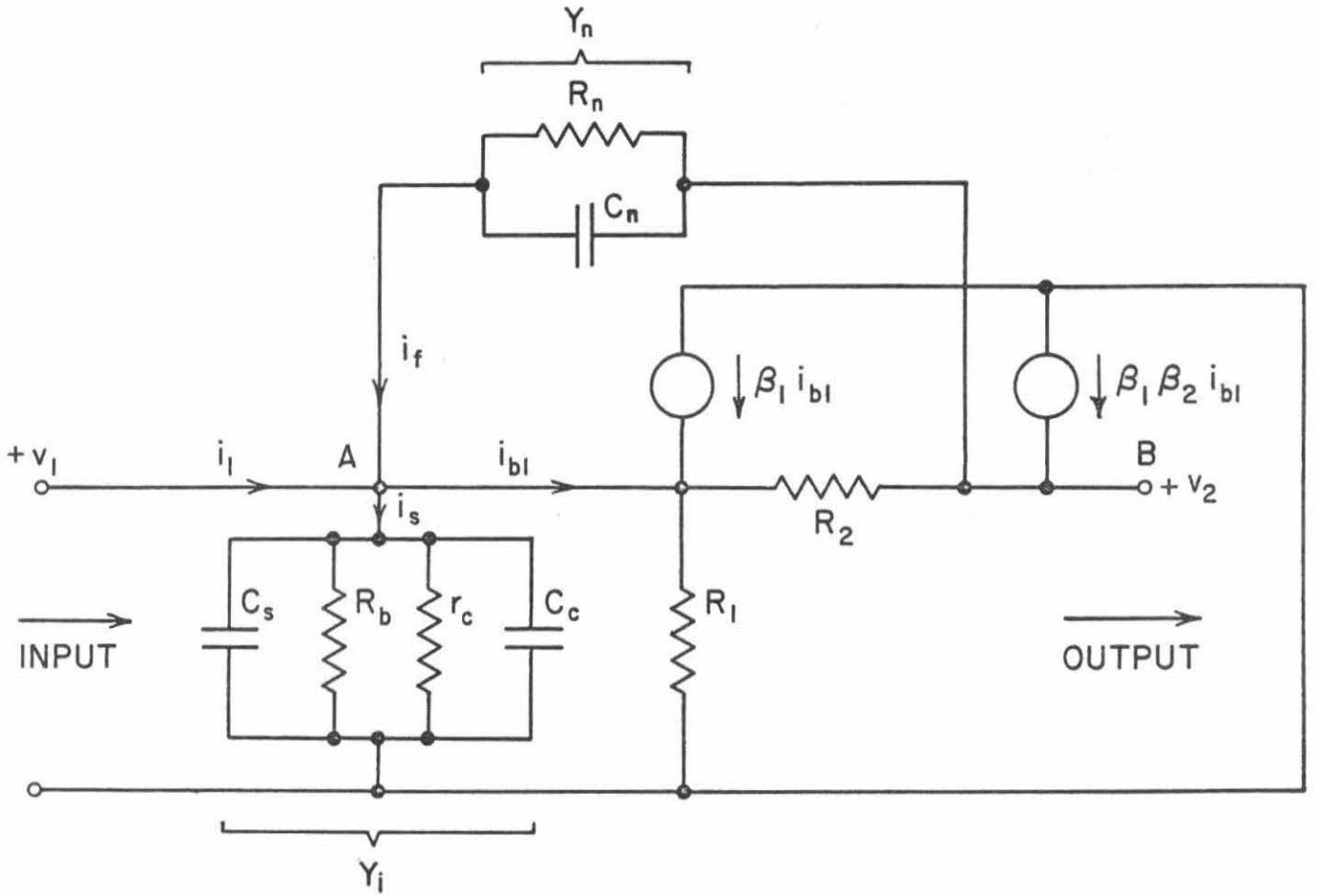
Y_n
R_n
C_n
i_f
$\beta_1 i_{b1}$
$\beta_1 \beta_2 i_{b1}$
$+v_1$
i_1
A
i_{b1}
B
$+v_2$
i_s
R_2
C_s
R_b
r_c
C_c
R_1
INPUT
OUTPUT
Y_i

Fig. 4

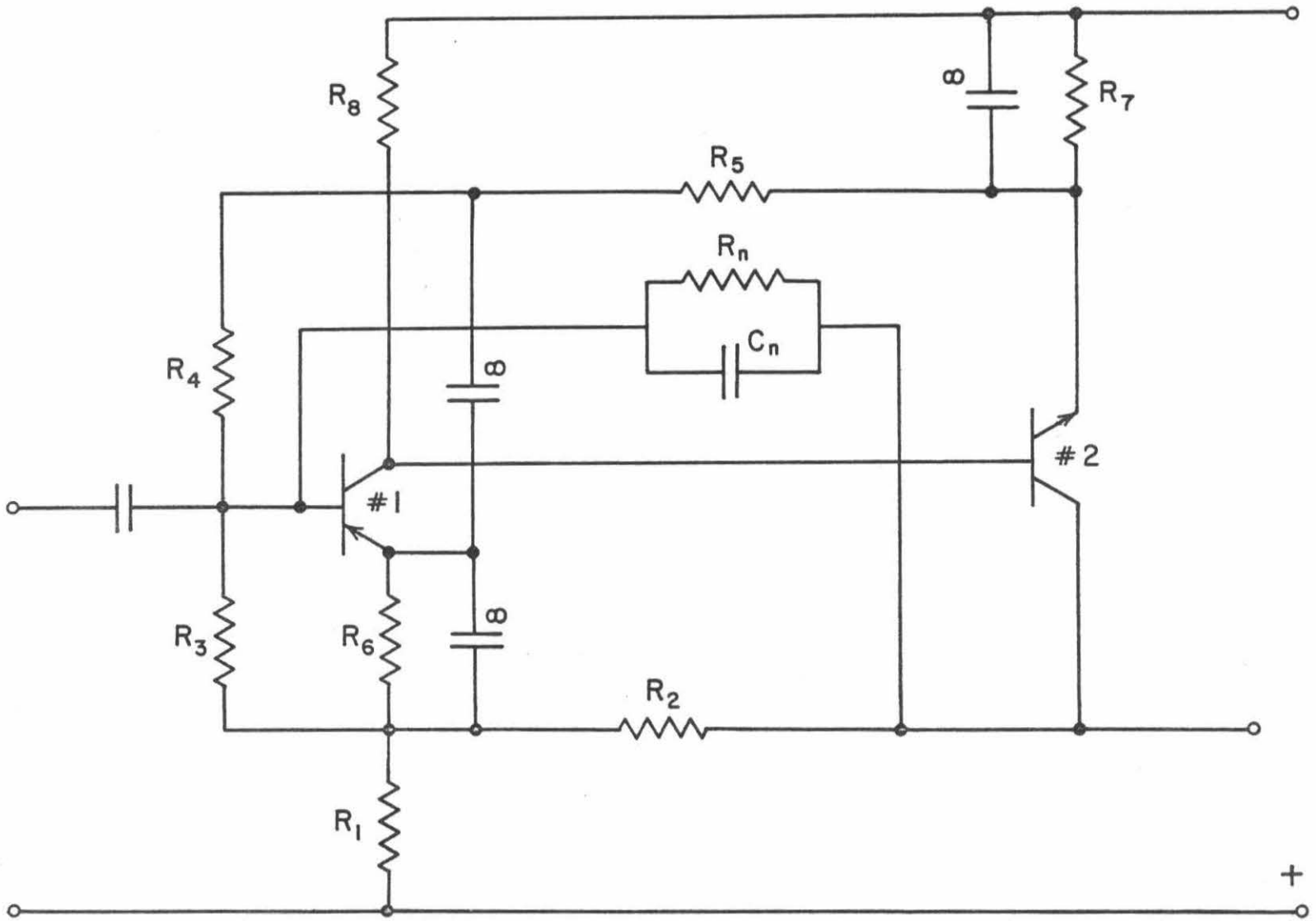

Fig. 5

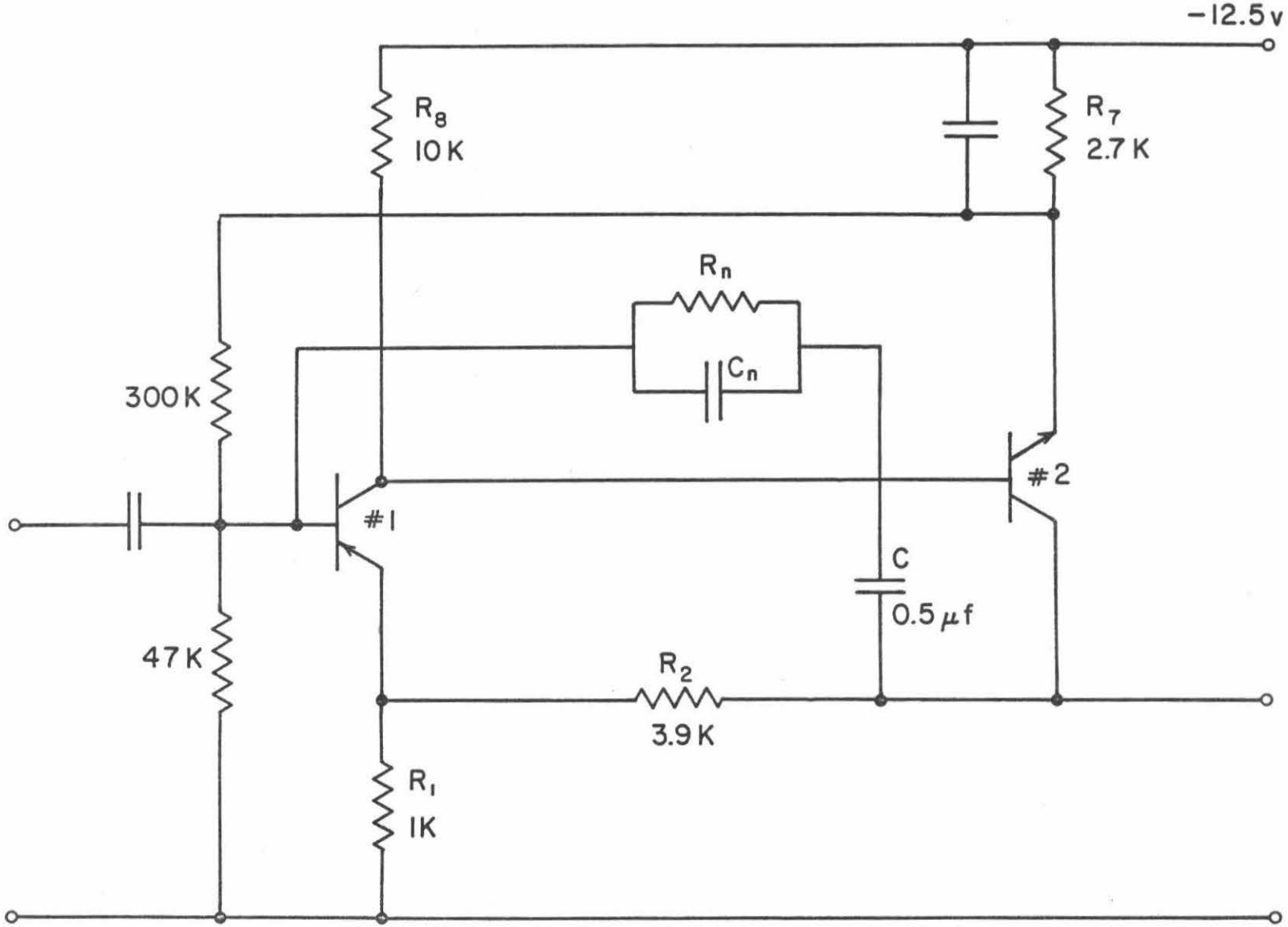

Fig. 6

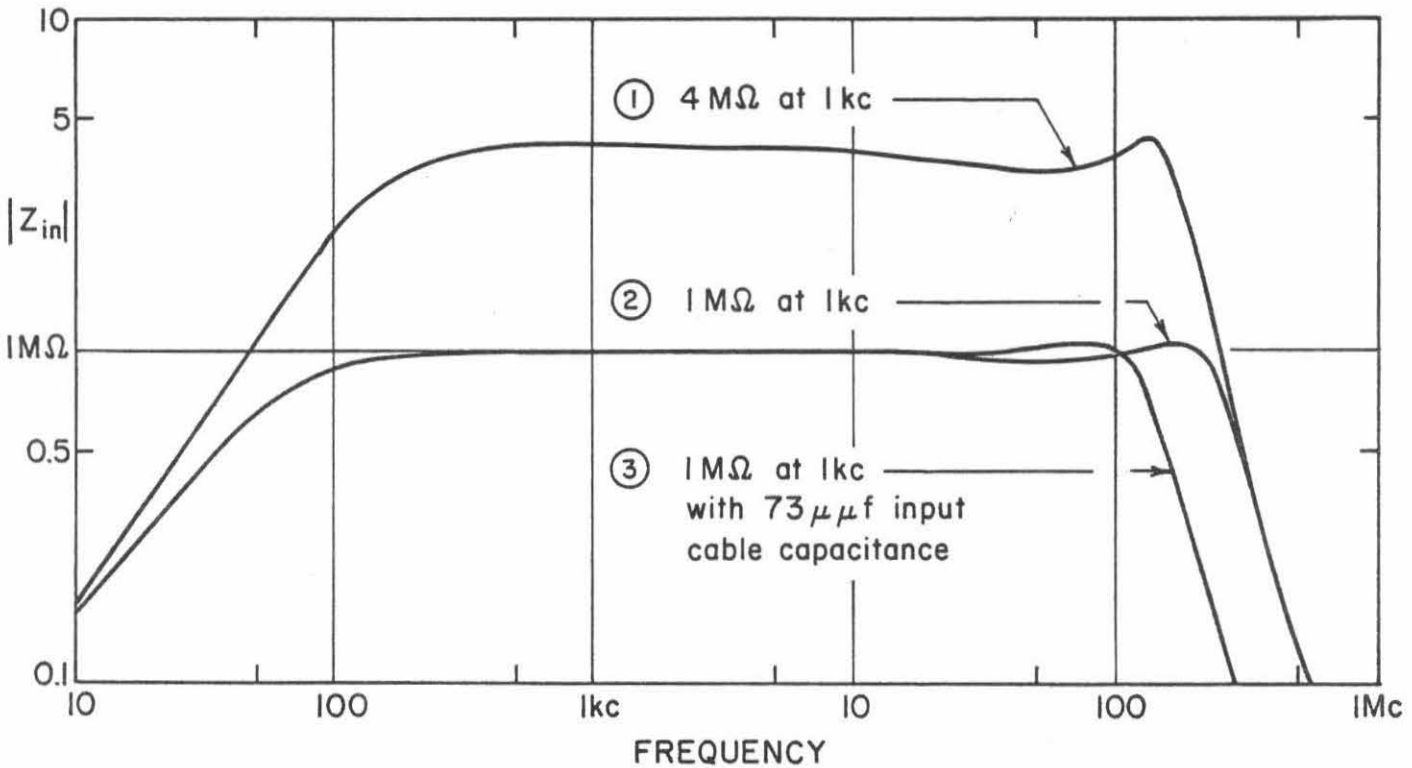
10
5
|Zin|
1MΩ
0.5
0.1
10
100
1kc
10
100
1Mc
FREQUENCY
① 4 MΩ at 1kc
② 1 MΩ at 1kc
③ 1 MΩ at 1kc
with 73 μμf input
cable capacitance

Fig. 7

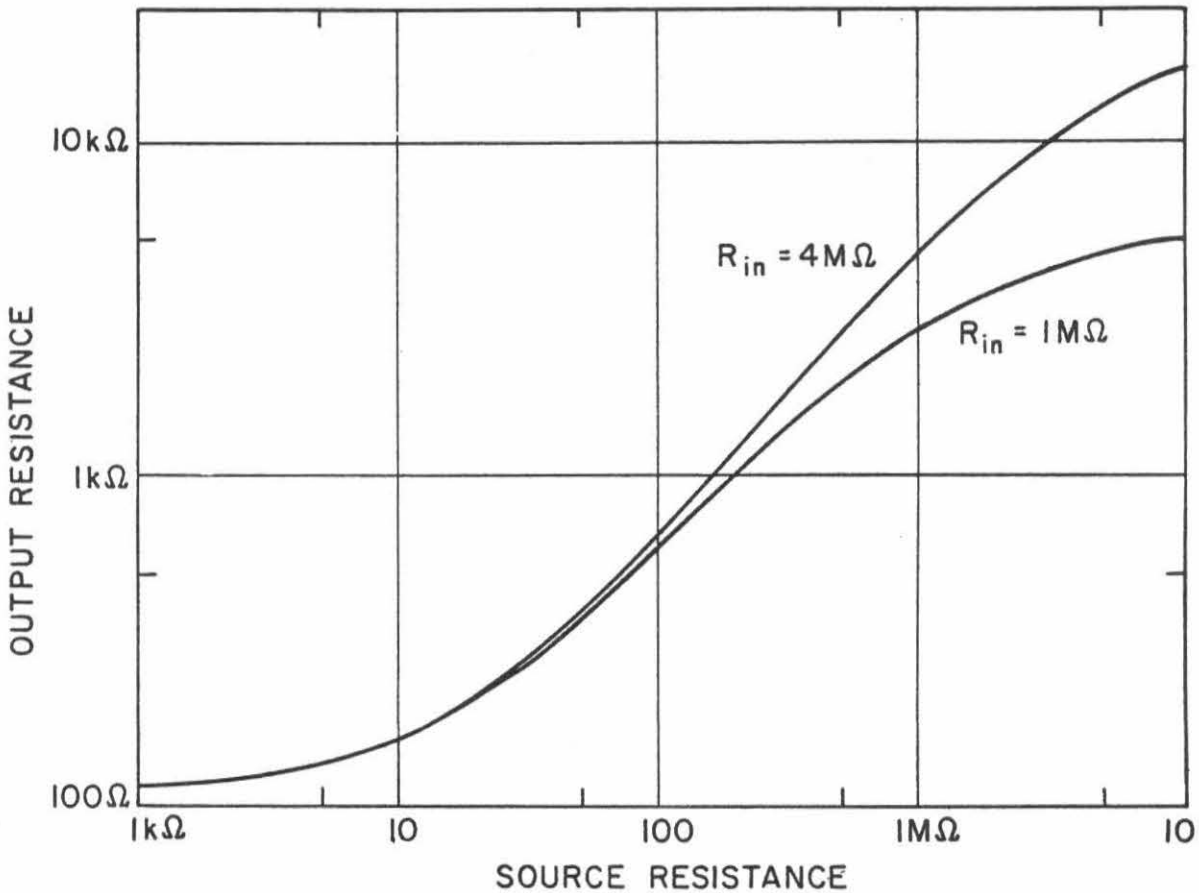
10kΩ
1kΩ
100Ω
OUTPUT RESISTANCE
R_{in} = 4MΩ
R_{in} = 1MΩ
1kΩ
10
100
1MΩ
10
SOURCE RESISTANCE

Fig. 8

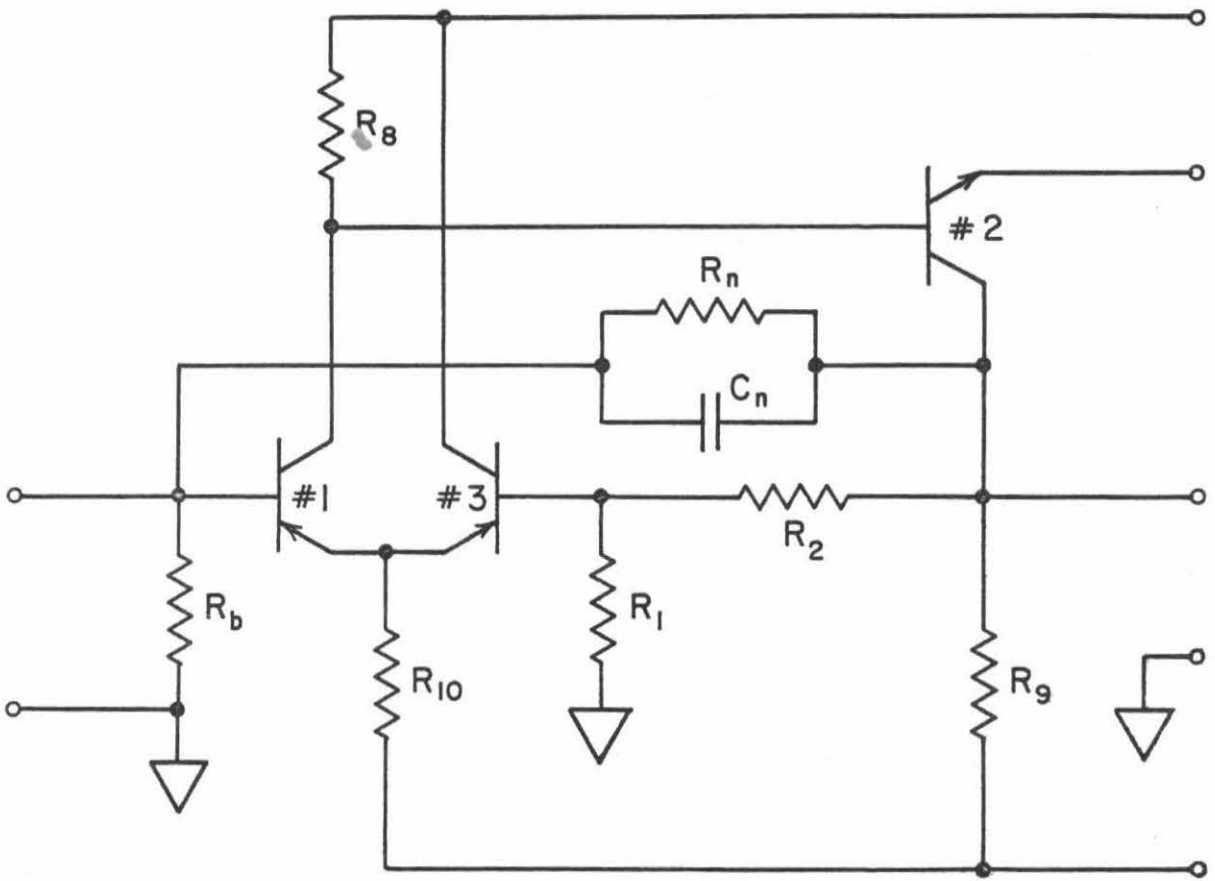

Fig. 9

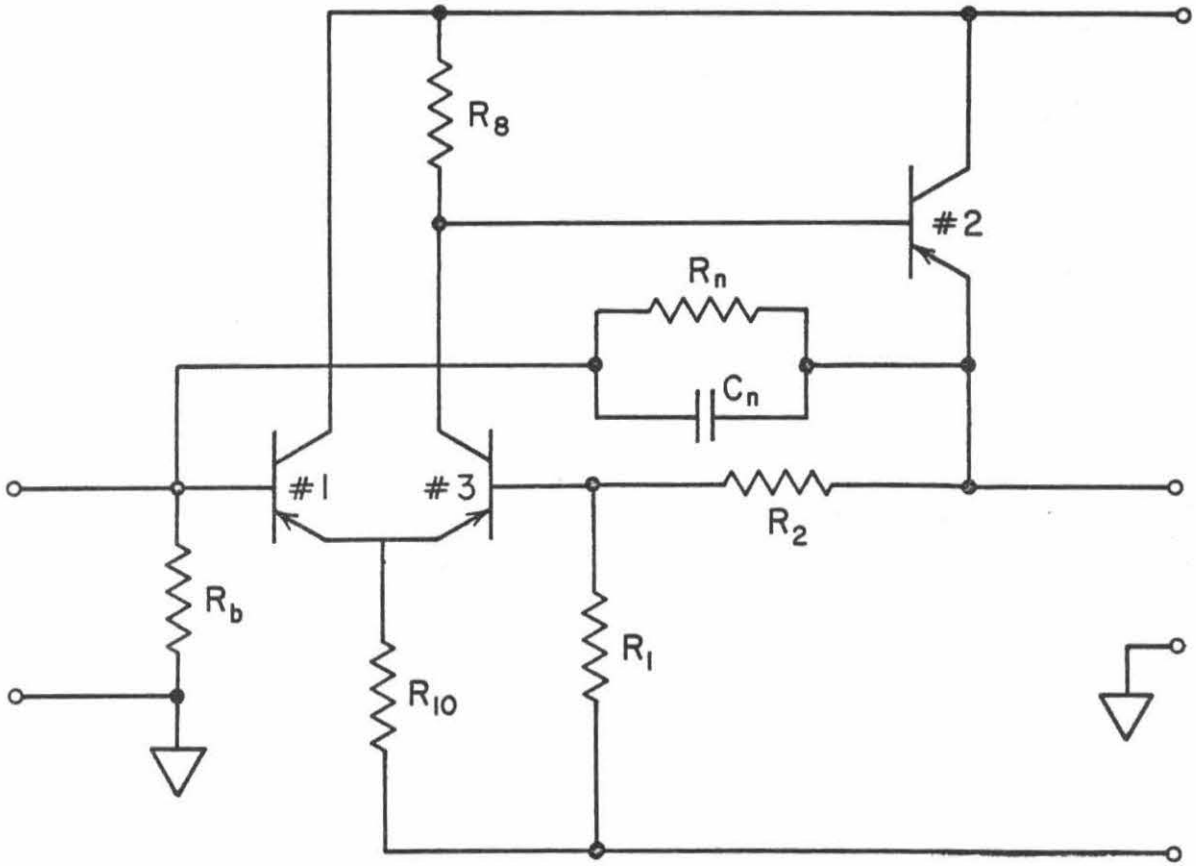

Fig. 10