Adaptation of Current Signals with Floating-Gate Circuits

Alberto Pesavento
Department of Electrical Engineering
California Institute of Technology
Pasadena, CA, 91125
alberto@klab.caltech.edu

Timothy Horiuchi
Zanvyl Krieger Mind/Brain Institute
Johns Hopkins University
Baltimore, MD, 21218
timmer@jhu.edu

Chris Diorio
Department of Computer Science and Engineering
University of Washington
Seattle, WA, 98195-2350
diorio@cs.washington.edu

Christof Koch
Computation and Neural Systems Program
California Institute of Technology
Pasadena, CA, 91125
koch@klab.caltech.edu

Abstract

In this paper we present a new, adaptive spatial-derivative circuit for use in CMOS image sensors. The circuit removes its offset as a natural part of its operation using a combination of electron tunneling and hot-electron injection to add or remove charge on a floating-gate of an auto-zeroing amplifier. We designed, fabricated and successfully tested a chip with the circuit. Test results show that the circuit reduces the offsets by more than an order of magnitude.

1. Introduction

The design of large arrays of analog circuits in VLSI is constrained by the inherent mismatch of transistors from the fabrication process. In photoreceptor arrays, the mismatch can appear as gain and offset errors. Under uniform intensity, such pixels will report slightly different values, producing a "fixed-pattern noise" image. While the removal of fixed-pattern noise is often performed by the subtraction of a calibration image stored on a downstream digital computer, the desire to combine both sensing and processing on the same chip ("smart sensors"), has precipitated the need for a more integrated solution. A common solution to this problem is to measure and store a correction value locally at each pixel which is subtracted before the output.

Although short-term storage can be performed on integrated capacitors, junction leakage from the connected circuitry limits its retention time to seconds, particularly for analog parameters. Floating-gate structures in VLSI (a MOS transistor with its gate completely surrounded by silicon dioxide), however, can provide an extremely effective charge-storage technique with its retention measured in years. Charge modification techniques using ultra-violet (UV) radiation [4, 9, 19, 14] and bidirectional Fowler-Nordheim tunneling (e.g., [18, 21, 2, 16]) have both been successfully tested; there are, however, some drawbacks to these techniques such as the need for a UV light source, multiple high-voltage supplies, or special fabrication processes. Recently the combination of tunneling and hot-electron injection [7] has emerged as a promising new charge-modification technique that requires only one high-voltage supply and standard CMOS fabrication processes. These types of structures are now being used for many different applications such as on-chip parameter storage (e.g., [4, 10, 17]) and neural networks (e.g., [22, 3, 20]).

As a result of these developments in technology, the use of floating-gate structures for fixed-pattern noise removal in images has been growing steadily in recent years. While earlier work used the UV technique to null offsets in a silicon retina [19], recent approaches have used bidirectional Fowler-Nordheim tunneling [6, 1] for storing image offset values.

In applications where the absolute image intensity is not preserved and the local spatial-derivative information is used, spatial-derivative is an appropriate signal to calibrate. This is the situation for many neuromorphic circuits [8] that adapt signals both spatially and temporally.

In this paper we present a new approach to fixed-pattern noise removal, by very slowly adapting the output of the spatial-derivative computation to zero rather than matching the photoreceptor outputs. Using the floating-gate auto-zeroing amplifier described by Hasler et al. [12, 11],

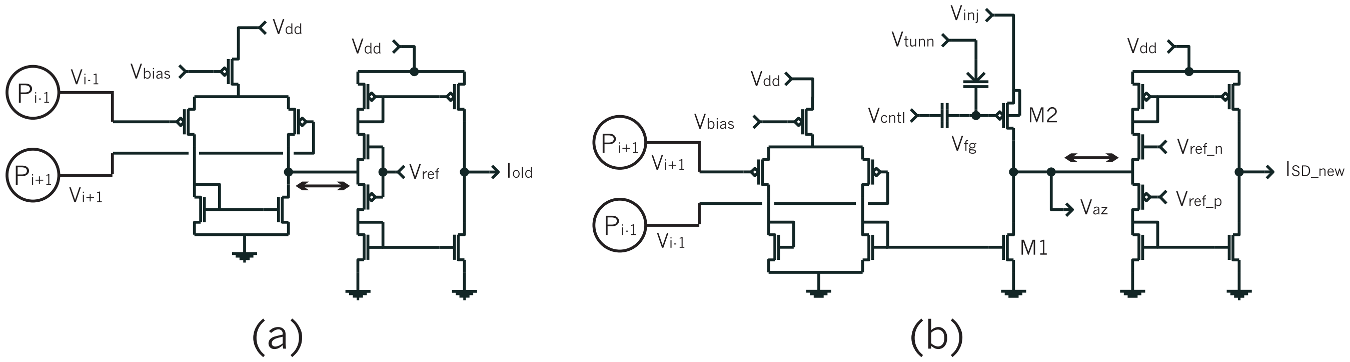

Figure 1. (a) Circuit diagram of the old circuit used to compute the spatial-derivative in analog VLSI imagers. (b) Circuit diagram of the adaptive spatial-derivative circuit. Adding the floating-gate amplifier and one bias line to the pair of stacked mirrors allows the circuit to remove offsets continuously.

a spatial-derivative circuit currently being used in other projects [15, 13] was modified to dramatically reduce offset errors, or equivalently, to increase the dynamic range. This circuit uses a combination of electron tunneling to reduce charge on the transistor gate and hot-electron injection to increase charge on the transistor gate.

2. Circuit Description

The circuit previously used to compute the spatial-derivative is shown in Fig. 1a. A transconductance amplifier receives input from two photoreceptors (P_{i+1} and P_{i-1}) and provides an output current that is a sigmoidal function of its differential input and therefore an approximation of the spatial-derivative of the input image. Positive current sourced from the amplifier is pushed into the n-type current mirror (in the bottom part of the pair of stacked mirrors) and negative current is drawn out of the p-type current mirror (in the top part of the circuit). The output arms of the two current mirrors are connected together to provide a bipolar output current. The two transistors connected to V_{ref} perform a thresholding operation, preventing very small spatial-derivative currents from appearing in the final output. While this can be desirable to reduce the effects of circuit offsets, it manifests itself as a "dead-zone" in the spatial-derivative transfer characteristics. Other configurations of the pair of stacked mirrors to compute the polarity or the absolute value of the bipolar current have been presented in the literature [15, 13].

The new circuit that we present is shown in Fig. 1b. The pFET differential pair is, in this case, terminated through a pair of diode-connected transistors. The diode-connected transistor on the right is the input to a current mirror which constitutes the input to the inverting auto-zeroing amplifier. This is the new output stage of the differential amplifier. As in the previous case, the output current is either drawn out of, or pushed into, the current mirrors on the top and bottom. The pair of stacked mirrors is a slightly modified version of the previous one to provide more control over the dead-zone created by the threshold voltages of the nFET and pFET transistors in the center.

Before considering the adaptive behavior of the circuit when tunneling and injection are present, let us first describe the principle of operation without considering the auto-zeroing properties of the amplifier.

If the two input voltages V_{i+1} and V_{i-1} are equal, the current provided by the bias transistor is divided equally between the two arms of the differential pair. Let us assume now that in this condition the voltage V_{az} sits at $V_{dd}/2$. When the output voltage of the photoreceptor P_{i+1} increases with respect to P_{i-1} more current starts flowing through the right-hand arm of the differential-pair and into the nFET current mirror. This increased current then pulls V_{az} down. There is a voltage level V_{down} at which the nFET controlled by V_{ref_n} turns on and the pFET mirror starts conducting, thus clamping the V_{az} voltage near V_{down}. The value of V_{down} is set by the threshold voltage of the nFET and by the bias voltage V_{ref_n}. If the difference between V_{i+1} and V_{i-1} keeps increasing then the current flowing through the pFET mirror will increase and V_{az} will remain very close to the same value. Conversely, if V_{i+1} is less than V_{i-1} the current through the diode connected nFET will decrease causing V_{az} to increase until the pFET controlled by V_{ref_p} turns on and the nFET mirror starts conducting. The voltage value at which V_{az} is clamped in the upswing, V_{up}, is set by the threshold voltage of the pFET and by V_{ref_p}. When V_{az} is between the two clamping voltages the final output of the spatial-derivative is zero; thus,

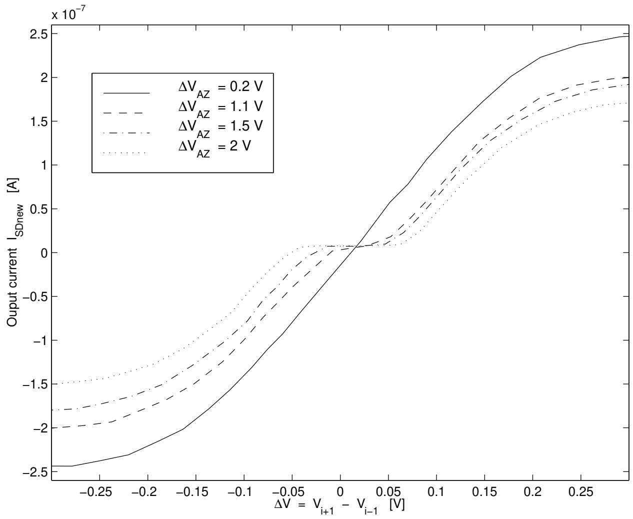

Figure 2. Plot of four different transfer characteristics obtained from the new spatial-derivative circuit for different values of $\Delta V_{AZ} = V_{up} - V_{down}$. A careful selection of the bias voltages V_{ref_n} and V_{ref_p} permits a transfer characteristic without a "dead-zone".

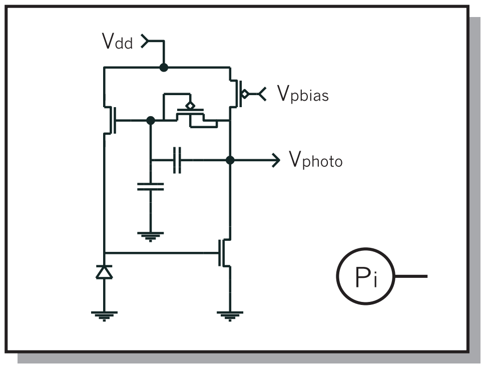

Figure 3. Schematic of the photoreceptor used in the chip and the symbol used in Fig. 1 to represent it.

for differential input voltages $\Delta V = V_{i+1} - V_{i-1}$ such that $V_{down} < V_{az} < V_{up}$ the circuit fails to compute the correct spatial-derivative. To avoid this dead-zone in the transfer characteristics, it is necessary to set the bias voltages V_{ref_n} and V_{ref_p} so that the dead-zone is at a minimum. In Fig. 2 we plot different transfer characteristics obtained from the circuit as a function of the value of $\Delta V_{AZ} = V_{up} - V_{down}$.

Let us now consider the behavior of the circuit with the auto-zeroing, floating-gate amplifier [12, 11]. The auto-zeroing, floating-gate amplifier is a simple two transistor amplifier stage, (transistors M1 and M2 in Fig. 1), that has the ability to adapt its steady state output voltage to lie at a value determined largely by fabrication parameters and global circuit variables and minimally by the individual signal levels. This adaptation is performed by modifying the charge on the floating-gate of the pFET transistor. Electrons are removed from the floating-gate by means of Fowler-Nordheim tunneling and added by pFET hot-electron injection. The steady-state output voltage is kept nearly constant by changing the charge on the floating-gate. The amplifier reaches equilibrium when the tunneling current equals the injection current. The hot-electron injection current increases linearly with I_{pFET} and exponentially with V_{ds}, while the tunneling current increases exponentially with the voltage across the gate oxide ($V_{tunn} - V_{fg}$). The tunneling process tends to turn the pFET transistor off and the injection process tends to turn the transistor on. Because the output of the amplifier directly controls V_{ds}, the amplifier provides a high-gain, negative feedback signal which drives the system to equilibrium. By modifying V_{tunn} and V_{inj}, the steady-state output voltage and the rate of adaptation can be controlled.

Fabrication mismatch is always present in any CMOS processes and this usually translates into reduced precision for the circuits that are affected. In the case of the spatial-derivative circuit, if the chip is placed under uniform illumination and the steady-state values of two photoreceptors V_{i-1} and V_{i+1} differ by just a few thermal voltage units ($V_T = kT/q = 25$ mV at room temperature) the output of the amplifier V_{az} will be forced to one of the two clamping voltages causing a non-zero value for the spatial-derivative current I_{SD_new} when the desired output value is zero. Using the auto-zeroing floating-gate amplifier we cancel much of the error caused by fabrication mismatch because the amplifier will counter offsets and drive the output to a known voltage level. Then, in order to obtain a balanced output transfer characteristic of the spatial-derivative circuit, we just need to choose appropriate values for V_{ref_n} and V_{ref_p} such that V_{down} and V_{up} are symmetric with respect to its steady-state value. When the spatial-derivative circuit is used in arrays it is also necessary that the difference $\Delta V_{AZ} = V_{up} - V_{down}$ matches the amount of variation expected from the statistics of the auto-zeroing amplifiers' equilibrium points. It is worth noticing that in the case of the spatial-derivative circuit, the auto-zeroing amplifier cancels the effects of offset mismatch from both photoreceptors and the spatial-derivative circuit.

3. Test Results

To test the new circuit, we fabricated a chip with an array of 26 photoreceptors connected to 25 new auto-zeroing

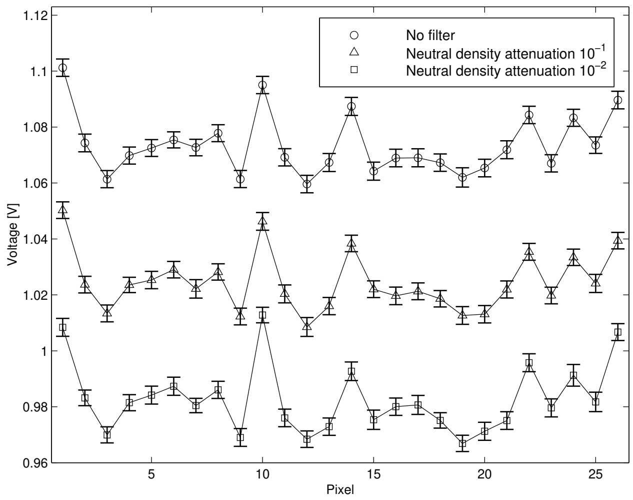

Figure 4. Voltage output of the array of photoreceptors under uniform diffuse illumination at different light intensities.

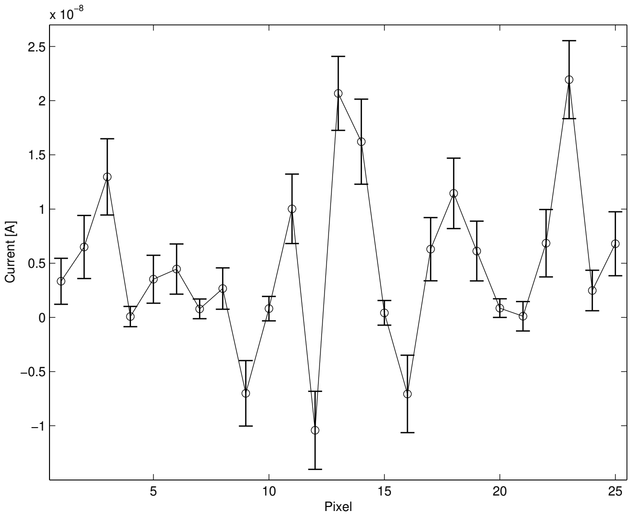

Figure 5. Output current of the old spatial-derivative circuit under uniform diffuse illumination.

spatial-derivative circuits and 25 old non-adaptive spatial-derivative circuits. We used the photoreceptor developed by Delbrück and Mead [5] that is reported in Fig. 3. To perform a fair comparison, all the transistor sizes of the differential-pair circuits and the stacked current mirrors were kept the same in the two designs. The circuit was fabricated in a 1.2 μm double-poly, double-metal, n-well CMOS process.

We performed the experiments by focusing a uniform stimulus onto the chip (i.e., a white screen illuminated by diffuse light). We measured the output of the array of photoreceptors over three orders of magnitude of uniform light conditions. Fig. 4 shows that the photoreceptor offsets are perfectly conserved across three orders of magnitude of light intensities and that there are cases where pairs of adjacent photoreceptors have a difference greater than a thermal voltage V_T. We then measured the ability of the auto-zeroing spatial-derivative circuit to adapt and remove the offsets.

In Fig. 5 we report the measurements of the non-adaptive spatial-derivative circuit. The output is not perfectly flat as we might expect for a uniform white stimulus. All the current measurements were performed using a current-sense amplifier (i.e., recorded as voltage) and the reported values were obtained by numerically converting voltage back to current. The calculated standard deviation of the current offset for this circuit was 7.8 nA which, compared to a dynamic range of 340 nA gives a “resolution” of 4.4 bits (for dynamic range we intend the difference between the positive and negative saturation values of the transfer characteristic).

In our first series of tests of the auto-zeroing spatial-derivative circuit we raised the tunneling and injection voltages and we let the array of auto-zeroing amplifiers adapt to their equilibrium point. For successful operation, the voltage range for the tunneling voltage, V_{tunn}, was between 25 and 30 V and the range for the injection voltage, V_{inj}, was from 7.5 V to 8.5 V. All the results reported here were obtained using a tunneling voltage of 26 V and an injection voltage of 7.7 V. In Fig. 6 we report the output of the auto-zeroing spatial-derivative circuit both before we started the adaptation process and after the equilibrium was reached. The effect of the auto-zeroing amplifier is a dramatic reduction of the peak value of the offset by a factor of 20. The calculated standard deviation of the offset after learning is about 1.2 nA. We can now compare in Fig. 7 the offset after the adaptation process with the constant offset of the non-adaptive circuit. The current offset of the auto-zeroing circuit is sensibly lower than the one of the non-adaptive circuit, the peak of the new circuit is about one order of magnitude lower than the the peak of the old circuit and the standard deviation ratio is about 6 to 1 in favor of the new scheme. Considering that the dynamic range of the auto-zeroing circuit was 235 nA the corresponding resolution was about 6.4 bits compared to the 4.4 bits of the non-adaptive circuit.

It is possible to obtain even better results if we use only the injection mechanism in the auto-zeroing amplifier. In this case, after setting the injection voltage to the appropriate value, the voltage V_{cntl} is increased (thus raising the floating-gate and reducing the current in the pFET transis-

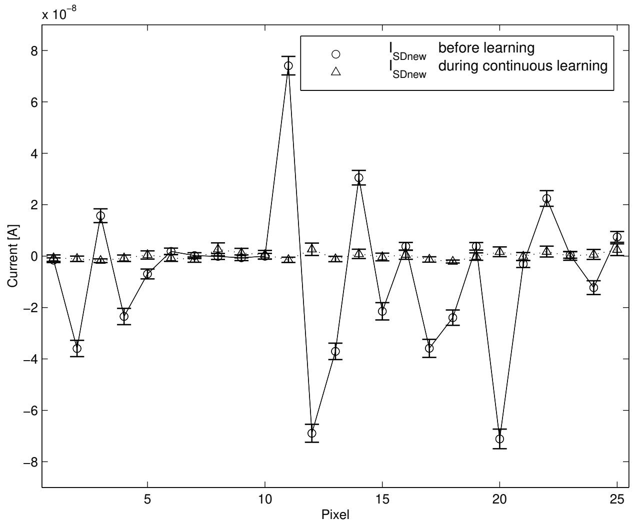

Figure 6. Comparison of the output current of the new spatial-derivative circuit before and during continuous time learning.

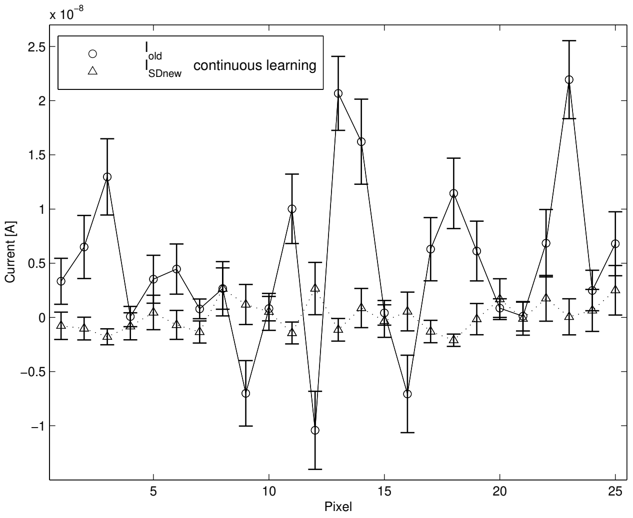

Figure 7. Comparison of the output current of the old spatial-derivative circuit and the new circuit during continuous time learning.

tor) so the output of the floating-gate amplifiers drops to a lower voltage. In this situation, the injection process becomes active and adds electrons onto the floating-gate until the pFET transistor drives the output of the amplifier high enough to turn the injection process off. With this procedure it was possible to further reduce the offsets of the spatial-derivative circuit, as shown in Fig. 8 where we compare the final offsets obtained with the two different methods. Even more significant are the benefits of this procedure if we compare the remaining offsets after this procedure, which we will call "one-time" learning, with the offset of the non-adaptive circuit in Fig. 9. The calculated standard deviation of the offset noise obtained with the one-time learning was 0.3 nA, a factor of 26 smaller than the offset noise in the non-adaptive circuit. The computed resolution for this case was 8.5 bits with a gain of four bits with respect to the non-adaptive circuit. The results for the auto-zeroing circuit were obtained setting the biases voltages V_{ref_n} and V_{ref_p} in such a way the dead-zone of the transfer characteristic was negligible with respect its linear range. Finally, in Fig. 10 we compare the output of the floating-gate amplifiers before and after the one-time learning. One drawback of this procedure is that the adaptation is performed only once and then unless tunneling is resumed the electrons are permanently stored on the floating-gates. Another important point is that, in the one-time learning case, the biasing of the pFET transistor of the floating-gate amplifier becomes critical to the correct functioning of the circuit. Temperature shifts could change the bias condition and therefore change the equilibrium point of the amplifier output. Temperature compensation could be possible by controlling the temperature dependence of the bias current in the differential-pair to match the dependence in the pFET transistor current.

Indirect evidence suggests that the reason the one-time adaptation is more accurate than the continuous learning is because the injection process is better matched across the chip than is the tunneling process. Consequently, turning off the tunneling reduces the errors.

In the injection-only case, once the pFET has largely balanced the input current, V_{ds} is reduced (output rises) until the injection shuts itself off. Since there is no tunneling current to balance, the equilibrium voltage only depends on the transistor matching. The actual gain of the injection process (which *is* a function of input current) only affects the rate at which the equilibrium is approached.

4. Discussion

In this paper we have presented a circuit for auto-zeroing a current signal as applied to a visual processing task. First, the array of offset-ridden current signals was balanced by a floating-gate auto-zeroing amplifier. Second, adjustable thresholds were introduced to prevent any remaining offsets from appearing at the output. The adaptation was achieved by adding a floating-gate amplifier and one extra circuit parameter. In comparison to previous designs, offset "noise" was reduced by more than an order of magnitude. It should be noted that the technique of offset correction *after* the differential-pair, while zeroing the final output, does not

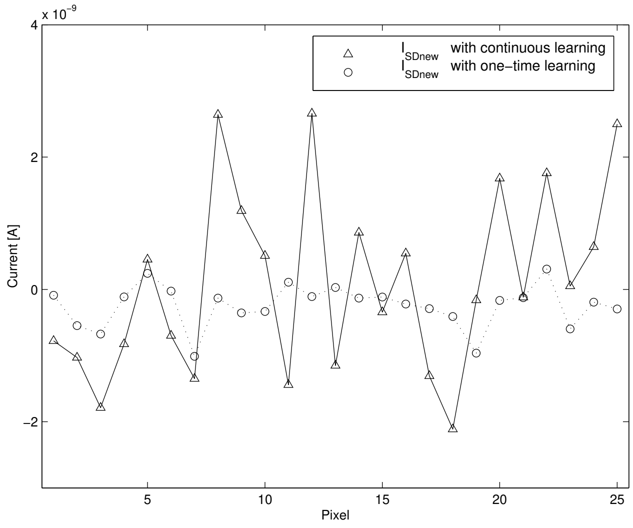

Figure 8. Comparison of the output current of the new spatial-derivative circuit during continuous time learning and after one-time learning.

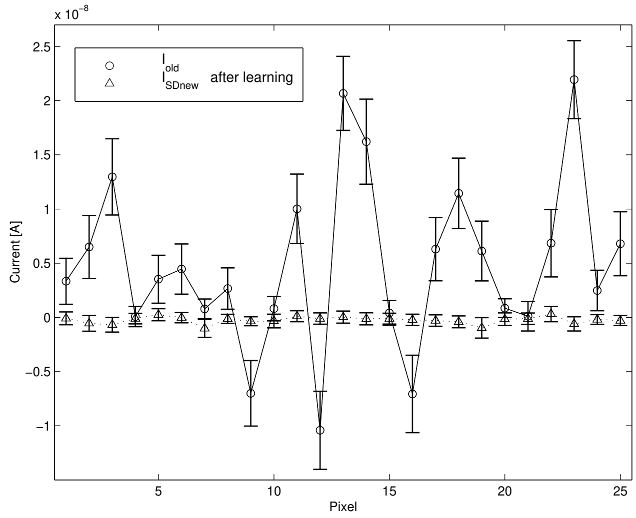

Figure 9. Comparison of the output current of the old spatial-derivative circuit and the new circuit after one-time time learning.

correct the imbalance produced by the offsets. Such an imbalance results in an asymmetrical output characteristic.

We also demonstrated two different strategies for adaptation, a one-time (injection-only) calibration routine and a continuously-adapting strategy (tunneling and injection). While the one-time calibration strategy provides a lower offset error after adaptation, we are most interested in the use of continuous calibration for systems that require very long periods of operation without intervention. As imaging systems are in operation over long periods of time and are exposed to the environment, persistent offsets from dirty optics or circuit failure can increasingly impair performance.

While one technique for reducing the effect of fabrication offsets is to increase the size of all of the transistors or improve the fabrication process, another is to make the circuit layout very small and utilize an adaptive system. In the chip we presented, all of the transistors were $6\lambda \times 6\lambda$, leaving room for further reduction in layout area in future designs. While both approaches to offset reduction are valid, the adaptive approach is attractive due to the potential for ignoring bad pixels and its ability to compensate for unforeseen changes in the system over time.

It should be noted that the work presented here is different from other work in the literature [6, 1], in that the sensor's output is not an image to be used by a downstream computer, rather it is intended to be used in a fully-integrated computational sensor [13] or in a larger system that requires pre-processed data. It is for this reason that adaptive photoreceptors are used and the spatial-derivative is used to calibrate the system rather than the image intensity. This adaptation strategy, however, does make the assumption that the visual world the sensor experiences has zero-mean spatial-derivative statistics over a time-interval comparable to the learning time-constant. For an autonomous, mobile visual system viewing natural scenes, the zero-mean assumption of the continuous adaptation approach is likely to be reasonable.

The brain has long been an inspiration to engineers for reasons of both computational ability and adaptability, however, attempts to mimic even the smallest portions of it have fallen surprisingly short. While early attempts to build neural circuits used small numbers of discrete components, recent approaches have utilized VLSI technology. Neuromorphic analog VLSI chips [8], while space and power efficient, have often been criticized for their lack of precision and lack of realistic memory structures. The recent surge in development of non-volatile analog parameter storage on silicon and the rapid growth of knowledge in neuroscience (where memory and computation are inextricably intermingled), however, have made neuromorphic analog VLSI systems a viable technology for designing tomorrow's extremely-low-power, smart sensors and systems.

5. Acknowledgments

This work was supported by a Learning and Intelligent Systems (LIS) Grant (BES-9720353) from the National Science Foundation and by the Center for Neuromorphic Systems Engineering at Caltech.

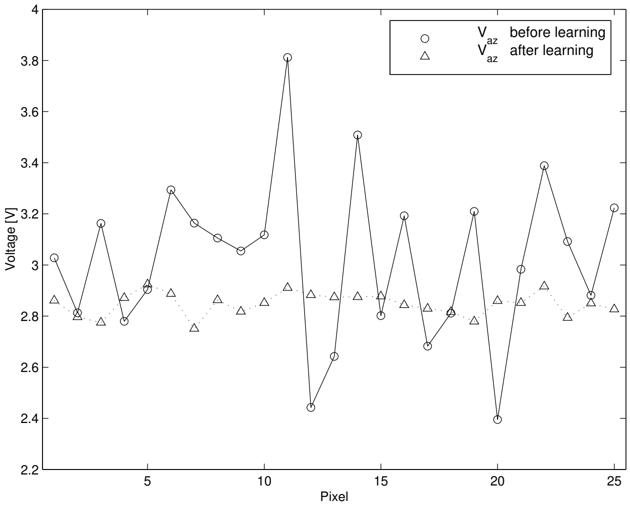

Figure 10. Comparison of the output of the amplifiers' V_{az} before and after one-time learning.

References

[1] A. Aslam-Siddiqi, W. Brockherde, M. Schanz, and B. J. Hosticka. A 128-pixel CMOS image sensor with integrated analog nonvolatile memory. *IEEE Journal of Solid-State Circuits*, 33(10):1497–1501, 1998.

[2] L. R. Carley. Trimming analog circuits using floating-gate analog MOS memory. *IEEE J. Solid State Circ.*, 24(6):1569–1575, 1989.

[3] H. Castro, S. Tam, and M. Holler. Implementation and performance of an analog non-volatile neural-network. *Analog Integrated Circuit and Signal Processing*, 4(2):97–113, 1993.

[4] G. Cauwenberghs, C. F. Neugebauer, and A. Yariv. Analysis and verification of an analog vlsi incremental outer-product learning system. *IEEE Trans. on Neural Networks*, 3(3):488–497, 1992.

[5] T. Delbrück and C. A. Mead. Photoreceptor circuit with a wide dynamic range. CNS Memo 30, California Institute of Technology, 1996.

[6] F. Devos, M. Zhang, Y. Ni, and J. F. Pone. Trimming CMOS smart imager with tunnel-effect nonvolatile analog memory. *Electronic Letters*, 29(20):1766–1767, 1993.

[7] C. Diorio, P. Hasler, B. Minch, and C. Mead. A complementary pair of four-terminal silicon synapses. *Analog Integrated Circuits and Signal Processing*, 13(1/2):153–166, 1997.

[8] R. Douglas, M. Mahowald, and C. Mead. Neuromorphic analogue VLSI. In W. M. Cowan, E. M. Shooter, C. F. Stevens, and R. F. Thompson, editors, *Annual Reviews in Neuroscience, Vol. 18*, pages 255–281. Annual Reviews Inc., Palo Alto, CA, 1995.

[9] L. A. Glasser. A UV write-enabled PROM. In H. Fuchs, editor, *Chapel Hill Conference on VLSI (1985)*, pages 61–65. Computer Science Press, Rockville, MD, 1985.

[10] R. R. Harrison, P. Hasler, and B. A. Minch. Floating-gate CMOS analog memory cell array. In *Proceedings of the 1998 IEEE ISCAS Meeting*, pages 204–207, 1998. Monterey, CA.

[11] P. Hasler, B. A. Minch, C. Diorio, and C. Mead. An autozeroing floating-gate amplifier. in press., 1999.

[12] P. Hasler, B. A. Minch, C. Diorio, and C. A. Mead. An autozeroing amplifier using pfet hot-electron injection. In *Proceedings of the 1996 IEEE ISCAS Meeting*, pages 325–328, 1996. Atlanta.

[13] T. K. Horiuchi, T. G. Morris, C. Koch, and S. P. DeWeerth. Analog VLSI circuits for attention-based visual tracking. In M. Mozer, M. Jordan, and T. Petsche, editors, *Advances in Neural Processing Systems 9*, pages 706–712. MIT Press, 1997.

[14] D. A. Kerns. *Experiments in Very Large-Scale Analog Computation.* PhD thesis, Electrical Engineering, California Institute of Technology, 1993.

[15] J. Kramer and G. Indiveri. Neuromorphic vision sensors and preprocessors in system applications. In *Advanced Focal Plane Arrays and Electronic Cameras (AFPAEC'98)*, Zürich, Switzerland, May 1998. in press.

[16] T. S. Lande, H. Ranjbar, M. Ismail, and Y. Berg. An analog floating-gate memory in a standard digital technology. In *Proc. 5th Intl. Conf. on Microelectronics for Neural Networks and Fuzzy Systems - MicroNeuro96*, pages 271–276, 1996. Feb. 12-14, 1996, Lausanne, Switzerland, IEEE Computer Society Press, Los Alamitos, CA.

[17] J. Lazzaro, J. Wawrzynek, and A. Kramer. Systems technologies for silicon auditory models. *IEEE Micro*, 14(3):7–15, 1994.

[18] M. Lenzlinger and E. H. Snow. Fowler-nordheim tunneling into thermally grown sio_2. *Journal of Applied Physics*, 40(1):278–283, 1969.

[19] C. Mead. Adaptive retina. In C. Mead and M. Ismail, editors, *Analog VLSI Implementation of Neural Systems*, pages 239–246. Kluwer Academic Publishers, Boston, MA, 1989.

[20] A. F. Murray, S. Churcher, A. Hamilton, A. J. Holmes, G. B. Jackson, H. M. Reekie, and R. J. Woodburn. Pulse stream VLSI neural networks. *IEEE Micro*, 14(3):29–39, 1994.

[21] E. Sackinger and W. Guggenbuhl. An analog trimming circuit based on a floating-gate device. *IEEE Journal of Solid State Circuits*, SC-23:1437–1440, 1988.

[22] C. K. Sin, A. Kramer, V. Hu, R. R. Chu, and P. K. Ko. EEPROM as an analog storage device, with particular applications in neural networks. *IEEE Trans. on Electron Devices*, 39(6):1410–1419, 1992.