Phased Array Systems in Silicon

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ABSTRACT

Phased array systems, a special case of MIMO systems, take advantage of spatial directivity and array gain to increase spectral efficiency. Implementing a phased array system at high frequency in a commercial silicon process technology presents several challenges. This article focuses on the architectural and circuit-level trade-offs involved in the design of the first silicon-based fully integrated phased array system operating at 24 GHz. The details of some of the important circuit building blocks are also discussed. The measured results demonstrate the feasibility of using integrated phased arrays for wireless communication and vehicular radar applications at 24 GHz.

INTRODUCTION

Space is the next frontier for wireless communications as networks evolve to meet higher data rate and quality of service requirements. It is becoming increasingly difficult to achieve further improvements in spectral efficiency using pure time and frequency domain methods. Interestingly, there are spatial methods that can be used to improve data rates without the dreaded increase in bandwidth. Therefore, exploiting the spatial dimension for improving spectral efficiency is an area of rapidly increasing interest. Multiple antenna systems have been identified as one means of effectively increasing spectral efficiency by taking advantage of spatial directivity and diversity, as well as array gain via the multipath scattering present in most indoor and urban environments. The antenna size and the spacing between the elements are inversely proportional to the frequency. This inspires a move to higher frequencies to leverage spatial processing techniques, as multiple antenna systems can be made physically smaller. In addition, larger bandwidths are available at higher frequencies. Small-sized highly integrated low-power multiple-antenna systems can also be used for ranging and sensing applications such as radar.

In 2002 the FCC released the guidelines for operation of wireless devices at 24 GHz [1]. It permits fixed point-to-point wireless communication in the 24–24.25 GHz band subject to limitations on the transmitted power and directionality of the transmitter. The FCC has also opened up 7 GHz of bandwidth from 22–29 GHz for vehic-ular radar applications. Short-range vehicular radar systems are expected to play an important role in collision prevention and driver assistance in the future (e.g., assisted parking and blind spot detection). The 24 GHz band already has users, particularly in the fields of remote sensing and astronomy. Interestingly, in addition to specifications limiting transmitted power to different levels at different frequencies (i.e., the spectral emissions mask), there is a spatial specification as well. The phased array approach provides a natural solution to these challenges.
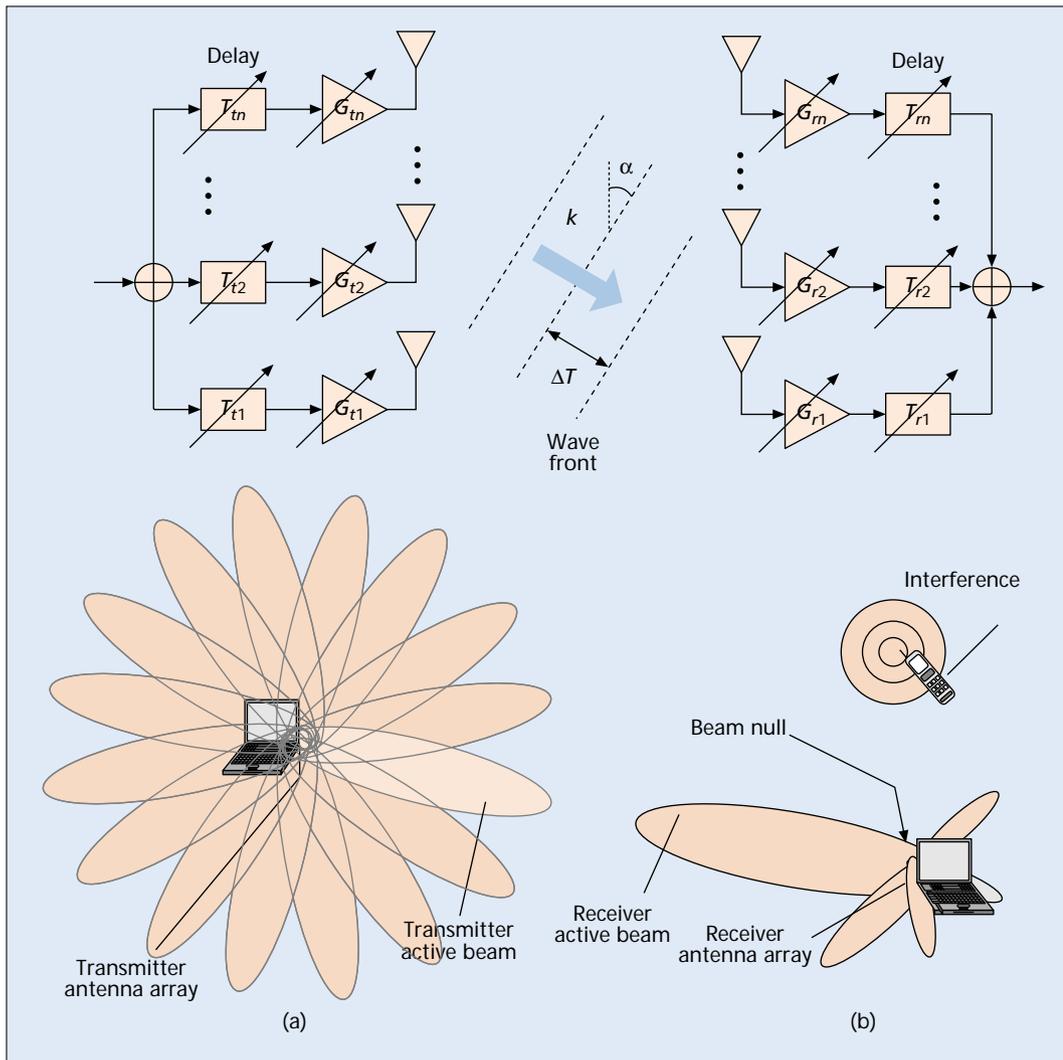
As opposed to a fixed directional antenna system, phased arrays allow the beam to be steered electronically in different directions, enabling accurate velocity and location estimation of objects that appear within the narrow beam. In addition to vehicular radar applications, such object and motion sensors could potentially be useful in many other applications.

Taking advantage of silicon integration, spatial processing, and large available bandwidth will make *gigabit wireless LAN* and *low-cost versatile vehicular radar* a reality. In this article we discuss the integration issues for such a multiple-antenna system in silicon and demonstrate the first silicon-based fully integrated phased array receiver at 24 GHz.

PHASED ARRAY: A SPECIAL CASE OF MIMO SYSTEMS

Antenna arrays can be implemented on either the transmit side (multiple-input single-output: MISO), the receive side (single-input multiple-output: SIMO), or both ends (multiple-input multiple-output: MIMO).

In MIMO systems, prevalent multipath scattering increases channel capacity by creating stochastically independent channels between each of the transmitter and receiver antenna array elements. For example, if there are n elements on each of the transmitter and receiver sides, scattering effectively creates n parallel channels between the transmitter and the receiver [2, 3]. The theoretically promised linear increase in capacity is never fully realized in practice because the effective channels created are not completely independent. Although the improvement factor is often less than n, practical demonstrations of MIMO systems have shown

■ Figure 1. *(a) A phased array transmitter focuses the beam at a desired angle; b) a phased array receiver focuses on the desired signal while it attenuates an interferer coming from another direction.*

that substantial increase in channel capacity is possible (20–40 b/s/Hz for an 8-transmitter 12-receiver MIMO system [4]). However, the spacing between antennas has proven to be a practical barrier to the implementation of multiple antenna arrays for mobile applications at frequencies in the low gigahertz range (e.g., $\lambda \sim 15$ cm @ 2 GHz). The size constraints mandate the move to higher frequencies.

Phased array, historically employed in radar and radio astronomy applications, is a class of multiple antenna systems. It can form beams and nulls in desired directions by controlling the time delay and gain of the signal in each path independently. The array gain and spatial directivity achieved in a phased array system provide a logarithmic increase in channel capacity with an increase in the number of elements in the phased array due to the logarithmic dependence of channel capacity on signal-to-noise ratio (SNR). The benefits provided by the beam directionality of a phased array transmitter, shown in Fig. 1a, can be likened to the advantages of a narrow flashlight beam over the omnidirectional incandescent bulb. In a flashlight, most of the light energy is focused only in the desired direction,

as opposed to a bulb's indiscriminate illumination in all directions. Thus, to obtain a given power intensity at the destination, much lower power needs to be radiated at the source for a directional beam, as compared to an omnidirectional one. At the same time, less interference is generated via this collimation of power.

Similarly, in phased array receivers, signals from multiple antennas are delayed individually to compensate for the path length difference in that direction and are then added coherently. As shown in Fig. 1b, phased array systems are capable of amplifying signals coming from one direction while attenuating interfering signals from other angles.

A phased array increases the effective SNR at the output of the receiver, thereby improving its sensitivity. With sufficient antenna spacing, the black-body radiation noise of each antenna is uncorrelated to the noise of the other antennas in the array. Furthermore, the receiver noise sources in each signal path before power combining are independent. As a result, the time-delayed signals from the antenna array add in amplitude (coherently) while the noise adds in power (incoherently). This results in a $10\log_{10}(n)$

[dB] improvement in the SNR at the output of the n element phased array receiver.

The improvement in the SNR at the target phased array receiver and reduction in the level of interference generated for other users because of the directionality of a phased array transmitter lead to substantially higher data rates and frequency reuse ratios, while lowering the power requirements of the transmitter. Although there are more active elements in a phased array system, its power consumption is still lower than that of single-path systems for the same data rate.

DELAYED ARRAY OR PHASED ARRAY?

Phased array is perhaps a misnomer for these systems given that true time delay, and not phase shift, is required in each path for coherent addition of signals. As shown in Fig. 1b, when a plane electromagnetic wave arrives at an antenna array at an angle of α with respect to the normal to the array plane, the signal is received by each antenna at a different time due to the difference in propagation path length. In general, an angle-dependent time delay in each path at the receiver can compensate for the arrival delay and effectively "listen" to a desired direction. In a one-dimensional array, the angle of incidence, α, is related to the delay difference of two adjacent elements, ΔT, the spacing of two adjacent antennas, D, and the speed of light, c, via

$$D.\sin(\alpha) = c.\Delta T. \qquad (1)$$

The beam forming works independent of the frequency and bandwidth of the signal with ideal delay elements following each antenna, as shown in Fig 1b. Unfortunately, there are practical challenges to implement such broadband delay elements in the radio frequency (RF) signal path, such as signal attenuation, noise, and linearity degradation, as well as signal dispersion. Fortunately, in many practical applications, particularly in wireless communications, the bandwidth of interest is a small fraction of the center frequency; hence, a uniform delay (linear phase) is only required over this narrow bandwidth. A simple way to realize the delay is to approximate it with a constant phase shift. This aligns the carrier phase of different paths. However, the modulating signal is not delayed appropriately, leading to some dispersion in the demodulated signal. A higher modulation-bandwidth-to-carrier-frequency ratio results in larger signal dispersion, manifested by the spreading of the constellation points. This distortion results in an increased bit error rate (BER) in wireless communication systems and in a reduced radial resolution in radar applications.

The effect of using phase shifting instead of true time delay compensation can be seen in the simulation results shown in Figs. 2a and 2b. They show the simulated constellation of the received signal (without noise) for an eight-element phased array receiver at bit rates of 1 Gb/s and 10 Gb/s at the worst case incident angle of 90° with respect to normal, using a quaternary phase shift keying (QPSK) binary-coded complex

modulation scheme with a carrier frequency of 24 GHz. The antenna elements are placed λ/2 = 2.5 mm apart in a one-dimensional array of eight. Receiver noise was not simulated to fully expose the limitations of the constant phase approximation. A square-root raised cosine filter with a rolloff factor, β, of 0.5 is used at both transmitter and receiver for pulse shaping. A β of 0.5 corresponds to a spectral efficiency of 1.33 b/s/Hz.

As the direction of the beam becomes more oblique, the delay between the paths increases, and so does the error introduced by constant phase shift approximation. The constellation spreading is a function of the signal's angle of incidence, ratio of signal bandwidth to carrier frequency, and pulse shaping used. Error vector magnitude (EVM) is a measure of constellation spreading and is the root mean squared difference between the perfectly demodulated and measured signals. The EVM of the received signal was calculated for different signal bandwidths and angles of incidence, and the results are plotted in Fig. 2c, assuming continuous phase control at the local oscillator (LO). As can be seen, for a carrier of 24 GHz, even for bit rates as high as 1 Gb/s and an incidence angle of 90° (worst case), EVM is lower than 2 percent, so the signal integrity is maintained without additional equalization. Given the 250 MHz wireless communication bandwidth, phase shift of the carrier at 24 GHz (a BW/f_{center} close to a factor of 0.01) is a very good approximation for the delay and sufficient for reliable communication. However, for broadband communication or to achieve fine radial resolutions in pulsed phased array radars, it may be necessary to use a better approximation of the actual delay rather than constant phase shift.

A phase shifter implementation in which the phase can be varied in discrete steps only introduces additional dispersion for certain angles of incidence, as shown in Fig. 2d. For example, in the phased array receiver described in this article, 16 discrete phases of LO are interpolated to obtain 32 discrete phases (5-bit resolution) that are then used to compensate the narrowband phase shift of the carrier frequency in each path. This discrete method can only precisely compensate the carrier phase shift at 32 angles of incidence between –90° and +90°. For all other angles, the signal constellation in each received path is rotated by an angle equal to the phase quantization error, which depends on the exact phase shift necessary in each path for the given angle of incidence. Since the constellation for each receiver path is rotated differently, there will be interference between the in-phase (I) and quadrature-phase (Q) demodulated channels.

Figure 2d plots the simulated EVM as a function of the angle of incidence when discrete phase shifts are used at the receiver for 8, 16, and 32 available phases, as well as a continuous version (Fig. 2c). The signal has a bandwidth of 7.5 GHz, and all other simulation parameters are identical to those used in Figs. 2a and 2b. Using a 5-bit phase shifting scheme with phase steps of 5.6° causes a peak EVM of 12 percent at an incidence angle of 75°, which is only 1.14 times larger than the peak EVM generated if an
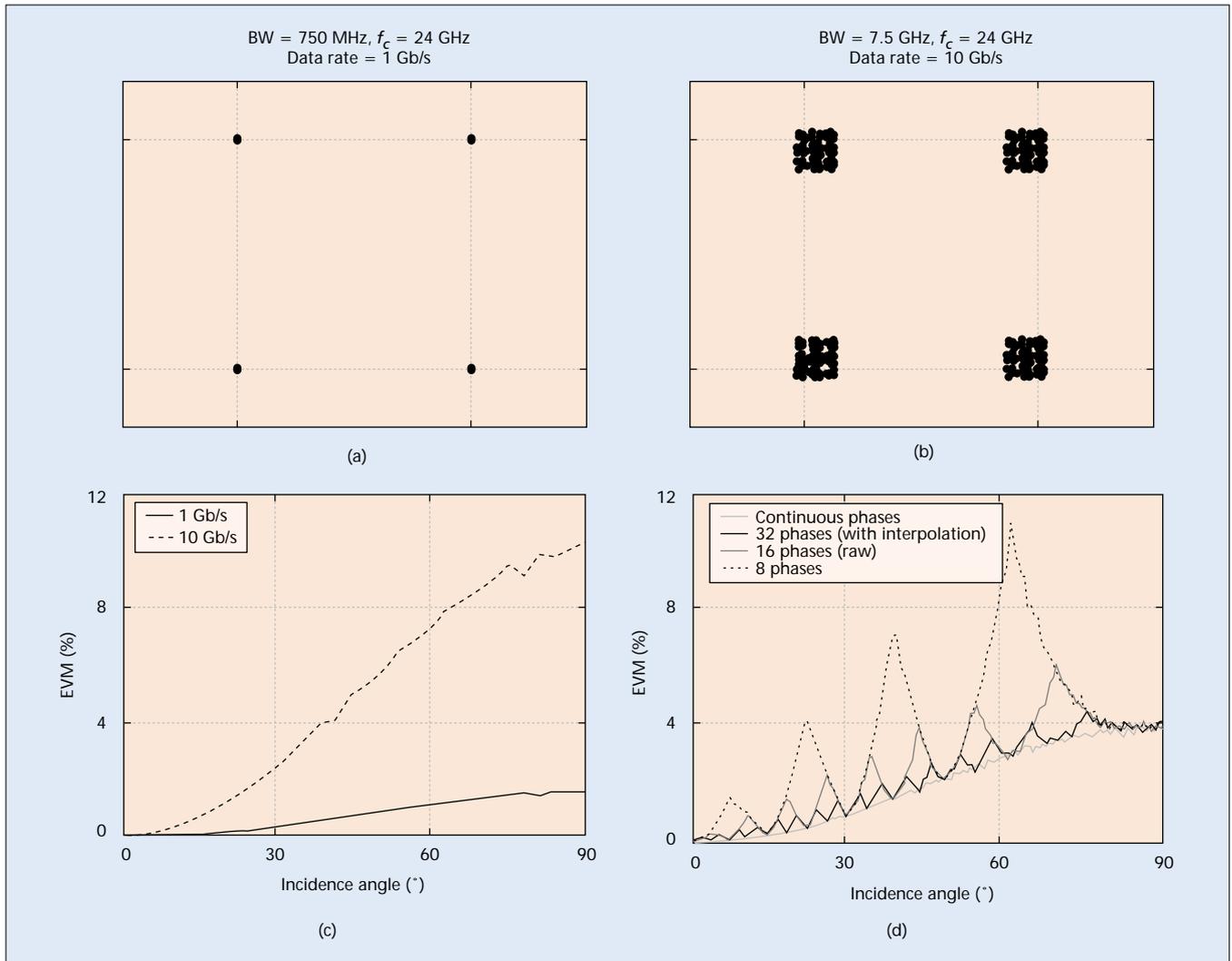
■ Figure 2. *The simulated constellation for a QPSK modulation scheme at a carrier frequency of 24 GHz for bandwidths of: a) 750 MHz and b) 7.5 GHz; c) EVM for the two constellation in Fig. 1a and b vs. angle of incidence; d) the effect of phase quantization error for 3-bit, 4-bit, and 5-bit resolution at different beam angles compared to continuous LO phase resolution.*

LO with continuous phase shifting were available. In the latter case, the peak naturally happens at an incidence angle of 90°, which corresponds to the largest time delay between antennas. It is evident from Fig. 2d that a 3-bit phase shifting resolution results in a much larger EVM relative to a 5-bit phase resolution. If a 3-bit phase shifting scheme with 45° phase steps were used, this peak would occur at an incidence angle of 60°, with a peak EVM value 180 percent higher than the peak EVM value for a continuous version. The relative degradation due to a coarse phase resolution increases for higher bandwidth-to-carrier ratios.

SILICON IMPLEMENTATION

Advances in silicon process technologies for integrated circuits have resulted in very fast transistors with cutoff (unity current gain) frequencies above 100 GHz. However, transistor speed is only one of the parameters affecting system operation. Additional constraints imposed by the low breakdown voltages, losses of integrated passive elements, low power budget, as well as cost

and area constraints have important bearings on overall system performance. Therefore, the architecture of the phased array system has to be chosen carefully to ensure repeatability and reliability.

Ideally, broadband variable delays are needed to make the signals from all the paths coherent before they are combined. Such a variable delay, if implemented in the signal path at RF, can reduce power consumption. The gain of the delay stage should be independent of the delay, as a change in amplitude with different delays will lead to distortion when the signals are combined. Thus, the delay element should have large and accurate variations in delay (0–140 ps @ 24 GHz for an 8-element array, with spacing of λ/2 between antennas) and low loss. Such delay elements are quite challenging to implement.

As mentioned before, for narrowband signals the delay can be approximated by a phase shift. Figure 3 shows the different stages at which the phase shift can be implemented in a simple two-element phased array receiver example. In the signal path, the phase shift can be provided at RF (Fig. 3a), intermediate frequency (IF)/base-
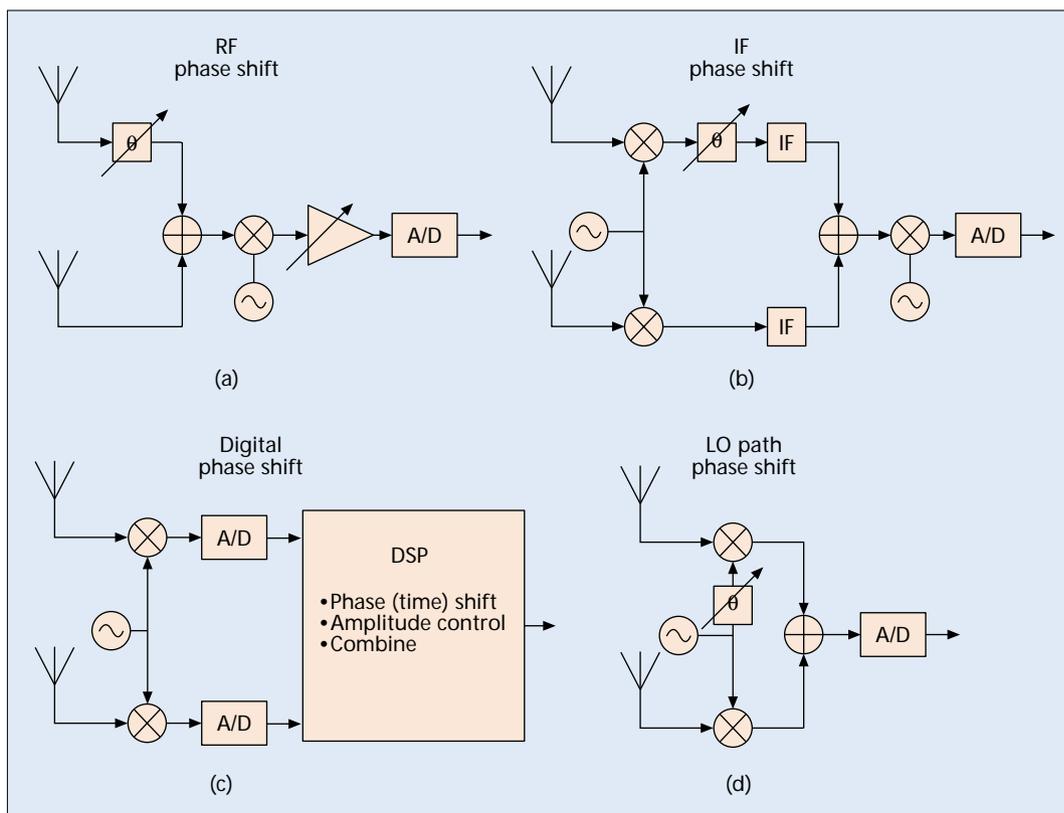
■ **Figure 3.** *Different architectures for implementing phase shift: a) RF phase shifting; b) IF phase shifting; c) digital phase shifting; d) LO path phase shifting.*

band (Fig. 3b), or digitally (Fig. 3c). Equivalently, the phase shift can also be provided by downconverting the signal in each path with a phase shifted LO signal (Fig. 3d). The architecture selection is accompanied, as always, by certain trade-offs in power consumption, capacity, silicon area, and system reliability.

An architecture with controllable phase shifters in each RF path and signal combining at RF has advantages with respect to lower power consumption as there only needs to be one IF/baseband stage (Fig. 3a). Additionally, since all the interferers are nulled out at RF, the linearity requirements of the IF/baseband stage are reduced. If the signal is delayed by time, τ, the carrier at frequency f_c undergoes a phase shift equal to $2\pi f_c \tau$. Since a phase shift of θ is equivalent to a phase shift of $2\pi + \theta$, the phase shifter only needs to provide phase shifts between 0 and 2π. Again, the gain should be constant across phase shifts, and the phase shifter should have low loss. There have been some phase shifters reported at lower frequencies, but their size and performance do not make them suitable for an integrated phased array system. The study of high-frequency phase shifters is an active area of research [5].

While it is possible to utilize phase shifters in the IF stage, they increase power consumption because in an *n* element receiver, there will have to be *n* downconversion mixers before the phase shifters (Fig. 3b). Since the value and therefore the size of passive components (i.e., inductors, capacitors, and transmission lines) needed to provide phase shift is inversely proportional to

the frequency, implementing the phase shifters at IF will increase system area.

Another architectural choice is to do away with analog phase shifting entirely, opting for baseband digital delay (Fig. 3c). This increases the flexibility of the system, as it can now be configured as both a phased array or a MIMO system depending on the application. However, this advantage is offset by the high power consumption of such a system, which is essentially equivalent to *n* receivers operating in parallel while sharing no blocks except the frequency synthesizer. Also, it places tough performance criteria on the analog-to-digital (A/D) converter in order to provide accurate delay. Additionally, as the interferers are still present, the linearity and dynamic range of the IF stage and A/D converter will also have to be substantially higher, leading to higher power consumption. As an illustration, imagine a digital array of eight receivers where each has an 8-bit A/D converter that samples the signal with a 100 MHz channel bandwidth at twice the Nyquist rate. These numbers are reasonable for such a system. The baseband data-rate of the whole system can be calculated as 76.8 Gb/s. This requires a high-speed interface, and a power-hungry and expensive signal processing core.

As compared to a signal path implementation at RF, IF, analog baseband, or digital signal processing, a phase shifter in the LO stage is relatively easier to implement (Fig. 3d). Since the downconversion mixers have their best performance when they are hard-driven, the LO stages should preferably be operated in saturation.
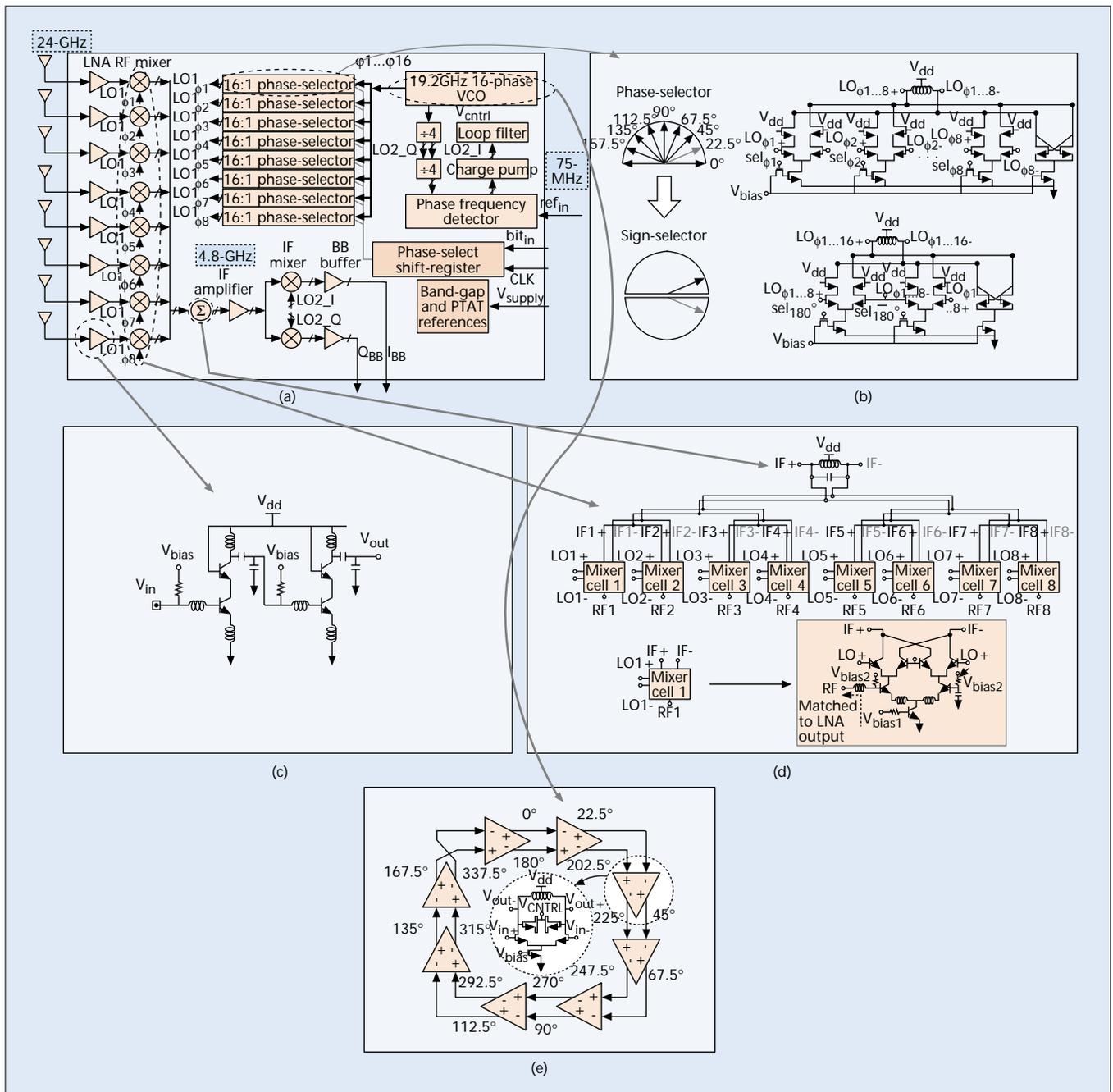
■ Figure 4. *a) The block diagram of the eight-path phased array receiver implemented in silicon; b) phase selection circuitry; c) 24 GHz low noise amplifier; d) RF mixer and combiner; e) multiple-phase LO.*

Noting that the output of the VCO has constant amplitude as well, the amplitude and phase variations can be completely decoupled. Therefore, each path will have a constant gain irrespective of phase shift. Since in this architecture there is only one IF amplifier followed by two (I and Q) A/D converters, the power consumption is reduced from that of an IF phase shift architecture.

A 24 GHz PHASED ARRAY RECEIVER

The trade-offs described above led to an LO-phase-shifting-based phased array receiver. The block diagram and circuit schematics of the eight-element 24 GHz phased array receiver are shown in Fig. 4. In order to avoid the dc offset and other problems associated with a homodyne receiver, a two-stage heterodyne radio architecture was adopted (Fig. 4a). The two LO frequencies were chosen to be 19.2 GHz and 4.8 GHz. With this choice, both LO frequencies can be generated in one frequency synthesizer phase-locked loop with the use of a frequency divide-by-four block.

The phased array receiver has been designed and fabricated in a IBM 7HP SiGe BiCMOS process with maximum cutoff frequency, f_T, of 120 GHz for bipolar devices and minimum channel length of 0.18 μm for complementary metal oxide semiconductor (CMOS) transistors [6]. The process offers five metal layers. As the top
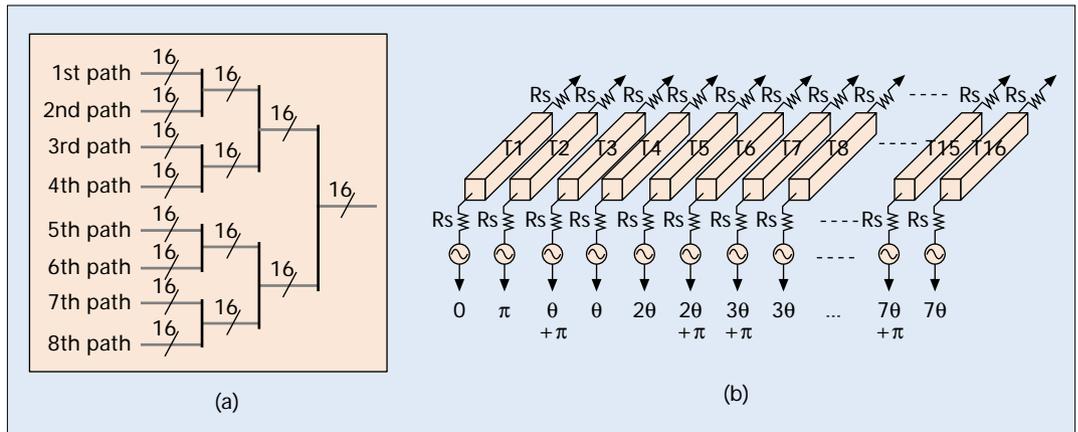
■ **Figure 5.** *a) Tree structure for LO phase distribution; b) order of angles in the LO distribution network.*

two metal layers are thicker, they are used for on-chip routing of high-frequency signals and implementing on-chip spiral inductors. The receiver can be broadly divided into circuits in the signal path, and circuits for LO generation and phase selection. It is important to note that while this architecture is more suitable for beamforming, the circuits in themselves are still applicable to a full *n*-element MIMO receiver.

SIGNAL PATH

Each RF front-end consists of a two-stage low noise amplifier (LNA) (Fig. 4c) and a Gilbert-type mixer. The outputs of all eight mixers are combined in the current domain and terminated with a tuned load at the IF frequency, as shown in Fig. 4d. Impedance matching networks were implemented on-chip between RF stages to maximize power transfer. More information on the design of the front-end can be found in [7]. The image frequency of the first downconversion is located at 14.4 GHz. The signals at this frequency are attenuated by the narrowband transfer function of the front-end (i.e., antenna and LNA). The cascaded LNA stages alone provide around 35 dB of image rejection. Since the transmissions around the image frequency band (14.4 GHz) are mainly low-power satellite signals, no image rejection architecture is used at the RF stage. The final downconversion to baseband is done by a pair of quadrature mixers. The divide-by-four block that is used to generate the second LO naturally produces in-phase and quadrature-phase signals to drive these mixers.

LO MULTIPLE PHASE GENERATION

A single oscillator core is used to generate multiple phases of a single frequency. Multiple phases can be generated by extracting signals from equidistant nodes of an oscillator loop, as shown in Fig. 4e. A phase shift of 360° is maintained across the oscillator feedback loop in order to maintain stable oscillation. In our design, a ring comprising 8 fully-differential CMOS amplifiers forms the 19 GHz VCO capable of generating 16 phases. As the structure is differential, flipping one of the connections halves the number of amplifying stages in the ring from 16 to 8. Each amplifier produces a phase shift of 22.5° phase shift at 19 GHz (Fig. 4e). It can be shown

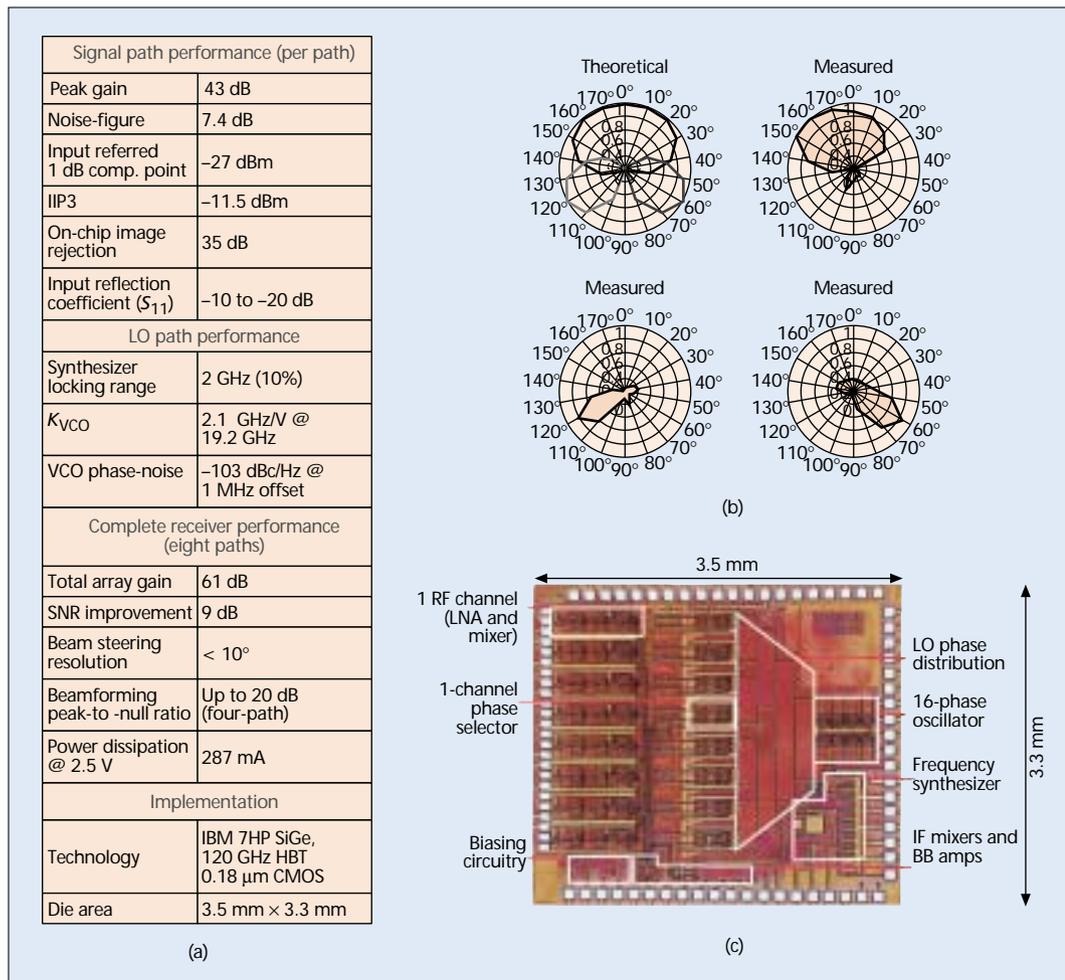that in order to achieve a 22.5° phase shift, each amplifier should be tuned close to the oscillation frequency. Each of the designed amplifier stages draws less than 3.2 mA from a 2.5 V supply, resulting in total power consumption of 63 mW for the oscillator.

PHASE DISTRIBUTION AND SELECTION

The oscillator core generates 16 discrete phases that are used to control the phase of each path. The 16 generated phases of the VCO are fed into the phase selection circuitry of each path in a symmetric manner to ensure that the delays of the traces connecting these blocks are equal for all the oscillator phases. The phase selectors (Fig. 4b) can be digitally controlled to interpolate between two adjacent phases; thus generating 32 equally spaced LO phases. However, there may be amplitude and phase variations in each path. These variations are because of the mutual coupling and the small mismatches in delivering the LO phases to different receiver paths. For example, based on electromagnetic simulations, the wavelength of a 19 GHz signal in a typical microstrip line in the silicon technology used is about 6 mm; hence, a length difference of 40 μm corresponds to a phase difference of 2.5°. The phase and amplitude mismatches among various paths deteriorate the side lobe attenuation or equivalently degrade the ability of the phased array to reject interfering signals.

Figure 5a shows the symmetric tree structure used to transfer all 16 phases of the LO signals to the phase selection circuitry of each path with minimal mismatch between the paths. Figure 5b shows the ordering of the phases in the LO phase distribution network. It was determined that this ordering minimized the coupling induced mismatch. In order to reduce the loss, the top two metal layers in the process were used for distributing multiple LO phases. The minimum spacing between lines in these thicker metal layers is around 5 μm; therefore, the phase distribution network occupies a significant fraction of the chip area. The large size of the LO phase distribution network, and sensitivity to mismatch and coupling is a disadvantage of this architecture.

The phase selectors in each path provide the appropriate phase of the LO to the correspond-

Signal path performance (per path)	
Peak gain	43 dB
Noise-figure	7.4 dB
Input referred 1 dB comp. point	–27 dBm
IIP3	–11.5 dBm
On-chip image rejection	35 dB
Input reflection coefficient (S_{11})	–10 to –20 dB
LO path performance	
Synthesizer locking range	2 GHz (10%)
K_{VCO}	2.1 GHz/V @ 19.2 GHz
VCO phase-noise	–103 dBc/Hz @ 1 MHz offset
Complete receiver performance (eight paths)	
Total array gain	61 dB
SNR improvement	9 dB
Beam steering resolution	< 10°
Beamforming peak-to -null ratio	Up to 20 dB (four-path)
Power dissipation @ 2.5 V	287 mA
Implementation	
Technology	IBM 7HP SiGe, 120 GHz HBT 0.18 μm CMOS
Die area	3.5 mm × 3.3 mm

(a)

(b)

(c)

■ **Figure 6.** *a) Measured receiver performance summary; b) four-element theoretical and measured array patterns; and c) die photo of the eight-path fully integrated receiver implemented in silicon.*

ing RF mixer. The phase selectors are equivalent to analog multiplexers, and the LO phase for each path is controlled irrespective of the phase of the other paths. The phase selection data is serially loaded to an on-chip shift register using a digital serial interface.

The phase selector in each receiver path has access to all 16 phases of the LO via the 8 differential LO outputs. In order to minimize the phase-selection circuit complexity, the appropriate phase of the local oscillator for each path is selected in two steps. Initially, an array of 8 differential pairs with switchable current sources and a shared tuned load are used to select one of the 8 differential outputs of oscillator (Fig. 4b).

This topology accommodates phase interpolation using the appropriate digital control word. When two (or more) phase branches are selected by turning on the tail current sources associated with those phases, the current addition at the output results in interpolation between the two (or more) selected phases, as shown in Fig. 4b. By interpolating two adjacent phases, 32 equally spaced phases (5-bit resolution) can be generated.

The next stage consists of two cross-coupled differential pairs. This stage can provide either a 0° or 180° phase shift (i.e., the output is either the input or its inverted version). The two stages of phase selection result in complete access to all LO phases. Notably, the two stages are designed to provide high gain in order to restore the amplitude of the LO signal that is attenuated because of the loss of the distribution network and mismatch between components.

MEASURED PERFORMANCE

The results of the measurements performed on the receiver have been summarized in Fig. 6a. The overall noise figure of the system is 7.4 dB over a bandwidth of 250 MHz. The array function improves the output signal power by 18 dB while increasing the noise power only by 9 dB, resulting in an improvement of 9 dB in the output SNR compared to the SNR at the antenna for eight elements. Therefore, the SNR at the baseband is about 1.6 dB *better* than the SNR at each antenna. Figure 6b shows the measured beam formed when signals from four paths are added after phase shifting for three different angles and compares it to the theoretically calculated patterns. Due to the inherent agility of the phase selection blocks, the phase configuration can be switched at a speed on the order of the logic switching time. Signal combining in the current domain results in an increase in the signal power of 18 dB. Thus. the eight-element

array exhibits a total gain of 61 dB and has a beamforming peak-to-null ratio of 20 dB. It draws a constant 287 mA from a 2.5 V supply, irrespective of beam direction.

A die micrograph of the fully integrated 24 GHz phased array receiver is shown in Fig. 6c. The complete receiver occupies 3.3×3.5 mm^2 of silicon area. As mentioned before, the phase distribution network occupies a significant portion of the chip area. Except for eight receiver inputs at 24 GHz, differential in-phase and quadrature-phase baseband outputs (four pads), and phase locked loop (PLL) reference (one pad), all the other pads are either ground or biasing/control voltage pads, demonstrating a fully integrated phased array receiver in silicon for the first time.

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BIOGRAPHIES

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Abbas Komijani received B.S. and M.S. degrees in electronics engineering from Sharif University of Technology. He is currently working toward a Ph.D. degree at Caltech. His research interests include high-frequency power amplifiers, wireless transceivers, phased array architectures, and delta-sigma data converters. He was a design engineer with Emad Semiconductors, where he worked on CMOS chipsets for voiceband applications from 1997 to 1999. He was a design engineer with Valence Semiconductors, where he worked on data converters for VoIP applications from 1999 to 2000.

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XIANG GUAN received a B. S. degree in electrical engineering from Tsinghua University and an M. Eng. degree in electrical engineering from the National University of Singapore. He is currently working toward a Ph.D. degree at Caltech. From 1996 to 1997 he was a research assistant at the Integrated Circuits Group, Instituto Superior Tecnico, Lisbon, Portugal, involved in the development of a data acquisition chip for electrocardiogram remote monitoring devices. In summer 2003 he was a co-op researcher at the IBM Thomas J. Watson Research Center, Yorktown Heights, New York.

HOSSEIN HASHEMI received B.S. and M.S. degrees in electronics engineering from Sharif University of Technology. He received a second M.S. and a Ph.D. in electrical engineering from Caltech. He joined the Department of Electrical Engineering — Electrophysics at the University of Southern California in 2003 as an assistant professor, where the core of his research constitutes the study of the fundamentals of high-speed and RF communication circuits and systems, along with integrated implementations. He has been a recipient of the Outstanding Accomplishment Award from the von Brimer foundation in 2000, Outstanding Student Designer Award from Analog Devices in 2001, and an Intel fellowship in 2002. He is an Associate Editor of *IEEE Transactions on Circuits and Systems, Part II*.