```
Pixel number: 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22
Input (3 bit): 06 06 07 06 06 06 06 06 06 05 05 05 04 04 04 04 03 03 03 03 03 03
Non-FZP DPCM: 0  0  10 11 0  0  0  0  0  11 0  0  11 0  0  0  11 0  0  0  0  0   (28 bits)
Reconstruction: same as input (not always the case)
FZP(2) DPCM:     0  10 11    0     0     0  11    0  11    0  11    0     0        (18 bits)
Reconstruction: 06 06 07 06 06 06 06 06 06 06 05 05 05 04 04 04 03 03 03 03 03 03
                      --       --
                Errors Have Occurred Here                                  573/4
```

Fig. 4 *Examples of FZP(z) and standard DPCM prediction*

of 2) and a normal DPCM coder using previous pixel prediction ($\hat{S}_n = 1{\cdot}0 + D$).

In the case of normal (non-FZP) DPCM, whenever the current pixel is less than the previous one the output will be -1 (11 in the Huffman code). With FPZ DPCM the -1 (or $+$) may be delayed until an even number of zeros (in the case of FZP(2)) has been previously output. In Fig. 4 it is seen that a '-1' has been delayed from pixel number 10 to number 11, and from number 13 to number 14. The '-1' at pixel number 17 has not however been delayed because it has been preceded by a pair of zeros. This illustrates the ability of FZP to recover from abnormal forced behaviour. What took 26 bits to transmit using Huffman encoded standard DPCM was reduced to 18 bits by using FZP DPCM. The cost has been the incorrect reconstruction of two of the input samples.

Table 1 OUTPUT BIT/PIXEL AGAINST FZP PADDING VALUE

FZP padding value	Bit/pixel in output
1	1·21
2	0·71
3	0·58
4	0·43
5	0·39
6	0·36

Result: When Huffman encoded noisy DPCM is combined with FZP, very significant compression can be achieved. Table 1 indicates the number of bits per pixel in an output image as the padding value is incresed. A 3 bit dither image is used as input. The noisy predictor employs a dither multiplier of 1·3. However as the padding value is increased the distortion in the reconstructed image becomes more significant. A padding value of 3 represents a good compromise between minimal subjective distortion and maximum compression. The image of Fig. 5 was compressed to 0·58 bit/pixel using noisy FZP(3). Its quality should be compared to that of Fig. 3, a 3 bit/pixel image.

573/5

Fig. 5 *Noisy FZP(3) compression at 0·58 bit/pixel*

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FABRICATION OF LOW THRESHOLD VOLTAGE MICROLASERS

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Indexing terms: Lasers, Semiconductor lasers

Vertical cavity surface emitting lasers (VCSELs) with threshold voltages of 1·7 V have been fabricated. The resistance-area product in these new vertical cavity lasers is comparable to that of edge-emitting lasers, and threshold currents as low as 3 mA have been measured. Molecular beam epitaxy was used to grow *n*-type mirrors, a quantum well active region, and a heavily Be-doped *p*-contact. After contact definition and alloying, passive high-reflectivity mirrors were deposited by reactive sputter deposition of SiO_2/Si_3N_4 to complete the laser cavity.

Introduction: High series resistances have severely limited the use of low-threshold vertical cavity surface emitting lasers (VCSELs). These high resistances (of about 1 kΩ) result from using the high reflectivity top mirror as the electrical *p*-contact. The lowest resistances have so far been obtained at the expense of high threshold currents by using metal contact/mirrors with relatively low (<97%) reflectivities [1]. More power efficient laser geometries based on high finesse cavities require electrical pumping through beryllium or carbon-doped GaAs/AlAs barriers, resulting in high driving voltages, cavity heating problems, and limitations of the laser operation speeds. Although already in the first monolithic VCSEL designs chirped layers were incorporated to reduce the series resistance of the *p*-side mirror/contacts [2], the threshold voltages of these devices have so far been limited to above 3·5 V. We have now reduced the voltage required for lasing in VCSELs to 1·7 V. The resistance-area products of our VCSELs are comparable to those reported for high-power edge-emitting lasers.

Procedure: Molecular beam epitaxy (MBE) was used to grow 30 pairs of *n*-doped $Al_{0.15}Ga_{0.85}As$/AlAs bottom mirror layers, the active *p–n* junction containing three 10 nm GaAs quantum wells separated by 12 nm $Al_{0.3}Ga_{0.7}As$ layers and a 1 μm *p*-doped top contact. 12 pairs of alternating SiO_2/Si_3N_4 layers formed a high-reflectivity mirror which completed the laser cavity. We have evaluated these reactive sputter-deposited mirrors using finesse measurements in resonator structures, and obtain reflectivities of 98·3% in 9·5 pairs [3]. Individual laser elements were defined by ion etching of mesas through the *p–n* junction, followed by deposition of SiO_2 to define the current path. Au–Zn *p*-contacts were then deposited around the mesa tops and alloyed for current injection (Fig. 1). Finally, another ion milling step was used to isolate individual contacts. Lasers with diameters ranging from 7·5 to 25 μm were thus fabricated and measured.

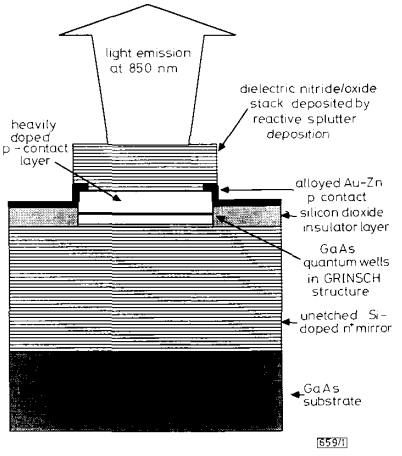

Fig. 1 *Schematic diagram of presented vertical cavity surface emitting laser structure*

Results and discussion: Light at 850 nm is generated by the 10 nm GaAs quantum wells and is emitted through the annular *p*-contact. The *p*-side resistance is reduced by heavily beryllium-doping the top of the cavity (Fig. 1) and completely avoiding the well/barriers inherent in epitaxially grown mirror/contact structures. By thus eliminating current flow through the upper *p*-doped semiconductor Bragg reflector present in previous VCSEL designs [2], this configuration reduces the series resistances of 12 μm diameter laser elements to 67 Ω averaged between the bandgap voltage (1·4 V) and the 2·0 V operating voltage. In contrast to the 'parabolic' profile of most VCSEL plots, this I–V characteristic is fairly linear right from the bandgap value (Fig. 2). The resulting resistance–area products are $<7 \times 10^{-5}\,\Omega\,cm^2$, nearly as low as the $<5 \times 10^{-5}\,\Omega\,cm^2$ calculated for high-power single-mode edge-emitting lasers*. The threshold currents and voltages of 12 μm diameter lasers were measured to be 3 mA and 1·7 V, respectively (Fig. 3). We determined peak output powers of 12 μm devices, and obtain 1 mW peak power when lasers are pulsed at 1% duty cycle with 20 mA. Higher powers are expected from optimised devices. These lasers have also been operated CW, although the threshold current increases to 4 mA when doing so.

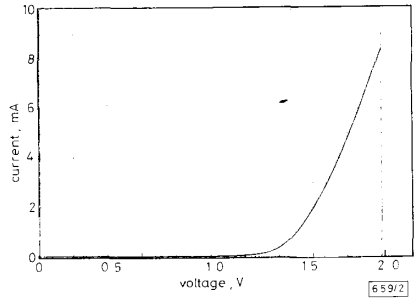

Fig. 2 *I–V characteristics of 12 μm diameter VCSEL*

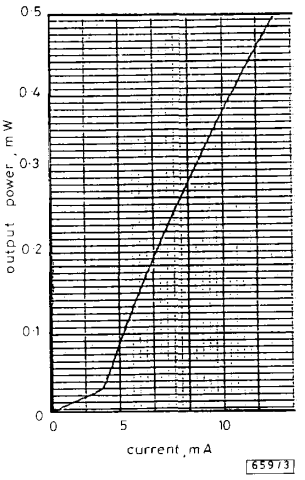

Fig. 3 *L–I curve from 12 μm diameter VCSEL pulsed with 1 μm at 1% duty cycle*

Another advantage of this laser design over previous monolithic laser structures lies in the relaxation of accuracy required during crystal growth. Thus, even if the cavity length is not tuned correctly to the quantum well emission wavelength and the bottom mirror reflectivity maximum, the top dielectric mirror stack can be redesigned to compensate for such a growth inaccuracy. This kind of retuning was required with this particular wafer. Figs. 4 and 5 show the measured

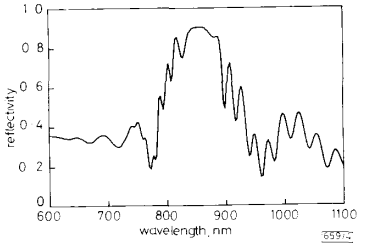

Fig. 4 *Reflectivity spectra of measured R against λ from grown wafer*

and modelled reflectivity spectra for the grown wafer, and it is evident that the measured cavity resonance peak is far from the optimum wavelength. In fact, we can reproduce the measured reflectivity spectrum (Fig. 4) by decreasing the optimum laser cavity length by about 1/4 λ or 65 nm (Fig. 6). This places the resonance as far from the optimum wavelength as possible. However, we can still fabricate lasers from this structure by compensating for the cavity length discrepancy with a 1/4 λ Si_3N_4 cavity extension layer before depositing the dielectric

* Spectra Diode Labs SDL-5400 series has 4 Ω in a 3 μm wide by 400 μm long area, or $4{\cdot}8 \times 10^{-5}\,\Omega\,cm^2$

top mirror. Although in principle this adjustment should severely compromise the laser performance because the $GaAs/Si_3N_4$ interface actually reduces the reflectivity of the mirror stack, the desirable device characteristics mentioned above are still obtained. This demonstrates the power of being able to deposit the upper portion of the Fabry–Perot cavity during processing to allow corrections of slight changes in layer thicknesses in the underlying semiconductor portion of the cavity. Smaller changes in the effective cavity length are obtained by controlling the top dielectric mirror thickness and we have tuned the emission wavelength from 850 to 855 nm. Further change of this wavelength is possible at the expense of higher threshold currents. This laser design also lends itself to microfabrication of focusing or polarisation optics in or close to the cavity. Sputter deposition of the passive dielectric mirrors does not require the clean, contamination-free surfaces and high growth temperatures necessary for epitaxial growth, and thus can be performed at the end of the fabrication procedure. We already obtain without fabrication, by depositing concave output mirrors, single transverse mode lasing in lasers with diameters as large as 25 μm.

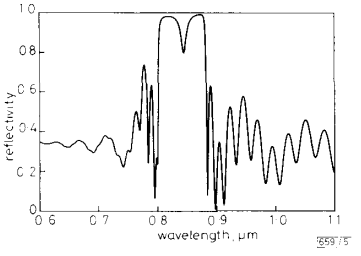

Fig. 5 *Calculated R against λ of grown wafer as designed with optimum cavity length ($m\lambda/2n$)*

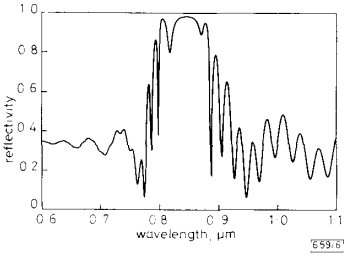

Fig. 6 *Calculated R against λ from modelled data assuming shorter ($m\lambda/2n - \lambda/4n$) cavity length*

Conclusions: The combination of high-reflectivity dielectric mirror layers coupled with MBE growth can be used to significantly reduce the power requirements of individual laser elements. Improved designs, growth, and fabrication should reduce the resistance further while allowing high quantum efficiency. We expect that this advance will allow us to integrate large numbers of VCSEL devices into complex arrays without the heat-dissipation problems found in more conventional VCSEL designs [4]. Finally, the relatively shallow depth of the active area from the semiconductor surface results in significantly shorter MBE growth times, and it allows us to greatly simplify the VCSEL fabrication process. Here we have shown that it is possible to obtain VCSELs from this hybrid design, and that we have significantly loosened the stringent requirements placed on the high accuracy of MBE crystal growth required for monolithic all-semiconductor VCSEL devices. In optimally grown laser structures, we expect lower threshold currents, much higher 'wallplug' power efficiencies, and higher powers and speeds than obtained with previous VCSEL designs.

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DETECTION OF BRIDGING FAULTS IN PROGRAMMABLE LOGIC ARRAYS

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Indexing terms: Programmable logic arrays, Fault detection, Large-scale integration, Logic testing

A test set and a testable design for MOS PLAs are proposed. The new design, which modifies a PLA by adding one extra line in the AND plane and one extra line in the OR plane, can detect bridging faults. Furthermore, the design modification requires very low area overhead and is independent of the personality of the PLA under test.

Introduction: Programmable logic arrays are an integral part of the VLSI design tool set and extensive research effort has been devoted to the problem of testing them. Faults that commonly occur in PLAs are modelled by stuck-at faults, crosspoint faults and bridging faults. All methods for testing PLAs can be categorised into test generation [3, 5] and testable design [6]. Almost all existing methods consider detection of only stuck-at and crosspoint faults. We propose a testable design to detect bridging faults that have often been ignored in the literature. We identify bridging faults that are equivalent to stuck-at or crosspoint faults. Thus such faults need not be dealt with in this Letter. We propose designs for a testability technique and a test set that guarantees detection of remaining bridging faults. We analyse the proposed designs for delay and area overhead and discuss the extension of our technique to encompass folded PLAs and compacted PLAs.

It has been discussed in the literature that bridging faults can be either AND type or OR type. Although we can also consider such a general definition of bridging faults in our treatment of faults, we choose a more realistic model. In MOS designs the logic behaviour of a bridging fault is almost always of the AND type. Therefore, in our discussion we shall consider only AND type bridging faults in PLAs.

The following notation is used to state our results and the necessary test sets. The n inputs to the PLA are denoted as x_1, $x_2, \ldots, x_n$. Bit lines corresponding to the input x_i are denoted as x_{i0} and x_{i1}, where $x_{i0}(x_{i1})$ is complemented (uncomplemented) x_i. It is shown in Reference 4 that a bridging fault between any two product lines, a bridging fault between any two output, and a bridging fault between x_{i0} and x_{i1} are equivalent to crosspoint faults in a PLA. Based on these observations, we conclude that the set of bridging faults F which are not shown to be equivalent to crosspoint faults