Simulation of current transients through ultrathin gate oxides during plasma etching

Gyeong S. Hwang and Konstantinos P. Giapis
Division of Chemistry and Chemical Engineering, California Institute of Technology, Pasadena, California 91125

(Received 25 June 1997; accepted for publication 2 August 1997)

Monte Carlo simulations of electron tunneling through a 3 nm gate oxide during etching of dense patterns of gate electrodes in uniform high-density plasmas reveal two current transients, which occur: (a) when the open area clears, and (b) when the polysilicon lines just become disconnected at the bottom of trenches. The first charging transient is fast (controlled by charging) and may be followed by a steady-state current which lasts until the lines get disconnected. The second charging transient lasts longer; the magnitude of the tunneling current generally decreases as the sloped polysilicon sidewalls become straighter. Most of the damage occurs at the edge gate when the open areas are covered by field oxide; however, the edge gate suffers no damage when the 3 nm oxide extends into the open areas. © *1997 American Institute of Physics.* [S0003-6951(97)02640-5]

Plasma-induced charging damage manifests itself in two ways: (a) lateral sidewall etching (notching effect)[1] and (b) gate oxide degradation (electron shading effect).[2] While the physics of the notching effect has been revealed,[3] the electron shading damage remains an unresolved issue[4] and exemplifies a formidable challenge that lies ahead as critical dimensions are incessantly reduced.[5] Oxide degradation is caused by large tunneling currents that flow during plasma etching; the latent nature of the damage requires sacrificial structures on the wafer or special charge monitors to its occurrence. The literature abounds with conflicting reports on when and how charging damage occurs.[4,6]

Like notching,[3] the electron shading effect is a result of differential microstructure charging brought about by the directionality difference between ions and electrons at the wafer.[2] The sidewalls of high aspect ratio trenches hinder the isotropic electrons from reaching the trench bottom and cause an imbalance of ion and electron currents, which must be overcome either by positive charging up of the surface or by an electron supply from elsewhere. When the gate-substrate potential difference across the gate oxide exceeds a threshold value,[5] electron tunneling occurs. Depending on the magnitude, duration, and nature of the tunneling current, reliability problems or even electrical failure may ensue.[5]

When do tunneling currents flow during the etching process? While no damage is expected during the main etch, ''damage is nearly invariant with the extent of overetch.''[7] Since monitoring of tunneling currents during etching is extremely difficult in realistic patterns, computer simulations are needed to reveal when and how tunneling currents cause damage. Such simulations have thus far been unavailable[8] as a result of the computational difficulty of the problem, which requires bridging three disparate timescales together: etching (10^2 s), charging (10^{-3} s), and tunneling ($\leqslant 10^{-7}$ s).

We report here results from Monte Carlo simulations of microstructure charging and sidewall profile evolution, explicitly accounting for electron tunneling currents through thin gate oxides. Two tunneling mechanisms are considered with well-established analytic expressions:[9] (a) Fowler–Nordheim tunneling (FNT) of electrons from the Fermi level of the n^+-polycrystalline Si (poly-Si) gate to the SiO_2 conduction band; and (b) direct tunneling (DT) of electrons from the n^+-poly-Si to the Si(100) conduction band (substrate). Tunneling from SiO_2 surface states is assumed to proceed by identical mechanisms. The treatment of charging and profile evolution is performed, as described elsewhere,[3] with the following addition: The potential of every SiO_2 surface segment and the equipotential of each gate are calculated to determine the electric field across the oxide and the total tunneling current to the substrate. The uniformly conductive substrate is assumed to be floating, and its potential responds to the net tunneling current.[6] Local electric fields are modified self-consistently as more charge accumulates, until steady state is reached. The charging calculations are repeated as the etch profile is advanced; decoupling is possible, since charging occurs at a faster timescale than etching.

Typical high-density plasma conditions are assumed: low pressure (<10 mTorr), uniform chlorine plasma of density 1×10^{12} cm^{-3}, dissociated to a degree that renders etching ion-limited. The sheath voltage is given by $37+30\sin\omega t$ V, where $\omega=0.4$ MHz is the rf bias frequency. The ion and electron temperatures are taken to be 0.5 and 4.0 V, respectively. The simulation starts with a masked structure (Fig. 1), consisting of five 0.3 μm photoresist lines separated by 0.3 μm spaces. Identical patterns are separated by open areas with a width of 4 μm. At the onset of etching, the structure consists of a 0.9 μm photoresist mask onto 0.3 μm n^+-poly-Si, formed on top of a 3 nm layer of SiO_2. The open areas are covered either by thick (>100 nm) field oxide

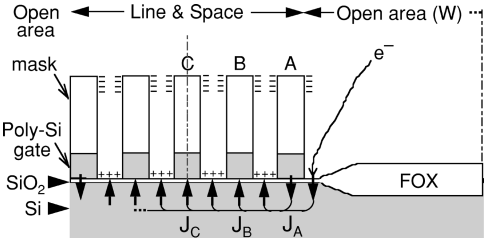

FIG. 1. Schematic of the line-and-space structure, as it would be if perfectly etched; case I is shown, with field oxide (FOX) covering the open area. The dashed-dotted lines indicate mirror axes defining the simulation domain. The arrows (J_i) indicate the direction of *electron* flow at various surface segments. Only currents under the poly-Si lines can cause reliability problems and electrical breakdown.

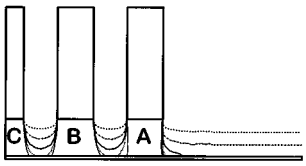

FIG. 2. Sequence of simulated etch profiles for case I, at various etch times. The thick solid line represents the profile just when the open area clears, and illustrates the existence of ARDE, despite etching in an ion-limited regime. The thin solid line represents the profile after 100% overetching.

(case I) or by 3 nm gate oxide (case II). The main etch is followed by an overetch step (100%).

To capture current transients, the profile evolution simulation must describe aspect-ratio-dependent etching (ARDE). ARDE is usually attributed to neutral shadowing[10] which, however, should not affect ion-limited etching. Nevertheless, ARDE can still occur because of differential microstructure charging,[11] as shown in Fig. 2. The smaller etch rate in the trenches can be explained by plotting the ion energy distribution function (IEDF) at the poly-Si surface at various ''snapshots'' during etching (Fig. 3). The IEDF at the onset of the main etch [Fig. 3(b)] differs from the initial IEDF [Fig. 3(a)] because ion motion is perturbed by in-trench electric fields. A reduction in intensity for both low- and high-energy peaks is apparent; the latter is also shifted to lower energies, mainly as a result of the potential of the poly-Si (3.8 V). Small changes in the IEDF take place during the main etch. At the onset of overetching [Fig. 3(c)], the IEDF is no longer bimodal, although there are still low energy ions arriving at the poly-Si surface. The high-energy peak is shifted to even lower energies due to an increase in the poly-Si potential. The energy is further reduced when the poly-Si lines become disconnected at the trench bottom [Fig. 3(d)]. These results clearly demonstrate that the etch rate in the trench aspect-ratio-dependent.

Next, we monitor the potential of various gates (V_i, i=A, B, C) and the floating substrate (V_{sub}), as a function of the etch time for case I [Fig. 4(a)]. During the main etch, $V_A=V_B=V_C=3.8$ V while $V_{sub}=1.9$ V. The electric field in the oxide is too small to induce electron tunneling. As the open area clears, the potential of the connected lines jumps to 10.6 V, while V_{sub} increases in unison to 9.1 V, where they remain for the duration of the initial overetch. When the trench bottoms start to clear and the lines become disconnected, V_B, V_C, and V_{sub} increase further while V_A decreases. After some fluctuation, the potentials appear to stabilize at about: $V_A=7.8$ V, $V_B=12.9$ V, $V_C=14.0$ V, and $V_{sub}=11.0$ V. These changes occur because of variations in the supply of electrons to the gates as the profile evolves, and can be understood in conjunction with the tunneling currents (J_i, i=A, B, C), plotted in Fig. 4(b). During the main etch, no tunneling current flows. Electrons bombarding the open area (unshadowed) help balance the current inequality at the patterned area due to electron shading. When the open area clears, electrons can only be supplied to the outer edge of the pattern. The potential of the connected lines must increase to attract more electrons, so that the balance is maintained. As the substrate attempts to follow, a few electrons tunnel to the poly-Si (first transient). The current balance is perturbed

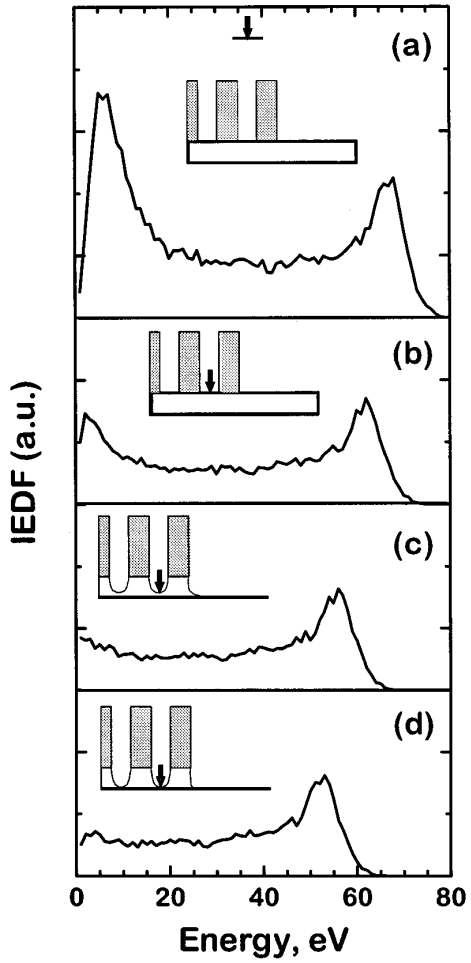

FIG. 3. Ion energy distribution functions (IEDFs) for case I, at various instances during etching: (a) initial IEDF just above the microstructure, (b) at the start of the main etch, (c) at the start of the initial overetch (just after the open area clears), and at the start of the final overetch (just when the lines become disconnected at the trench bottoms). The insets show the surface segment where the IEDF is calculated (arrows).

again, when the lines become disconnected. The electron supply to the outer edge of line A becomes localized and decreases V_A. V_B and V_C must increase to deflect more ions; as V_{sub} trails, J_B and in particular J_C increase dramatically (second transient). The deflected ions in the trenches neutralize the entrance potential, thus allowing more electrons to enter; the supply to intermediate lines increases, stabilizing their potentials. J_B increases less than J_C because of its proximity to gate A. Since $V_A<V_B$, more electrons entering the trench between A and B are deflected to B; the same is not true for the neighboring trench ($V_B\approx V_C$, initially). As etching proceeds and the sidewalls become straighter (Fig. 2), fewer ions are collected by the gates, thus requiring less electrons to tunnel from the substrate. J_B and J_C decrease gradually. However, the ions charge up the newly exposed SiO_2, and the need for electron tunneling from the substrate continues. Increasing electron tunneling from gate A to the substrate satisfies that need. J_A saturates when the sidewalls become straight. During the second transient, J_B and J_C peak at 1.9 and 4.1 mA/cm^2, respectively, which appears to be too small to cause oxide breakdown, a conjecture also supported by the less damaging DT mechanism for electron conduction at 3 nm. However, the current under gate A persists for the

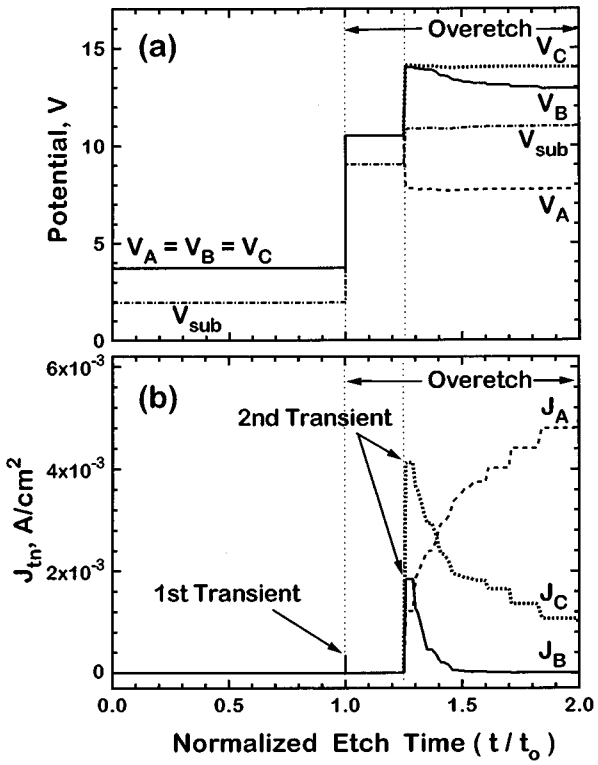

FIG. 4. (a) The charging potentials of various gates (A, B, C), and (b) the tunneling currents under them as a function of the normalized etch time, for thick field oxide covering most of the open areas (case I).

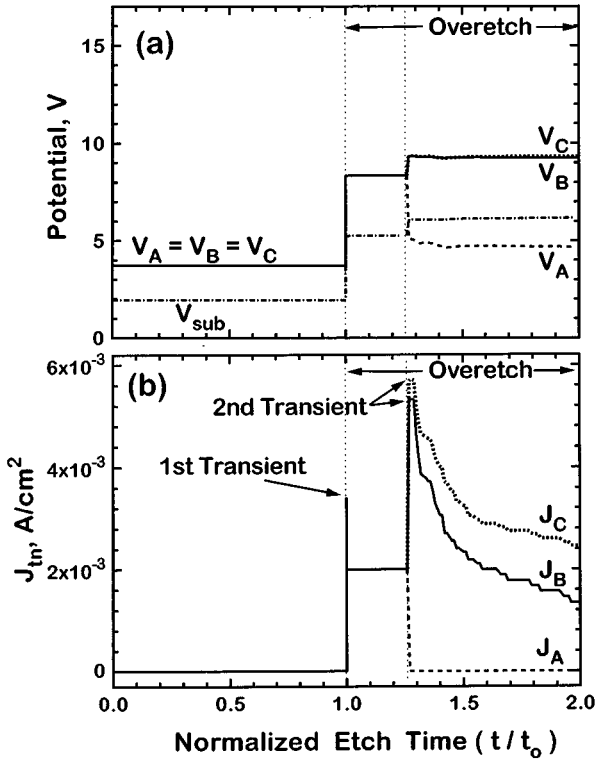

FIG. 5. (a) The charging potentials of various gates (A, B, C), and (b) the tunneling currents under them as a function of the normalized etch time, for a 3 nm gate oxide spanning the whole wafer (case II).

duration of the overetch and may cause cumulative damage.

Reducing the field oxide thickness to 3 nm (case II), facilitates electron tunneling through the open area. During overetching, the extra electrons pin the substrate potential [Fig. 5(a)]. As a result, the potentials of all lines are also lower than those attained in case I, the trends with etch time are very similar. In contrast, the tunneling current behavior is profoundly different [Fig. 5(b)]. During the first transient, the current jumps to a higher value of 3.4 mA/cm^2, before dropping to a steady-state value of 2.0 mA/cm^2; the latter lasts until the lines become disconnected at the trench bottoms. At that instant, J_B and J_C jump up to 5.3 and 5.7 mA/cm^2, respectively, before they begin to drop gradually as overetching continues. Remarkably, no tunneling current flows under gate A during the final overetch. Thus, if there is damage, it will now appear under intermediate gates.

Since the profile shape controls the ion current to intermediate gates, a reduction in the magnitude of the second transient in both cases I and II is possible. For example, if the sidewalls evolve straighter during the main etch—as when the aspect ratio is lower or the rf bias is larger, then less sidewall area is exposed to direct ion bombardment when the trench bottoms become disconnected. While both transients occur because of ARDE, the peak transient current does not depend on the extent of ARDE. However, the cumulative current between the two transients, seen for Case II [Fig. 5(b)], does depend on the extent of ARDE.

In conclusion, simulations of charging and profile evolution during gate electrode etching offer insight into the nature of charging damage by revealing when, where, and how tunneling currents flow under the gates. Current transients are found to surge under intermediate gates when these become disconnected at trench bottoms during overetching. As the sidewalls become straighter, the tunneling current is gradually reduced. When field oxide covers the open area separating dense patterns, tunneling current under the edge gates increases with overetching and cumulative damage may ensue there. When gate oxide (3 nm) spans the open area, no current flows under the edge gates; however, a new current transient surges at endpoint, which is followed by a steady-state current until the gates become disconnected.

This work was supported by a Camille Dreyfus Teacher-Scholar Award to KPG.

[1] T. Nozawa, T. Kinoshita, T. Nishizuka, A. Narai, T. Inoue, and A. Nakaue, Jpn. J. Appl. Phys. **34**, 2107 (1995).
[2] K. Hashimoto, Jpn. J. Appl. Phys. **32**, 6109 (1993); **33**, 6013 (1994).
[3] G. S. Hwang and K. P. Giapis, J. Vac. Sci. Technol. B **15**, 70 (1997).
[4] Proceedings of the 1st International Symposium on Plasma Process-Induced Damage, Santa Clara, CA, 1996.
[5] S. Wolf, *Silicon Processing for the VLSI Era* (Lattice Press, Sunset Beach, CA, 1995), Vol. 3.
[6] K. P. Cheung and C. P. Chang, J. Appl. Phys. **75**, 4415 (1994).
[7] S. Krishnan, W. Dostalik, K. Brennan, S. Aur, S. Rangan, and S. Ashok, Technical Digest, International Electron Device Meeting, 1996, p. 731.
[8] Simplistic calculations of current injection through thin gate oxide during metal etch have been presented by T. Kinoshita, S. Krishnan, W. W. Dostalik, and J. P. McVittie, *Proceedings of the 2nd International Symposium on Plasma Process-Induced Damage*, Monterey, CA, 1997, p. 45. Since profile evolution during etching was not included, no *true* transients were observed.
[9] M. Lenzlinger and E. H. Snow, J. Appl. Phys. **40**, 278 (1969); Z. A. Weinberg, Solid-State Electron. **20**, 11 (1974).
[10] R. A. Gottscho, C. W. Jurgensen, and D. J. Vitkavage, J. Vac. Sci. Technol. B **10**, 2133 (1992;), and references therein.
[11] J. C. Arnold and H. H. Sawin,J. Appl. Phys. **70**, 5314 (1991).