Performance Enhancement of a Graphene-Zinc Phosphide Solar Cell using the Electric Field-Effect

Supporting Information

Oscar Vazquez-Mena,1,2 Jeffrey P. Bosco,3 O. Ergen,1,2 Haider I. Rasool,1,2 Aidin Fathalizadeh,1,2 Mahmut Tosun,2,4 Michael Crommie,1,2,5 Ali Javey,2,4 Harry A. Atwater,3 and Alex Zettl1,2,5

1 Department of Physics, University of California, Berkeley, California 94720, U.S.A.
2 Material Sciences Division, Lawrence Berkeley National Laboratory, Berkeley, California 94720, U.S.A.
3 Department of Applied Physics and Department of Chemical Engineering, California Institute of Technology, Pasadena, California 91125, U.S.A.
4 Electrical Engineering and Computer Sciences, University of California, Berkeley, California 94720, U.S.A.
5 Kavli Energy Nanosciences Institute at the University of California, Berkeley, and the Lawrence Berkeley National Laboratory, Berkeley, California 94720, U.S.A.

Corresponding Authors:
Prof. Alex Zettl (azettl@berkeley.edu)
Oscar Vazquez-Mena (oscar.vazquezmena@gmail.com)
Supporting Information Content

A) Fabrication process

B) Capacitance measurements for Figure 3.D

C) Calculations of carrier concentration, change in graphene Fermi level and built-in potential

D) Photovoltaic measurements instruments
A) Fabrication process

The process flow fabrication for the devices is illustrated below in Figure S1. We start with a Zn$_3$P$_2$ layer 7 μm thick on top a Zn-doped GaAs substrate ~500 μm thick as shown in step 1 (from step 2 to 8 we only show the Zn$_3$P$_2$ and we omit the GaAs substrate). Then an oxide layer labeled Oxide-1 is deposited on the substrate and is composed of a 20 nm thick ZrO$_2$ film deposited by atomic layer deposition followed by a 40 nm thick SiO$_2$ layer deposited by electron beam evaporation (step 2). The oxide-1 layer is patterned by e-beam lithography and lift-off. Then a graphene layer, grown on copper by chemical vapor deposition, is transferred onto the substrate covering the entire chip (step 3). The graphene is then patterned by e-beam lithography and O$_2$ plasma (step 4). To make electrical contact to graphene, a Cr(10 nm)/Au(80 nm) thick layer labeled as Au-C is deposited on top of oxide-1 (step 5). The oxide-1 layer prevents an electric short between the Au-C and Zn$_3$P$_2$. Then the gate oxide layer, labelled as Oxide-2, is deposited. It has the same composition as oxide-1, 20 nm thick ZrO$_2$ film deposited by atomic layer deposition followed by a 40 nm thick SiO$_2$ layer deposited by electron beam evaporation (step 6). As a gate electrode we use a thin Au layer consisting of 3 nm of Cr and 12 nm of Au (Au-G) deposited by thermal evaporation (step 7). Finally, an Ag electrode is deposited directly on top of Zn$_3$P$_2$ to make an ohmic contact with Zn$_3$P$_2$.

Figure S1: Fabrication Process Flow

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1)</td>
<td>Zn$_3$P$_2$ (~7μm thick) on Zn-doped GaAs substrate (~500μm thick)</td>
</tr>
<tr>
<td>2)</td>
<td>Oxide-1 (20 nm ZrO$_2$) Oxide-1 (40 nm SiO$_2$) Oxide-1 (40 nm SiO$_2$)</td>
</tr>
<tr>
<td>3)</td>
<td>Oxide-1 (20 nm ZrO$_2$) Oxide-1 (40 nm SiO$_2$) Oxide-1 (40 nm SiO$_2$) with Graphene</td>
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</table>
The capacitance measurements were performed using an HP4192 LF Impedance Analyzer with an excitation of 50 mV @ $10^5$ Hz.
For the data from Figure 3.D we apply a top gate voltage with a Keithley sourcemeter. We observed variations in the measurements, so we performed a series of 5 measurements at each gate voltage of −1, 0 and 1 V that are shown in Figure S2.

These data were taken as follows. We apply a $V_g = -1$ V and ramp $V_{bi}$ from −0.5 to 0.2 V. From this data we obtain our first data for $V_g = -1$ (Vg_-1_M1 in previous plot). Then we left $V_g$ and $V_{bi}$ electrically floating for ~30 min. After the 30 min we applied again $V_g = -1$ V and ramp $V_{bi}$ from −0.5 to 0.2 V to obtain our second set of data for $V_g = -1$ V (Vg_-1_M2). We repeated the same process 3 more times to obtain our 5 sets of measurements for $V_g = -1$ V. This procedure was repeated again for $V_g = 0$. We left the device electrically floating, then apply $V_g = 0$ and ramp $V_{bi}$ from −0.5 to 0.2 V. Then we float again $V_g$ and $V_{bi}$, wait 30 min, and then set again $V_g = 0$ and ramp $V_{bi}$ from −0.5 to 0.2 V until we get 5 data sets.
The same was done for \( V_g = 1 \) V. In this way we got 5 measurements for each of the gate voltages of \(-1, 0, \) and \(1\) V, with \(\sim 30\) minutes between each measurement leaving the device floated (disconnecting our probes from the device).

The mean value with error tolerances obtained for the built-in potentials are:

- At \( V_G = -1 \) V \(\rightarrow V_{bi} = 0.18 \pm 0.02 \) V
- At \( V_G = 0 \) V \(\rightarrow V_{bi} = 0.31 \pm 0.04 \) V
- At \( V_G = +1 \) V \(\rightarrow V_{bi} = 0.44 \pm 0.06 \) V

\[ \text{C)} \] Calculation of carrier concentration, change in graphene Fermi level and built-in potential

C.1) Carrier concentration in \( \text{Zn}_3\text{P}_2 \) extracted from Figure 2.B:

The total capacitance \( C_T \), measured in Figure 2.B, is equal to the equivalent capacitance of the oxide capacitance \( C_O \) in series with the capacitance \( C_D \) from the depletion zone in \( \text{Zn}_3\text{P}_2 \) (\( 1/C_T = 1/C_O + 1/C_D \)).

At negative voltages, in the accumulation mode, \( C_T \sim 58 \) nF/cm\(^2\). Since, \( C_D \rightarrow \infty \) because there is no depletion width, then \( C_O = C_T \sim 58 \) nF/cm\(^2\).

At positive voltages, in depletion mode, \( C_T \sim 40 \) nF/cm\(^2\). Since \( 1/C_D = 1/C_T - 1/C_O \), then \( C_D = 128 \) nF/cm\(^2\).

From the depletion width we can estimate the carrier concentration through the expression:

\[
W = 2 \sqrt{\frac{\varepsilon \ell t}{q n_i^2 N_A}}.
\]

Substituting for \( n_i = 3.5 \times 10^{20} \) m\(^{-3}\) (Springer database) and \( N_A = 6 \times 10^{22} \) m\(^{-3}\) gives \( W \sim 73 \) nm.

Thus the estimated carrier concentration in \( \text{Zn}_3\text{P}_2 \) is \( \sim 6 \times 10^{16} \) cm\(^{-3}\).

C.2) Carrier concentration in \( \text{Zn}_3\text{P}_2 \) extracted from Figure 3.D:

\[
1/C^2 = 2 (V_{bi} - V)/q \varepsilon N_A,
\]

thus, the slope of the function is equal to:

\[
\Delta(1/C^2)/\Delta V = -2/q \varepsilon N_A,
\]

and

\[
N_A = 2/(q \varepsilon) \times (\Delta V/\Delta (1/C^2)).
\]

Substituting that \( \varepsilon = 11 \times 8.85 \times 10^{-14} \) F/cm, and taking from Figure 3.D for \( V_G = 0 \) that for \( \Delta V = 0.7 \) V, \( \Delta (1/C^2) = 90.9E-6 \) cm\(^4\)/nF\(^2\), we obtain \( N_A = 9.88 \times 10^{16} \) cm\(^{-3}\).

C.3) Change in Fermi level in graphene induced by gate voltage:

The gate dielectric consists of a 20 nm layer of \( \text{ZrO}_2 \) with a 40 nm layer of evaporated \( \text{SiO}_2 \). Our characterization of the films has given values of \( \varepsilon (\text{ZrO}_2) = 18 \) and \( \varepsilon (\text{SiO}_2) = 5.6 \). From here we can estimate the capacitance of the layer:

\[
\begin{align*}
C(\text{ZrO}_2) &= 18 \times (8.85 \times 10^{-14} \text{F/cm})/20 \text{ nm} = 796 \text{ nF/cm}\(^2\), \\
C(\text{SiO}_2) &= 5.6 \times (8.85 \times 10^{-14} \text{F/cm})/40 \text{ nm} = 123.9 \text{ nF/cm}\(^2\).
\end{align*}
\]

Total capacitance (series) is: 107.21 nF/cm\(^2\).
The charge induced in graphene can be easily calculated from \( Q = CV \), for a gate voltage of 1 V:
\[
Q = CV = (107.21 \text{ nF/cm}^2) \times (1 \text{ V}) = 107.21 \text{ nC/cm}^2 = 6.68 \times 10^{11} \text{ e}^-/\text{cm}^2.
\]

The corresponding change in Fermi level:
\[
\Delta E_F \sim v_F \sqrt{(\pi n)} \approx (1.15 \times 10^8 \text{ cm/s}) \times (6.58 \times 10^{-16} \text{ eVs}) \times \sqrt{(\pi \times 6.68 \times 10^{11} \text{ cm}^2)} = 0.109 \text{ eV} \sim 0.11 \text{ eV}.
\]

Thus, the estimated change in graphene Fermi level for \( \Delta V_G = 1 \text{ V} \) is \( \sim 0.11 \text{ eV} \).

Where \( v_F = 1.15 \times 10^8 \text{ cm/s} \) is taken from Xu et al. Appl. Phys. Lett. 98, 133122 (2011)

C.4) Built-in potential induced by gate voltage

The built-in potentials were extracted by extrapolating to the abscissa of \( 1/C^2(V_B) \) for each of the measurements and then averaging and setting the standard deviation as error tolerance. The mean values extracted are:

At \( V_G = 1 \text{ V} \), \( V_{bi} = 0.442 \pm 0.062 \text{ V} \)
At \( V_G = 0 \text{ V} \), \( V_{bi} = 0.309 \pm 0.037 \text{ V} \)
At \( V_G = -1 \text{ V} \), \( V_{bi} = 0.188 \pm 0.016 \text{ V} \)

The change in built-in potential when \( V_G \) goes from \(-1\) to \( 0 \) \text{ V} \) is:
\[
\Delta V_{bi} = V_{bi}(V_G = 0) - V_{bi}(V_G = -1 \text{ V}) = (0.309 \pm 0.037 \text{ V}) - (0.188 \pm 0.016 \text{ V}) = 0.121 \pm 0.040 \text{ V}
\]

The change in built-in potential when \( V_G \) goes from \( 0 \) to \(+1\) \text{ V} \) is:
\[
\Delta V_{bi} = V_{bi}(V_G = +1) - V_{bi}(V_G = 0 \text{ V}) = (0.442 \pm 0.062 \text{ V}) - (0.309 \pm 0.037 \text{ V}) = 0.133 \pm 0.072 \text{ V}
\]

D) Photovoltaic measurements instruments

Photovoltaic conversion was measured under an Oriel AM1.5 sunlight simulator (model 67005).