and so the ratio
\[ \frac{I_d}{g_m} = \frac{1}{n} (V_p + V_d) \] (3)
should give a straight line when plotted on linear scales as a function of \( V_p \). Further, the pinch-off voltage and the exponent are obtained directly as the intercept on the voltage axis and the reciprocal slope of the straight line.

Plots of (3) for \( p-n \) junction FET's of various structures are shown in Fig. 1, and the resulting values of \( V_p \) and \( n \) are given in Table I. It is seen that the experimental points do indeed define straight lines quite closely, thus vindicating the postulated power-law relation of (1). Moreover, the values of \( n \) obtained are reasonably close to 2, thus lending weight to the simple theoretical square-law derivation of the accompanying communication. The departure from a straight line in some units near the pinch-off voltage is due to drain leakage current, and is the effect that prevents direct measurement of the pinch-off voltage. The maximum in \( I_d/g_m \) that occurs at small positive gate voltages is to be expected on theoretical grounds, and is not significant in determining the best-fit straight line over the range \( 0 < |V_d| < V_p \).

It is concluded that the power-law relation of (1) satisfactorily represents both theoretically and experimentally the transfer characteristics of an FET in the pinch-off region, and allows values of the pinch-off voltage to be determined directly from experimental measurements.

A future communication will show so that occurs at small positive gate voltages is to be expected on theoretical grounds, and is not significant in determining the best-fit straight line over the range \( 0 < |V_d| < V_p \).

| Unit | Type | Nature of function | \(|V_d|\) volts | \(|V_p|\) volts | \( n \) |
|------|------|--------------------|---------------|---------------|-----|
| #1   | Crystalonics 610 | alloy (n-channel) | 9.83 | 2.20 |
| #2   | Motorola MM 764 | epitaxial (n-channel) | 2.74 | 2.18 |
| #3   | Texas Instruments TIX 691 | diffused (n-channel) | 1.79 | 2.15 |
| #4   | Fairchild FSP 401 | diffused (n-channel) | 2.68 | 1.98 |

A Simple Derivation of Field-Effect Transistor Characteristics

In the conventional treatment of the field-effect transistor, the first step is the specification of an impurity profile that describes the nature of the gate-channel contact. Solutions for the static and small-signal characteristics are then valid only for the particular impurity profile chosen, and must be repeated from the beginning for different structures.

The purpose of this communication is to present a simple, though approximate, development of the characteristics of an FET without specifying the detailed nature of the structure. The charge-control approach is used, and it is shown that in the pinch-off region the relation between the drain current and the gate-source voltage is approximately square law. The results are applicable to all gate-channel structures, including the insulated gate types.

The basic model of an \( n \) channel FET (field-effect transistor) is shown in Fig. 1. One-dimensional current flow in the channel of length \( L \) is assumed to occur under the influence of a drain-source voltage \( V_d \) and a gate-source voltage \( V_g \). The method of solution is to calculate the drain current \( I_d \) from the fundamental charge-control relation
\[ I_d = Qe/\tau_i, \]
where \( \tau_i \) is the average transit time of the mobile carriers making up the total charge \( Q \) in transit between source and drain. The total mobile charge \( Q \) in the channel can be considered as made up of two parts: one part, \( Q_o \), is the charge which would exist in the absence of the gate structure; the other part, \( Q_c \), is the additional charge induced by a gate voltage.

The basic simplifying assumption to be made is that the potential drop in the channel is uniform so that the electric field is constant and equal to \( V_d/L \). If the mobile carriers have constant mobility \( \mu \), the drift velocity is constant at \( v_d = \mu V_d \) and the transit time is
\[ \tau_i = L^2/\mu V_d. \]

The drain current is
\[ I_d = (Q_o + Q_c) V_d = G(1 + Q_c/Q_o) V_d \]
where
\[ G(1 + Q_c/Q_o) \]
represents a capacitance which, under certain conditions, may be identified as the total gate capacitance. Hence the drain current is given by
\[ I_d = G(1 + V_d/V_o) V_d. \] (1)

The above equation describes approximately the drain characteristics of the device in the region where the incremental drain conductance \( \partial I_d/\partial V_d \) is finite, as indicated in Fig. 2. From the above equation, the drain conductance is
\[ \frac{\partial I_d}{\partial V_d} = G(1 + V_d/V_o), \] (2)
which goes to zero when \( V_d = V_o = Q_c/C_o \). The drain current for which the drain conductance is zero is therefore given as a function of gate voltage by substitution of this condition on \( V_d \) back into (1), which leads to
\[ I_d = G(1 + V_d)^2/V_o. \] (3)

If the gate voltage is chosen so that \( V_g = -Q_c/C_o \), the drain current is zero and
hence $V_p = Q_d/C_d$ is identified as the pinch-off voltage. To a first approximation, therefore, the drain conductance is zero when the drain voltage equals or exceeds $V_p + V_d$. In normalized form, (3) may be written

$$I_d = I_{d0}(1 + V_d/V_p)^n$$

where $I_{d0}$ is the drain current in the pinch-off region when $V_d = 0$. Eq. (4) thus describes approximately the drain characteristics beyond pinch-off, as indicated in Fig. 2.

The transconductance $g_m$ in the pinch-off region is obtained from (3) as $g_m = dI_d/dV_d = G(1 + V_d/C_d/Q_d)$, which shows the well-known result that the transconductance at zero-gate voltage is equal to the total channel conductance in the absence of the gate structure.

The square-law dependence of drain current upon gate voltage is only approximate, not only because of the initial assumption of constant channel field, but also because the capacitance $C_d$ in general is not constant, but is a function of both $V_d$ and $V_g$. However, when the drain voltage equals or exceeds the pinch-off voltage, $C_d$ is essentially independent of $V_d$. The result of (2) is valid when used to obtain the characteristics beyond pinch-off. Nevertheless, the parameters $I_{d0}$ and $V_p$ in (4) in general remain dependent, though only weakly so, upon $V_d$.

The simple square-law functional relation of (4) has been derived without specification of the channel impurity profile or of the nature of the gate contact, and is valid for negative $V_d/V_p$ ($p-n$ junction FET's) and for either positive or negative $V_d/V_p$ (insulated-gate FET's). Experimental substantiation of this power law is presented in an accompanying communication.

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### Nanovolt Transistor dc Amplifiers

The major limitation in the design of low-level transistor dc amplifiers has always been considered to be the drift resulting from the variations in parameters of transistors with temperature. In the differential configuration, the null stability has been mainly limited by the unavoidable mismatch in the thermal coefficients of the transistor parameters. A considerable improvement has been achieved by the use of a compensation circuit. However, the degree of compensation is again limited by the temperature differential between the transistors and the compensation network.

We have developed a new type of differential configuration, in which the compensation is realized by the transistors themselves. For this reason, this configuration may be referred to as "self-compensating." The drift can be cancelled to such a degree that the low-level limitation in transistor dc amplifiers seems now to be the low-frequency noise.

For reasonably small source resistances and low operating collector currents, the dominant component of the thermal drift in silicon transistors normally arises from the mismatch in the temperature coefficients of the base-emitter voltages. This temperature coefficient of $V_{BE}$ is predictable on well-established theoretical grounds, and, to a high degree of accuracy, it depends only on $V_{BE}$ itself. Thus it appears that the match of the temperature coefficients of $V_{BE}$ should be improved by operating the two transistors with equal base-emitter voltages, rather than with the conventional procedure of using equal collector currents and matched collector resistances.

These conditions of operation with matched $V_{BE}$ can be realized in a floating input stage as shown in Fig. 1 where $R_b$ is made equal to zero and $R_b$ is adjusted in order to have the same base voltages. The need for $R_b$ and the network containing $R_b$ will appear later. The zero adjustment (i.e., the condition zero output for zero input signal) is realized by unbalancing the collector load resistors by means of potentiometer $R_b$.

The square-law dependence of drain current upon gate voltage is only approximate, not only because of the initial assumption of constant channel field, but also because the capacitance $C_d$ in general is not constant, but is a function of both $V_d$ and $V_g$. However, when the drain voltage equals or exceeds the pinch-off voltage, $C_d$ is essentially independent of $V_d$. The result of (2) is valid when used to obtain the characteristics beyond pinch-off. Nevertheless, the parameters $I_{d0}$ and $V_p$ in (4) in general remain dependent, though only weakly so, upon $V_d$.

The simple square-law functional relation of (4) has been derived without specification of the channel impurity profile or of the nature of the gate contact, and is valid for negative $V_d/V_p$ ($p-n$ junction FET's) and for either positive or negative $V_d/V_p$ (insulated-gate FET's). Experimental substantiation of this power law is presented in an accompanying communication.

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