Equalization of IM3 Products in Wideband Direct Conversion Receivers

Edward Keehr and Ali Hajimiri

California Institute of Technology
Pasadena, CA, USA
Outline

- Introduction
  - RF Building Blocks
  - Equalization Challenges and Techniques
  - Experimental Results
  - Conclusion
Nonlinearity in RF Receivers

- Nonlinear circuits, blockers cause cross-modulation distortion.
- This may cause interference at the desired signal frequency.
- In FDD UMTS, TX leakage and CW blocker dominate this effect.
3rd Order Distortion in Receivers

- Standard blocks + SAW-less → IM3 products overwhelm the desired signal.
Feedforward IM3 Equalization [1]

- Regenerate IM3 terms without desired signal.
- Equalize effective baseband transfer functions in two paths.
- General technique – not limited to FDD IM3 problem.

LEGEND
- Desired Signal
- CW Blocker
- Modulated Blocker
- CW IM3 Product
- Modulated IM3 Product
Experimental Receiver Architecture
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Main Path: LNA and Balun
Main Path: Mixer

- High IIP2 performance [2].
- Folded for 1.2V operation.
Alternate Path: IM3 Term Generator

Requirements of IM3 Term Generator:
1. Negligible linear term feedthrough.
   • Signal (IM3) to error ratio = IER
2. Alternate Path IER >> Main Path peak IER.
   • Target: 7dB IER path excess.
   • Target: 10dB IER generator excess.

Why?
1. Will avoid small signal gain reduction.
2. Minimizes requirements on Main Path blocks.
- Desired IER > 30 dB.
- MOSFET = Weak 3\textsuperscript{rd} order nonlinearity.
- This design [3] does not meet specification.
**IM3 Generator - 2\textsuperscript{nd} Order Nonlinearity**

- MOSFET = Strong 2\textsuperscript{nd} order nonlinearity.
- Break up cubing into a squaring and a multiplication.
- Add gain in between nonlinear operations.
IM3 Generator - 2\textsuperscript{nd} Order Nonlinearity

- Canonical MOS squaring circuit is used in this design.
- Dummy squaring circuit replicates CM signal.

= Resistor Connected to DC Bias Voltage
IM3 Gen. – Distributed Multiplication

MULTIPLICATION #1 – IM2 PRODUCTS GENERATED

MULTIPLICATION #2 – IM3 PRODUCTS GENERATED

• High gain can be applied to IM2 products over low-bandwidth stages.
Distributing the multiplication can result in error when an IM3 term contributor is a modulated signal.
Error occurs at the points where symbols overlap.
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LMS Adaptive Equalization: Introduction

- Time-varying FIR filter weights a reference signal and subtracts it from another signal.
- Filter taps are adjusted based on the instantaneous correlation estimate between the equalizer output and the reference signal.
LMS: Mismatch in I/Q Mismatch

Path Complex DC Transfer Function

- Regular LMS can only perform rotation and scaling.
- Need another degree of freedom.
Enhanced LMS Adaptive Equalization

- Permit independent taps from each alternate input to both I and Q main paths.
- Each tap (register) can be considered a degree of freedom.
- Little additional hardware cost, as # of multipliers is the same.
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Effect of DC Offset on Adaptive Equalizer

- DC offset is a random variable.
- DC offset is uncorrelated with the path mismatch.
- Attempting to equalize both DC offset and path mismatch requires many taps.

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DC Offset and High-Pass Filters

- When the alternate path is turned on, the DC offset appears as a step response to the HPF.
- The resulting error transient delays equalizer convergence.
- 10kHz HPF cutoff frequency $\rightarrow$ 40-60$\mu$s convergence time.
DC Offset Trimming prior to HPF

- Removing DC offset in alternate path prior to adaptive equalizer power-up prevents the error transient.
- DC offset trimming circuit removes 70/256 LSB of offset in 4\( \mu \)s.
- DC offset trimming can be carried out off-line.
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Chip Die Photo

• 130nm RF CMOS process, fully ESD protected.
Description of Experiment

• “Two-tone” test with QPSK modulated UMTS TX signal.
• Sweep TX/CW Blocker amplitude with/without correction.
• Fix $A_{CW} = A_{TX}-8dB$
• Worst case: $f_{TX}=1.98GHz$, $f_{CW}=2.05GHz$, $f_{LO}=2.12GHz$. 
Measurement – Swept Blocker Amplitude

- Uncorrected IM3 error rises with slope of 3 as expected.
- Effective IIP3 is improved from -7.1dBm to +5.3dBm.
- Regular NLMS: IM3 is 4dB worse at -25dBm TX leakage.
• Consider $\omega_{CW} < \omega_{TX}$. Also, fix $A_{CW} = A_{TX} - 5$ dB.
• Here, the IM3 product contains squared TX leakage.
• Distributed multiplication group delay effect is present here.
• Cases shown are more stringent than specification.
• The complete system was operated across the UMTS RX band.
• Performance is consistent at all frequencies.
• Effective IIP3 is boosted by about 12dB under correction.
Measurement – Convergence

\[ \omega_{TX}(-25\text{dBm}) < \omega_{CW}(-33\text{dBm}) \]

\[ \omega_{CW}(-30\text{dBm}) < \omega_{TX}(-25\text{dBm}) \]

- Measured algorithm convergence time is about 10\(\mu s\).
- Convergence without DC offset correction takes much longer.
# Performance Summary

<table>
<thead>
<tr>
<th>Parameter Measured at $f_{\text{LO}}=2.1225\text{GHz}$</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Active Analog Die Area</td>
<td>1.6mm $\times$ 1.5mm</td>
</tr>
<tr>
<td>Technology Node</td>
<td>130nm CMOS</td>
</tr>
<tr>
<td>Analog Die LNA+Main Path DC Gain</td>
<td>31dB</td>
</tr>
<tr>
<td>Complete Main Path System Gain</td>
<td>70dB</td>
</tr>
<tr>
<td>Return Loss (S11) 2.11GHz-2.17GHz</td>
<td>&lt;-13dB</td>
</tr>
<tr>
<td><a href="mailto:IIP2@1.98GHz">IIP2@1.98GHz</a></td>
<td>+58dBm</td>
</tr>
<tr>
<td>Uncorrected IIP3 @1.98GHz/2.05GHz</td>
<td>-7.1dBm</td>
</tr>
<tr>
<td>Effective <a href="mailto:IIP3@1.98GHz">IIP3@1.98GHz</a>/2.05GHz</td>
<td>+5.3dBm</td>
</tr>
<tr>
<td><a href="mailto:ICP1@1.98GHz">ICP1@1.98GHz</a></td>
<td>-19dBm</td>
</tr>
<tr>
<td>Analog Die LNA+Main Path NF</td>
<td>5.0dB</td>
</tr>
<tr>
<td>Complete System NF</td>
<td>5.5dB</td>
</tr>
<tr>
<td>Analog Die Supply Voltage</td>
<td>1.2V/2.7V</td>
</tr>
<tr>
<td>Analog Die LNA+Main Path Current</td>
<td>28mA (1.2V)</td>
</tr>
<tr>
<td>Analog Die Alternate Path Current</td>
<td>6.7mA (1.2V)</td>
</tr>
<tr>
<td>Estimated Digital Alternate Path Current</td>
<td>5.6mA (1.0V)</td>
</tr>
<tr>
<td>Double-Sided Signal Bandwidth</td>
<td>3.82MHz</td>
</tr>
</tbody>
</table>
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Conclusions

• Feedforward IM3 cancellation improves IIP3 performance for a SAW-less UMTS receiver.
• Novel IM3 generation circuit was described and implemented to provide a suitable reference signal for equalization.
• Novel technique to overcome the limitation of the difference in IQ mismatches of the main and alternate paths is presented and successfully demonstrated.
• Techniques to deal with the interaction of DC offset with the adaptive equalization are also presented.
Acknowledgements

• Funding from NDSEG Fellowship Program and Lee Center for Advanced Networking.
• Frequency divider IP from F. Bohn of Caltech.
• Testing assistance by H. Mani and J. Yoo of Caltech.
• Chip fabrication from MOSIS.
• Copper plated dielectric substrate from Rogers Corporation.
• PCB gold plating from DVH Circuits.
• Advice from Profs. A. Emami and B. Hassibi of Caltech.
• Advice from H. Wang, Y. Wang, F. Bohn, S. Jeon, A. Babakhani, J. Chen, and M. Loh of Caltech.
• Advice from S. Kousai of Toshiba.
Adaptive Equalizer Operation

Output of Equalizer

![Graph showing the output of an equalizer with labels for Amplitude (LSB) and Sample. The graph includes three lines: blue for Original Signal, red for Output Signal + Error, and green for Error.]
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