A Scalable 6-to-18GHz Concurrent Dual-Band Quad-Beam Phased-Array Receiver in CMOS


California Institute of Technology
Outline

- Introduction
  - Proposed Concurrent Phased-Array System
  - 6-to-18GHz Phased-Array Receiver
  - Test Setups and Experimental Results
  - Conclusion
Wideband Large-Scale Phased Arrays

Military radars

Space & satellite communications

Weather radars
**Phased Arrays**

- Coherent addition of signals from each element.
- Reject other signals with different incident angles.

\[ \Delta \varphi = \frac{2\pi}{\lambda} d \sin \theta \]
Advantages of Phased Arrays

- **Multi-beam scanning**
- **Interference rejection**
- **High array gain**
- **Fast scanning time**

SNR Improvement by $10 \log N$
Conventional Structure of Large-Scale Arrays

- Interconnection of separate modules.
- Compound-semiconductor MMICs.
- High cost and complexity
Outline

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➤ Proposed Concurrent Phased-Array System

- 6-to-18GHz Phased-Array Receiver

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Tunable Concurrent Multi-Beam Array

Concurrent dual-band quad-beam receiving

- $f_{LB}, \theta_1$
- $f_{HB}, \theta_2$
- $f_{LB}, \theta_3$
- $f_{HB}, \theta_4$

6-18GHz CMOS receiver

- HP: Horizontal polarization
- VP: Vertical polarization
- LB: Low band
- HB: High band

Easily scalable

Reference signal for PLL (50MHz)

- Required components reduced dramatically.
Features of Proposed Concurrent Array

- Easily scalable to build large-scale arrays.
  - Dramatically reduce number of components required.
  - Low cost, low complexity, more reliability.
- Wideband operation (6 – 18GHz)
- Concurrent dual-band quad-beam scanning.
  - LB (6 – 10.4GHz) and HB (10.4 – 18GHz)
  - Two polarizations.
- Phase noise improvement in large-scale arrays.
Phase Noise Improvement

- Phase noise improved by $10\log_{10}N$.
- On-chip frequency synthesizers acceptable for the phase noise requirement.

$S_{out} = N^2 \times S_{in}$
$PN_{out} = N \times PN_{in}$

• Signals added up in current domain.
• Uncorrelated phase noise added up in power.
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Receiver Architecture

HP: Horizontal polarization, VP: Vertical polarization, LB: Low band, HB: High band
Receiver Architecture

HP dual RF input (LB + HB) → TCA → RF mixer (LB) → IF buffer (LB) → IF mixer (LB, I) → Baseband VGA → BB out (LB, I)

RF mixer (HB) → IF buffer (HB) → IF mixer (HB, I) → BB out (HB, I)

IF mixer (LB, Q) → BB out (LB, Q)

IF mixer (HB, Q) → BB out (HB, Q)

LB: Low band, HB: High band
Receiver Architecture

HP: Horizontal polarization, VP: Vertical polarization, LB: Low band, HB: High band

- **RF input (LB + HB)**
- **RF mixer (HP_LB)**
- **RF mixer (HP_HB)**
- **IF buffer (HP_LB)**
- **IF buffer (HP_HB)**
- **Baseband VGA**
- **BB out (HP_LB, I)**
- **BB out (HP_LB, Q)**
- **BB out (HP_HB, I)**
- **BB out (HP_HB, Q)**
- **BB out (VP_HB, I)**
- **BB out (VP_HB, Q)**
- **BB out (VP_LB, I)**
- **BB out (VP_LB, Q)**

- **Data Clock Latch**
- **170 bits**
- **VCO (LB, 5 - 7GHz)**
- **VCO (HB, 9 - 12GHz)**
- **PLL (LB)**
- **PLL (HB)**
- **MUX**
- **Ref (50MHz)**
- **2.8V 1.6V Bandgap reference**
- **VP dual RF input (LB + HB)**

Receiver Architecture

HP: Horizontal polarization, VP: Vertical polarization, LB: Low band, HB: High band

VCO (LB, 5 - 7GHz) → PLL (LB) → MUX → Ref (50MHz) → PLL (HB) → MUX → VCO (HB, 9 - 12GHz)

RF mixer (HP_LB) → RF mixer (HP_HB) → Phase interpolators → IF mixers

RF mixer (VP_LB) → RF mixer (VP_HB)
Receiver Architecture

HP: Horizontal polarization, VP: Vertical polarization, LB: Low band, HB: High band
**Frequency Plan**

- LO2 switches between 1/2 and 1/8 of LO1, depending on IF frequency.
  - Performed by on-chip multiplexers.
  - Relax the required VCO tuning range.
Tunable Concurrent Amplifier (TCA)

- Single-input, dual-output.
- Tunable LC loads for two separate tuned amplifiers.
Mixers

- Current commuting double-balanced mixers.

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**Frequency Synthesizers**

**Architecture**

- Frequency generation step: 200MHz.
Digital Phase Rotators

- Phase and amplitude synthesis by summation of differently weighted I and Q.
- VGA by current-combining of binary-weighted Gilbert cells.
LO Distribution and Buffers

LO from Synth.

Differential grounded CPW lines ($Z_{\text{odd}}=50\Omega$)

LO to Mixers / Phase rotators (H-pol)

LO to Mixers / Phase rotators (V-pol)

$V_{\text{out}+}$ $V_{\text{out}-}$

$V_{\text{in}+}$ $V_{\text{in}-}$

$V_{\text{Bias}}$
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Test Setup for Receiver Element

- On-wafer probing for RF input.
- BB output taken differentially and converted to single-ended.
LO Generation

- Locking range:
  4.8 – 7.8GHz

- Locking range:
  8.8 – 12.5GHz
**RF Performance**

- Conversion gain = 16 ~ 24dB
- Pin_1dB = -25 ~ -15dBm
- IIP3 = -17 ~ -5dBm
- Discontinuities due to frequency band or scheme changes.
RF Input Matching

- Input matching insensitive to different TCA settings.
Noise Figure

- NF = 8 ~ 14dB across the entire band.
- 2.6 ~ 3.1dB, considering the preceding wideband GaN LNA in the active antenna module (2.5dB NF, 20dB Gain).
Isolation Performance

- Good isolations between two bands (more than 48dB) and between two polarizations (more than 62dB).
Phase Interpolation Performance

Measured constellation of interpolated baseband signal @18GHz

-1.2
-0.8
-0.4
0
0.4
0.8
1.2

Phase interpolation performance summary

<table>
<thead>
<tr>
<th>RF Freq.</th>
<th>Phase Error RMS</th>
<th>Phase Error Max.</th>
<th>Amp. Variation RMS</th>
<th>Amp. Variation Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>6GHz</td>
<td>0.5°</td>
<td>2.6°</td>
<td>0.4dB</td>
<td>1.9dB</td>
</tr>
<tr>
<td>10.4GHz</td>
<td>0.2°</td>
<td>1.2°</td>
<td>0.2dB</td>
<td>1.5dB</td>
</tr>
<tr>
<td>14GHz</td>
<td>0.3°</td>
<td>1.4°</td>
<td>0.2dB</td>
<td>1.7dB</td>
</tr>
<tr>
<td>18GHz</td>
<td>0.2°</td>
<td>1.3°</td>
<td>0.5dB</td>
<td>2.3dB</td>
</tr>
</tbody>
</table>
Array Test Setup

- RF source: HP83650B
- DAC
- 4-way 0° power splitter
- Tek 6604B
- 4-channel digital oscilloscope
- DC supply for BB buffer (1.5V)
- Digital prog. by LabView®
- DC supply (2.8V, 1.6V)
- 2-way 180° power combiner
- Bias tee
- LPF
- 2-way 180° power splitter
- Variable phase shifter
- 4-way 0° power splitter
- Crystal osc. (50MHz)
Array Patterns

Array patterns at 6GHz

Array patterns at 10.4GHz

Array patterns at 18GHz

- Peak-to-null ratio > 21.5dB
Phase Error Calibration

- One-time digital calibration of phase errors due to:
  - Mismatch, skews in ref signal distribution, element-by-element variation.
- On-chip phase shifting with fine resolution is essential.
Digital Modulation Performance

- Modulation format: QAM32 @ 10.4GHz carrier.
- EVM improved in array.
  - I & Q mismatch improved after signal combining.
  - SNR improved after signal combining.
Interference Rejection

- Desired signal: QPSK with 4Msps @ 10.4GHz, Pin = −35dBm, Incident angle fixed.
- Interference signal: FM with 100kHz @ 10.4GHz, Pin = −45dBm, Incident angle swept.
- Interference signal almost rejected at null positions.
## Performance Summary

### Receiver Element Performance

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conversion gain (6 – 18GHz)</td>
<td>15.7 ~ 24.7dB</td>
</tr>
<tr>
<td>Input-referred 1-dB compression (6 – 18GHz)</td>
<td>-25.9 ~ -14.7dBm</td>
</tr>
<tr>
<td>Input-referred IP3 (6 – 18GHz)</td>
<td>-17.0 ~ -5.2dBm</td>
</tr>
<tr>
<td>Input return loss (6 – 18GHz)</td>
<td>&gt; 9.5dB</td>
</tr>
<tr>
<td>Cross-polarization rejection (6 – 18GHz)</td>
<td>&gt; 63.4dB</td>
</tr>
<tr>
<td>Cross-band rejection (6 – 18GHz)</td>
<td>&gt; 48.8dB</td>
</tr>
<tr>
<td>LO leakage (6 – 18GHz)</td>
<td>&lt; -24.5dBm</td>
</tr>
<tr>
<td>Antenna-to-baseband noise figure† (6 – 18GHz)</td>
<td>2.6 ~ 3.1dB</td>
</tr>
<tr>
<td>Phase shifting resolution (6 – 18GHz)</td>
<td>&lt; 5° (within 2dB amplitude variation)</td>
</tr>
<tr>
<td>RF channel spacing</td>
<td>225MHz (Div8 LO₂), 300MHz (Div2 LO₂)</td>
</tr>
<tr>
<td>Power consumption</td>
<td></td>
</tr>
<tr>
<td>RF and LO circuitry</td>
<td>658mA @2.7V, 217mA @1.6V</td>
</tr>
<tr>
<td>Baseband buffers</td>
<td>328mA @1.5V</td>
</tr>
<tr>
<td>Technology</td>
<td>130nm CMOS</td>
</tr>
<tr>
<td>Die area</td>
<td>3.0×5.2 mm²</td>
</tr>
</tbody>
</table>

### Phased-Array Performance (4 elements measured at 6-, 10.4-, and 18-GHz)

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of beams concurrently receivable</td>
<td>4</td>
</tr>
<tr>
<td>Phase shifting resolution per element</td>
<td>&lt; 5°</td>
</tr>
<tr>
<td>Total phased-array gain</td>
<td>&gt; 27.7dB</td>
</tr>
<tr>
<td>Beam-forming peak-to-null ratio</td>
<td>&gt; 21.5dB</td>
</tr>
</tbody>
</table>
Conclusions

- The first tritave dual-band quad-beam phased-array receiver element in CMOS.
- RF front-end integrated from RF, LO to baseband.
- Easily scalable toward very large-scale phased arrays with low cost and high reliability.
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