Growth of vertically aligned Si wire arrays over large areas (>1 cm^2) with Au and Cu catalysts

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Arrays of vertically oriented Si wires with diameters of 1.5 μm and lengths of up to 75 μm were grown over areas >1 cm^2 by photolithographically patterning an oxide buffer layer, followed by vapor-liquid-solid growth with either Au or Cu as the growth catalyst. The pattern fidelity depended critically on the presence of the oxide layer, which prevented migration of the catalyst on the surface during annealing and in the early stages of wire growth. These arrays can be used as the absorber material in novel photovoltaic architectures and potentially in photonic crystals in which large areas are needed. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2779236]

Photovoltaic devices designed to achieve high cell efficiency with low-quality materials must have optically thick absorber layers, yet must simultaneously allow efficient collection of low diffusion length charge carriers. An attractive approach involves an array of vertically aligned semiconducting wires to enable carrier collection in the wires' radial direction, a distance that is short relative to their optical thickness (i.e. length).[1] Well-defined wire arrays have been produced using lithographic patterning followed by anisotropic etching,[2,3] but such methods require large areas of high-quality substrate materials. In contrast, wires of various materials[4] have also been grown 'bottom up' by the vapor-liquid-solid (VLS) process.[5] Control of the size and position of VLS-grown wires has been demonstrated,[6,7] particularly in the case of Si by patterning of a surface oxide.[8–10] Wire array growth, however, has only been achieved over relatively small areas, unless a template is used.[11] We demonstrate herein the VLS growth of arrays of Si wires having diameters of 1.5 μm and lengths of >70 μm, with very low defect densities, over areas >1 cm^2, without the use of a template.

Attempts to grow Si wire arrays did not yield high pattern fidelity when the catalyst was not confined. Wires were grown by photolithographically patterning S1813 photoresist (Microchem) on a clean Si(111) wafer, then exposing it for 5 s to buffered HF(aqueous) (Transene, Inc., 9% HF, 32% NH_4F), followed by evaporation of 500 nm of Au and lift-off of the resist. This produced a square array of 3 μm diameter Au islands with a center-to-center pitch of 7 μm. Samples were then annealed in a tube furnace at 900–1000 °C for 20 min under 1 atm of H_2 at a flow rate of 1000 SCCM (SCCM denotes cubic centimeters per minute at STP), followed by wire growth under 1 atm of H_2 and $SiCl_4$, at flow rates of 1000 and 20 SCCM, respectively. This produced arrays of low fidelity, with no control over the wire diameter or wire position (not shown). Examination of the samples after a 20 min H_2 anneal only revealed that this behavior was due to substantial agglomeration of the catalyst (Fig. 1).

The successful production of large-area Si wire arrays involved the use of an oxide buffer layer to confine the VLS catalyst to the desired areas in the pattern. To implement this approach, a 300 nm oxide was thermally grown on Si(111) wafers and then photolithographically patterned as described above. The oxide within the patterned resist holes was removed by immersion of the samples for 4 min in buffered HF(aqueous). The desired catalyst islands, now separated by a buffer oxide, were then formed by thermal evaporation of 500 nm of either Au or Cu, followed by lift-off of the resist. These samples were then annealed in a tube furnace at 850–1100 °C for 20 min under 1 atm of H_2 at a flow rate of 1000 SCCM. Wires were then grown for up to 30 min at 850–1100 °C with the same pressure and $SiCl_4/H_2$ flow-rates as for the samples with no oxide.

This approach produced nearly defect-free arrays that exhibited an extremely narrow diameter and length distribution, and highly controlled wire position (Fig. 2). The wire growth was very uniform over areas >1 cm^2, with the sample size currently limited by the diameter of our tube furnace. The growth uniformity declined within several hundred microns of the edges of the sample, presumably due to differences in temperature and/or gas flow at such locations. Transmission electron microscopy of the Au-catalyzed Si wires indicated that wires were single crystalline and grew

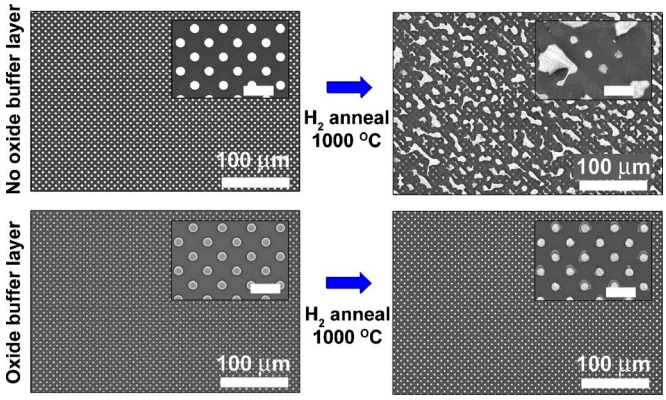

FIG. 1. (Color online) Effect of a 20 min anneal in H_2, at 1000 °C and atmospheric pressure, on Au arrays with and without a 300 nm oxide buffer layer, demonstrating the importance of the buffer oxide in maintaining the pattern fidelity. The scale bars in the insets are 10 μm.

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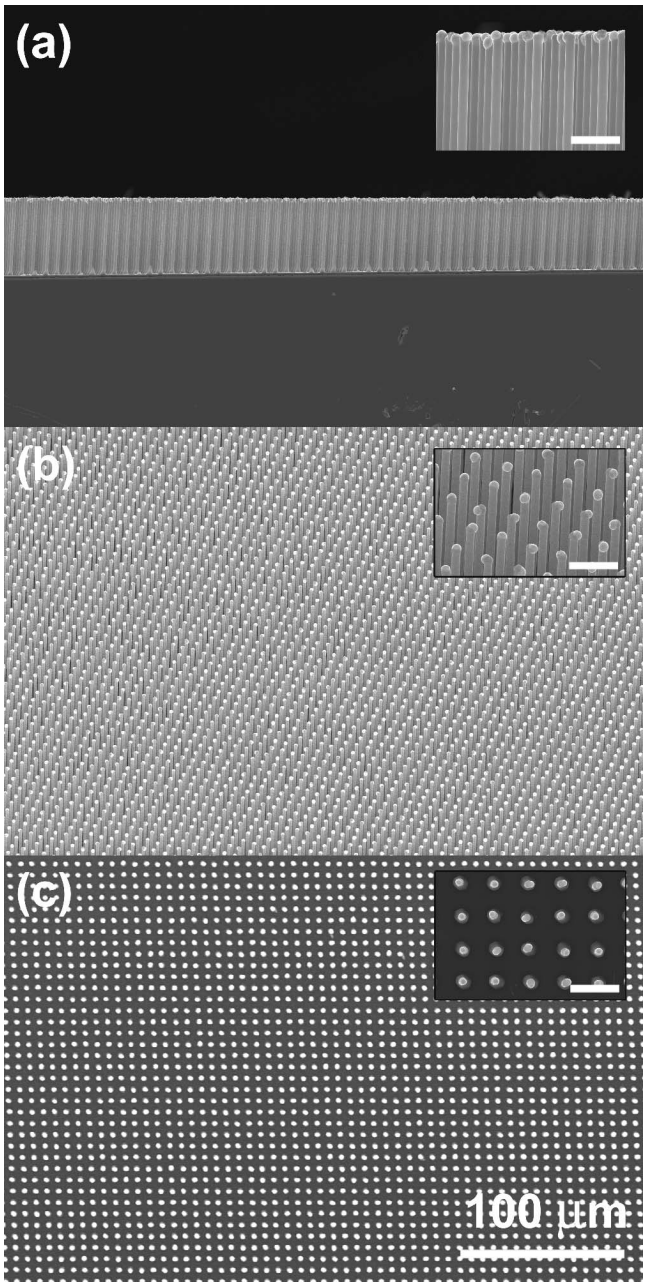

FIG. 2. (a) Edge-on, (b) tilted, and (c) top-down scanning electron microscopy (SEM) views of a Au-catalyzed Si wire array having nearly 100% fidelity over a large (>1 cm^2) area. The 100 μm scale bar applies to all three panels, and in all cases the scale bar in the insets is 10 μm.

along the [111] direction [Fig. S1 (Ref. 12)]. Nominally identical wire arrays were produced when Cu was used as the VLS catalyst instead of Au (Fig. 3). Figure S2 of Ref. 12 shows regions near each of the four corners of a 0.5 cm^2 sample grown with a Cu catalyst, and illustrates the uniformity achieved over large areas.

To characterize the electrical properties of the Si wires, four-point probe and field-effect measurements were performed on individual wires in the arrays. For these measurements, the as-grown wires were removed from the growth substrate by sonication in isopropanol and were then deposited on a degenerately doped silicon wafer that had been coated with 100 nm of Si_3N_4. The four-probe electrodes were fabricated using photolithography, followed by evaporation of 300 nm of Al and 900 nm of Ag, and finally by lift-off of the resist. Annealed Al was observed to make suitable ohmic contacts to the wires. Back-gated measurements indicated that the as-grown wires were *n* type, with a resistivity of 0.1–0.6 Ω cm, corresponding to dopant densities of 8×10^{15}–5×10^{16} cm^{-3} [Fig. S3 (Ref. 12)],[13] assuming that the carrier mobility in these wires is the same as that in bulk Si.

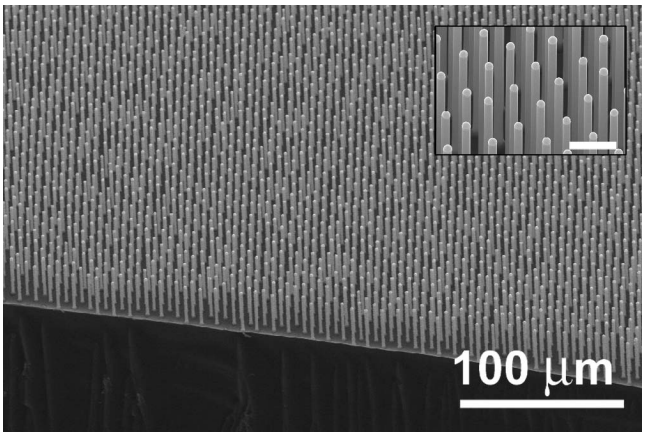

FIG. 3. Tilted SEM views of a Cu-catalyzed Si wire array having nearly 100% fidelity over a large (>1 cm^2) area. The scale bar in the inset is 10 μm.

Si nanowires have been grown previously at 800–900 °C with $SiCl_4/H_2$,[14,15] but the Si microwires described herein had optimal growth temperatures of 1000–1050 °C. At 950 °C and below, the wires either did not grow straight, grew intermittently straight with kinks, or grew straight but not aligned normal to the substrate (not shown). This difference in optimal growth temperatures between Si nanowires and Si microwires is not necessarily surprising because size-dependent effects have been observed for other aspects of VLS growth.[16] At 1075 °C and above, the wires grew straight and normal to the substrate, but significant destruction of the surface oxide was observed during the growth process, leading to a loss of the pattern fidelity (Fig. S4 of Ref. 12). Furthermore, the required thickness of catalyst is proportional to the diameter of the wires being grown, so 500 nm of catalyst material was required to produce $\sim$1.5 μm diameter Si wires. We believe that this relatively thick catalyst layer, and/or the higher growth temperatures, led to a significant problem with catalyst migration if a buffer oxide was not present on the surface, in contrast to earlier reports in which much thinner catalyst layers were used.[14,15]

Device analysis has shown that photovoltaic efficiency is maximized in wire arrays when the mean radius of the wires is comparable to the minority carrier diffusion length.[1] This is because of a trade-off between increased current collection and the loss of open-circuit voltage due to the increased junction and surface area. Diffusion of gold into bulk silicon at our VLS growth temperatures of 1000–1050 °C leads to carrier lifetimes of >1 ns,[17] which combined with carrier mobilities expected for the observed dopant densities,[13,18] indicates minority carrier diffusion lengths of $\geqslant1$ μm. This is in agreement with our near-field scanning optical microscope measurements of the minority carrier diffusion length of Au-catalyzed Si wires.[13] As shown in the present work, photolithography is an ideal method for enabling uniform arrays of wires of this diameter to be grown over large areas. In cost-sensitive applications such as photovoltaics, it would ulti-

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mately be desirable to employ lower-cost lithographic methods, and the method reported here should be readily extendable to alternative patterning techniques such as nanoimprint lithography.[19]

Cost also motivates the use of non-Au catalysts for the VLS process. Cu has recently been reported as a vapor-solid catalyst for Si wire growth[20] and was mentioned much earlier as a VLS catalyst,[21] but to our knowledge, arrays of Cu-catalyzed wires have not yet been demonstrated. Cu is, unlike Au, an inexpensive, earth-abundant material,[22] and therefore of particular interest for this application. Although Cu is more soluble in Si than Au,[23] and is also a deep trap,[24] the literature suggests that Si solar cells are more tolerant of Cu contamination than of Au,[25,26] and thus we expect diffusion lengths of at least microns even in the case of Cu-catalyzed growth.

In summary, we have outlined a straightforward procedure to attain excellent control of the size, position, and uniformity of vertically aligned, large-area Si wire arrays. To illustrate the utility of these arrays in novel photovoltaic device designs, we have recently reported a Si wire photoelectrochemical cell.[27] We have also demonstrated operation of a single wire *p-n* junction Si solar cell.[13] We expect that these arrays may also be useful as photonic crystals. Finally, it should be possible to extend this methodology to alternative lithographic techniques, as well as to making wire arrays of materials that cannot currently be fabricated with top-down methods.

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