High Total Dose Tolerance of Prototype Silicon Nanocrystal Non-Volatile Memory Cells

Mihail P. Petkov, L. Douglas Bell, and Harry A. Atwater

***Abstract*—We report the first results pertinent to the high total dose tolerance of Si nanocrystal nonvolatile memory cells. The studied prototype nc–Si field effect transistors made by ion implantation retained virtually unchanged write/erase characteristics, typical for the two-state devices, to cumulative doses exceeding 15 Mrad(Si).**

***Index Terms*—Field effect transistors (FETs), nonvolatile memory (NVM).**

I. INTRODUCTION

RECENT rapid developments of nonvolatile memory (NVM) technologies, driven by the ever-increasing demand for mobile capabilities, benefit significantly space exploration missions. NVMs offer low power and high storage density solutions to NASA's generic needs, spanning both flight data systems and flight instruments. Radiation-hardened variants that can satisfy stringent operation requirements imposed by high radiation environments have attracted specific interest. The presently leading technology, flash memory, offers an appealing alternative to dynamic random access memories (DRAMs). It stands out with its complementary metal oxide semiconductor (CMOS) compatibility and scalability to extremely high density. However, its state-of-the-art radiation-hardened version carries significant limitations to missions operating in the Jovian environment (e.g., NASA's Jupiter Icy Moon Orbiter). Alternative technologies that are being developed for the general market are also under evaluation in the quest to find a feasible solution. Arguably, the most advanced among them are those utilizing magnetic-RAM (MRAM), ferroelectric-RAM (FRAM), phase-change-RAM (PCM, also known as chalcogenide or CRAM) cell elements, followed closely by nanocrystal silicon (nc–Si) and carbon nanotube (CNT) technologies. Other approaches using molecular, organic, ionic, optical, holographic, microelectromechanical systems (MEMS), etc., storage elements are also being considered.

With the exception of flash and nc–Si, the implementation of other NVM technologies is hindered by several factors. The integration of materials without prior use in CMOS processing is accompanied by incompatibility and cross-contamination issues, which are difficult to resolve and can plausibly give rise to future reliability problems. Aggressive cell-size (thereby storage density) scaling is also problematic for MRAM, FRAM, and CRAM.

Although different, the fundamental principals utilized for information storage in these new technologies can be reduced to changes in the local microstructural state. Ferroelectrics in FRAMs rely on two-state metastable atomic cell structure, magnetic domains are used in MRAMs, and a amorphous-to-crystalline phase change in CRAMs. In all cases, the change from one state to another is virtually insensitive to ionizing radiation; cell survivability for MRAM, FRAM, and CRAM has been demonstrated to total ionizing doses (TID) in excess of 1 Mrad(Si) [1]–[3]). Thus, these technologies are appealing to the radiation community, which can take advantage of the state-of-the-art, provided measures are taken to mitigate single event effects (SEE) resulting from ion strikes. The sensitive readout CMOS circuitry is likely to remain the "Achilles heel" of all NVM technologies. To add nc–Si and CNT to this family of viable NVM technologies for space use, their TID and SEE tolerance must be investigated. However, the relevant information existing to-date is scarce.

The present work reports experimental results pertinent to the evaluation of the nc–Si NVM technology performance in high TID radiation environments. We focused our attention on technology characteristics originating solely from the nanocrystal ability to sustain charging and discharging controlled by external potentials, which is the foundation of the nc–Si technology. All fabrication-specific variables, such as nanocrystal formation method, layout geometry, structure and size, are ignored.

II. BACKGROUND ON NC–Si TECHNOLOGY

A. Nanocrystal Fabrication Methods

1) Aerosol Method: This process [4] relies on Si aerosol generated by pyrolysis from silane in a continuous-flow reactor. Nanocrystals are grown by chemical vapor deposition, seeded randomly by homogeneous nucleation within the aerosol. The Si crystals are sintered to attain spherical shape with a diameter of approximately 3 nm. This process produces crystals with narrow size distribution, which can be further reduced by a subsequent time-of-flight mass selection. In a second reactor, a 1–2 nm thermal oxide shell is grown at $\sim 1100\,^{\circ}$C in dry oxygen. The

Manuscript received July 20, 2004; revised September 1, 2004. This work was supported by Intel, the Jet Propulsion Laboratory, California Institute of Technology under a contract with the National Aeronautics and Space Administration.

M. P. Petkov and L. D. Bell are with the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109 USA (e-mail: mihail.p.petkov@jpl.nasa.gov; lloyddoug.bell-ii@jpl.nasa.gov).

H. A. Atwater is with the T. J. Watson Laboratory of Applied Physics, California Institute of Technology, Pasadena, CA 91125 USA (e-mail: haa@caltech.edu).

Digital Object Identifier 10.1109/TNS.2004.839141

0018-9499/04$20.00 © 2004 IEEE

oxide shell is designed to provide sufficient isolation to prevent crystal-to-crystal charge tunneling between spheres in contact. This guarantees the independent charge storage on each Si nanocrystal [5]. A monolayer of such oxidized Si nanoparticles is deposited onto a thin tunneling dielectric (oxide, oxy-nitride, or high-k), covering the channel of a field effect transistor (FET). Thicker passivating layer (SiO_2 or FSG) is deposited on top of the crystals, which are thus integrated as a floating gate assembly of the FET.

2) Low-Energy Si Implantation: This method involves Si ion implantation into a bare oxide layer on Si substrates [6], [7], which produces a Si excess in the oxide. Subsequent high-temperature annealing drives the SiO_2 and Si phase separation. Random nucleation and diffusion-driven Oswald ripening combine to form Si nanocrystals with a relatively broad size distribution, spherical shape, and a depth profile similar to that of the initial implantation profile. The agglomeration of excess Si ions also results in the formation of pure oxide insulation, which prevents charge transfer between adjacent crystals. Since the Si substrate acts as an absorber for diffusing Si ions, a thin layer of pure SiO_2 is formed at the $Si - SiO_2$ interface. This serves as a tunneling layer in the final FETs.

3) Deep Si Implantation: This technique differs from the above [8], [9], as Si^+ ions are implanted deep into the substrate beyond the active region of a transistor. Thus the method can be applied to already fabricated conventional FETs. The key process is the smearing of the $Si - SiO_2$ phase boundary at the interface, which results from the atomic collisions triggered by the implanted ions and secondary recoils. Thus, three distinct regions are formed in the vicinity of the interface—a mixture of Si and SiO_2 phases, surrounded by narrow layers of Si-rich SiO_2 and O-rich Si, in which the excess atoms are in super-saturated solid solution (ssss). Upon high-temperature annealing phase separation reconstructs the original $Si - SiO_2$ interface; the excess O dissolves in the Si substrate, whereas the ssss-Si nucleates and grows into nanocrystals. These resulting crystals have a relatively narrow size distribution and remain separated from the Si substrate by the regrown SiO_2 layer at the interface, which acts as a tunneling layer.

4) Si Deposition Methods: This method [10] uses substrates with a deposited tunneling layer, on which small Si nanocrystals are grown, e.g., by molecular beam epitaxy. Surface forces and stresses at the $Si - SiO_2$ interface prevent the formation of a monolayer. Instead, Si "droplets" grow randomly nucleated into hemispherical shapes. A thick insulating layer is deposited to passivate the nanocrystals as in the aerosol method.

B. Nc–Si Technology Comparison

For best performance, the Si nanocrystals must be closely and uniformly spaced from the channel (for uniform tunneling barrier thickness), must have narrow size distribution (for well defined energy levels and thereby write/erase voltages), and must be sufficiently isolated from each other (to prevent charge cross-transfer). On the other hand, to be appealing for mass production, the fabrication process must be fast and inexpensive. The aerosol process produces devices with excellent performance characteristics, though its complexity and cost may be prohibitive for mass production. The deposition methods trade off crystal size distribution for higher cost efficiency. The hemispherical nanocrystal shapes facilitate faster write and erase times, but may cause increased leakage current. The deep Si implantation is a new technology, which has shown promising qualities. Its main attractions are the minimum added complexity (implantation after FET fabrication and annealing) and low cost, combined with well-defined charging characteristics. In comparison, the low-energy Si implantation method results in broad distributions of crystal sizes and tunneling layer thickness, which combine to hinder the FETs electrical performance. Nevertheless, its cost-effectiveness renders it especially suited for fundamental nc–Si technology investigations without accent on individual device performance.

C. Comparison With Flash Memory Technology

1) Electrical Performance: The nc–Si NVM technology shares many features with the conventional flash technology. Both use FET structure with isolated charge storage node(s), which is (are) charged or discharged by tunneling of "hot" carriers under externally applied electric field. Readout is performed by current-sensing of the field created by the stored charge on the floating gate(s). Therefore, regardless of the fabrication method, the nc–Si NVM technology can be considered a variant of the flash memory technology, in which the monolithic floating gate is replaced by multiple (millions of) Si nanocrystal floating gates. Consequently, all attractive features of flash—fast programming speed (using layered tunneling barriers), long charge retention time, small power requirement and small bit size enabling high device density—can be retained in nc–Si NVM. The distribution of the stored charge among many nodes can further add redundancy and enhance device reliability. For example, the effects of structural defects in the tunneling dielectric that can sustain a leakage path between the floating gate and the channel of a flash FET, are minimized; the malfunction of several crystals in the defect vicinity is not critical. This may prove important for localized hot-carrier-related damage, to which nc–Si FETs should be more resilient.

2) Performance in Radiation Environments: It can be argued that nc–Si NVM technology has *intrinsic* radiation tolerance to both TID and SEE effects, and built-in redundancy that is nonexistent in flash memory. This originates from the ability of the cell to maintain functionality with only a fraction of intact charge storage nodes, in contrast to a monolithic floating gate. A *statistical approach* of assessing bit status can thus be devised. Instead of "0" or "1," a nc–Si memory cell can take all values in between, proportional to the fraction of remaining charged crystals. The distinction between the two bit states can be brought down to, e.g., 0.1 (10% of the voltage corresponding to "1") or less, when suitable current sensing capabilities are engineered in the circuit. In this example, if the crystals within 90% of the cell area are rendered inactive (cannot store charge), the remaining 10% of the nanocrystals can store a sufficient amount of charge to maintain the "1" status.

TID effects are usually associated with a continuous evolution of electric fields originating from drift, diffusion and trapping of charge carriers. The resulting enhancements of localized electric fields may cause dielectric breakdown and permanent

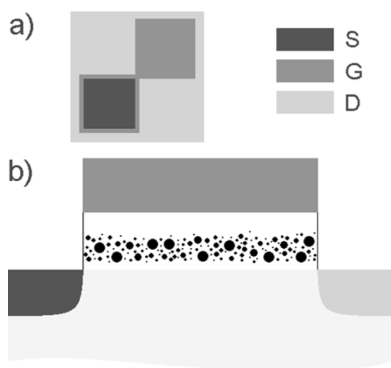

Fig. 1. (a) Ring-gate layout of the FETs used in this study. The source (S), gate (G) and drain (D) regions are shown with different colors (see legend). The large gate pad is inactive area used for metal contact deposition and wirebonding. (b) Schematic representation of a nc–Si FET cross-section; same color are used for S, G, and D. The nanocrystals, represented by differently sized dots, form the multi-node floating gate.

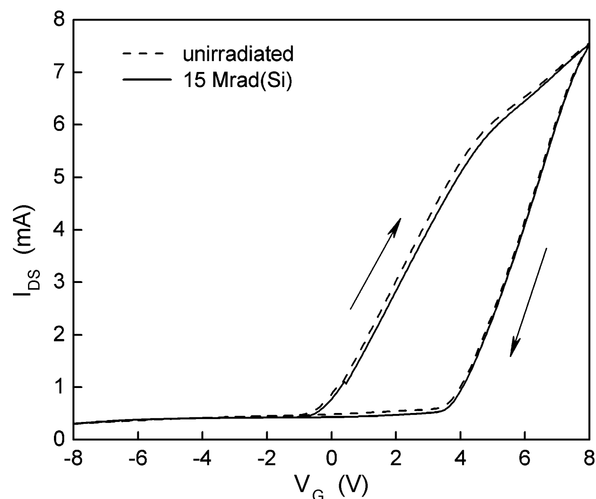

Fig. 2. Typical I_{DS} versus V_{G} characteristics of a nc–Si FET. The dashed curve shows that of a virgin FET, and the solid one—after exposure to a cumulative dose of 15 Mrad(Si).

device failure. Such localized damage to a small set of nanocrystals may not be critical for the functionality of the entire nc–Si cell.

Experimental measurements of cross-sections of ion tracks ([11] and theoretical models referenced therein) yield values of the order of 1 μm. This implies that the area hit by a single ion strike is unlikely to span the full area of a current-technology flash FET. In a conventional flash FET, the entire charge stored on a monolithic gate can be drained through the current path created by the ion track. In contrast, such discharge of nanocrystals in a nc–Si FET is limited to the cross-section area of the effective ion track; the charge stored on crystals that fall outside this area remain intact.

The above presents existing and plausible mechanisms that imply enhanced radiation tolerance of nc–Si NVM cells. It should be stressed, however, that further investigation is warranted as no direct experimental proof exists to-date. The possibility of retaining the good electrical characteristics and beneficial high-device-density potential of conventional flash NVM, while avoiding their vulnerability, is appealing for space applications.

III. Experimental

Nc–Si devices were fabricated by the method described in Section II-A2. $^{28}\mathrm{Si}^{+}$ ions were implanted at 5 keV to a fluence of $\sim 1.3\times10^{16}\ \mathrm{cm}^{-2}$ into a bare 15 nm-thick $\mathrm{SiO_2}$ layer, grown on top of p-type doped Si wafer. An ion implantation profile calculated by TRIM [12] using these data shows a peak depth of ~10 nm and a stoichiometry at the peak of $\mathrm{Si_{1.75}O_2}$. A calculated small fraction of the implanted ions (<5%) reach the Si substrate. The wafers were annealed at $\sim 1050^{\circ}\mathrm{C}$ for 5 min in dry oxygen, during which time the nanocrystals were formed and the majority of the implantation-induced defects were annealed out. An optically transparent 50 nm poly-Si gate was deposited on top of the wafers. Device patterning was done using a single-mask dry-etching process, followed by co-doping of the source (S), drain (D) and gate (G) regions to achieve metallization. Fig. 1 shows the ring-gate shaped layout of the FETs and a schematic representation of the cross-section. The dimension of the gate area was identical, 1000 × 1000 $\mu\mathrm{m}^2$, while the gate width was 1, 5, 10, 50, 100, and 500 μm for properties scaling purposes. Conventional FETs with identical layout and processing steps, excluding the Si^{+} implantation and subsequent annealing stages, were also made as control devices. They were used as reference standards in the radiation tests. Gold contacts deposited on the gate pads (Fig. 1(a)) were used for wirebonding of groups of 18 FETs in ceramic packages.

Radiation experiments were carried out using the $^{60}\mathrm{Co}$ in-house radiation facilities at the Jet Propulsion Laboratory. Preliminary tests indicated high tolerance to TID. This required long exposure time, for which the charge retention without refreshing was deemed unsatisfactory. Thus we focused on dynamic tests to assess the nc–Si FET ability to function as memory elements after prolonged exposure. Two different conditions were used: (1) S—common; $V_{\mathrm{DS}} = 1.5$ V; $V_{\mathrm{G}} = \pm 6$ V (write/erase square wave potential), and (2) all contacts grounded. They yielded indistinguishable results for the duration of the experiments, in which the maximum achieved dose was 15 Mrad(Si). (Continuation to higher doses did not appear to add significant value.) Changes in the FETs characteristics were traced by gate threshold voltage $(V_{\mathrm{G-th}})$ measurements (both written and erased states for the nc–Si FETs).

IV. Results and Discussions

A typical I_{DS}-V_{G} curve of a nc–Si FET is shown in Fig. 2. As in a floating gate of a flash FET, a large positive potential charges the crystals by hot electron injection through tunneling from the open transistor channel. Conversely, a large negative potential repels the electrons stored on the crystals. The controlled localization of charge in the body of the oxide translates into an ability to control the electric field at the channel by the charge stored on the nanocrystals. That charge offsets the electric field at the channel, which results in the hysteresis I_{DS}-V_{G} curve. The hysteresis is the fingerprint of a memory function—it sets a range of V_{G} values for which the FET is either open or closed, thereby defining a two-state device. The studied FETs exhibited moderate differences in the width and height of the hysteresis,

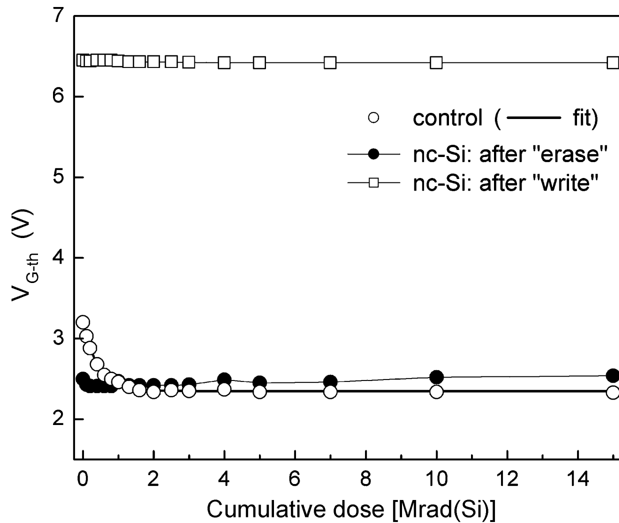

Fig. 3. Gate threshold voltage ($V_{\mathrm{G-th}}$) for a control FET (open symbols) as a function of the cumulative TID; the line is an exponential fit to the data. The gate threshold voltages for the erased and written states of a nc–Si FET are also shown with solid circles and open squares, respectively.

which carried little relevance to our investigation that focused on trends, not absolute values.

Fig. 2 also compares the typical hysteresis of a device prior to and after ^{60}Co irradiation. This test was conducted on 15 nc–Si FETs with write/erase square wave potential applied to the gate. The electrical characteristics of all transistors were virtually unchanged as in the given example.

Another set of 6 nc–Si FETs and three conventional FETs was exposed to ionizing radiation environment with all contacts grounded. Fig. 3 depicts the measured $V_{\mathrm{G-th}}$ for the written and erased state of a nc–Si FET and a control FET with identical dimensions. The control n-channel FET yielded decreasing $V_{\mathrm{G-th}}$ with dose, notably below $\sim$1 Mrad(Si). This is consistent with the accepted models for degradation of metal-oxide-silicon structures under irradiation [13]. The lack of change at $>$2 Mrad(Si) doses is attributed to saturation of interface defect generation and hole trapping.

Somewhat surprisingly, both $V_{\mathrm{G-th}}$ of the nc–Si FET show no significant changes in the entire test range of up to 15 Mrad(Si). This can be ascribed to the ion-implantation-induced damage [14] and the subsequent reconstruction of the oxide. Oxide properties, especially these related to defect density, charge trapping and mobility, can differ greatly prior to implantation and after reconstruction. Hence, for nc–Si technologies that do not utilize implantation, we can expect to observe a shift of the $V_{\mathrm{G-th}}$ (erased state) upon radiation exposure, as in conventional FETs. (This similarity originates from the fact that in neither case is charge stored on the body of the oxide except trapped at defects states.) For the written state of a nc–Si FET, electron localization at the nanocrystals is unlikely to be affected by the defects in the $\mathrm{SiO_2}$. It can thus be speculated that for all nc–Si technologies changes of $V_{\mathrm{G-th}}$ for the written state are not expected to occur during exposure to ionization environments. Therefore, the nc–Si NVM technology appears highly immune to ionization radiation.

The gate threshold voltage data in Fig. 3 were taken at the second erase-write-erase cycle after irradiation. There was ev-

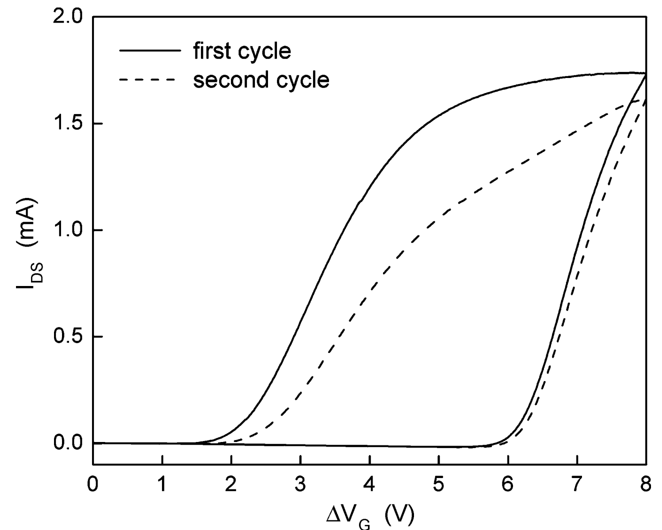

Fig. 4. Differences between the hysteresis characteristics of the firsts and second erase-write-erase cycle after irradiation at 10 Mrad(Si). The first and second measurements are shown with dashed and solid lines, respectively. Subsequent cycles carry no evidence of further changes.

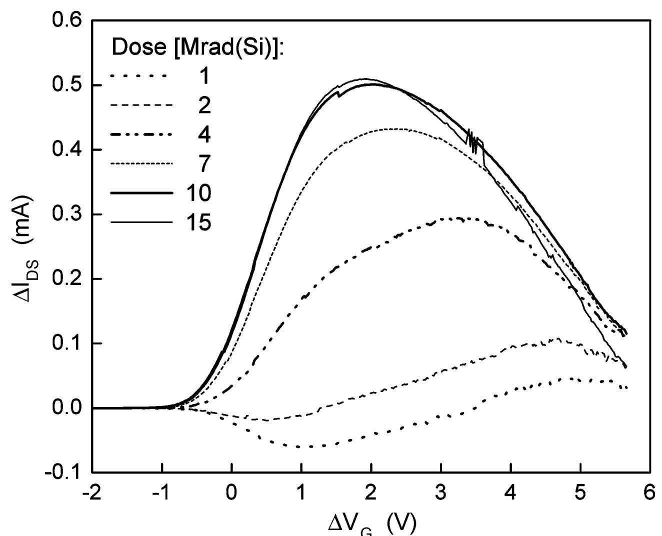

Fig. 5. Difference between the first and second erase-write-erase cycle (curves shown in Fig. 4), ΔI_{DS}, with respect to the "erase" gate threshold voltage, $\Delta V_{\mathrm{G-th}}$. The different curves give the results for nc–Si FET exposure to different TID values.

idence of charge trapping in shallow and deeper defect states, probably contained in the $\mathrm{SiO_2}$. This acted to shift the threshold V_{G} for the erased state to lower values as shown in Fig. 4. The second cycle virtually recovered the pre-irradiation conditions and subsequent cycles exhibited no further change. Some fraction of the charge accumulated at the traps during the irradiation leaked out in the first several minutes. We found that measurements done at one to several hours after irradiation were repeatable, which is the signature of charge localized in deeper traps (for available levels see, e.g., [15]). The calculated differences between the I_{DS}-V_{G} curves of the erase-write legs of the first and second cycle for different doses are shown in Fig. 5. The abscissa gives the difference with respect to $V_{\mathrm{G-th}}$ for the erased state. Since the first cycle empties these charge traps, the horizontal is a representation of the energy level of the defect in the

oxide, whereas the vertical scale is a measure of the defect density. The data infer saturation of defect formation and/or charge trapping at approximately 10 Mrad(Si), while the electric field needed to delocalize the charge exceeds several MV/cm.

Further investigation of this effect is warranted. It should be stressed, however, that the trapped charge does not diminish the performance of a nc–Si memory cell, as it leads to an increased I_{DS} and wider hysteresis.

V. Conclusion

In this paper we presented the first experimental investigation of the radiation tolerance of nc–Si NVM technology to ionizing radiation. As this is novel technology is in its early stages of development, we focused on qualitative assessments, which would be relevant to the technology itself and not the actual prototype devices. Thus, the same behavior should be expected for Si nanocrystal NVM made by other methods. We demonstrated a virtually unchanged dynamic performance of the nc–Si memory cells (FETs) of up to 15 Mrad(Si). The present results, in conjunction with the inherent benefits of flash NVM technology, make nc–Si NVM an appealing candidate for use in high radiation environments. Further investigations are anticipated for adequate comparison to other more advanced competing NVM technologies. Recent industrial developments in this field (Motorola announcement of 4 Mbit multi-domain flash NVM process; 2003) further enhance the potential for applications in space missions.

References

[1] S. Bernacki, K. Hunt, S. Tyson, S. Hudgens, B. Pashmakov, and W. Czubatyj, "Total dose radiation response and high-temperature imprint characteristics of chalcogenide based RAM resistor elements," *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 2528–2533, Dec. 2001.

[2] R. Sinclair and R. Beech, "High speed, radiation hard MRAM buffer," in *Proc. Non-Volatile Memory Technology Symp.*, Honolulu, HI, Nov. 4–6, 2002.

[3] S. C. Philpy, D. A. Kamp, A. D. DeVilbiss, A. F. Isaakson, and G. F. Derbenwick, "Ferroelectric memory technology for aerospace applications," in *Proc. IEEE Aerospace Conf.*, vol. 5, 2000, pp. 377–383.

[4] M. L. Ostraat *et al.*, "Synthesis and characterization of aerosol silicon nanocrystal nonvolatile floating-gate memory devices," *Appl. Phys. Lett.*, vol. 79, no. 3, pp. 433–435, 2001.

[5] E. A. Boer *et al.*, "Localized charge injection in $\mathrm{SiO_2}$ films containing silicon nanocrystals," *Appl. Phys. Lett.*, vol. 79, no. 6, pp. 791–793, 2001.

[6] E. Kapetanakis, P. Normand, D. Tsoukalas, K. Beltsios, J. Stoemenos, S. Zhang, and J. van den Berg, "Charge storage and interface states effects in Si-nanocrystal memory obtained unisng low-energy $\mathrm{Si^+}$ implantation and annealing," *Appl. Phys. Lett.*, vol. 77, no. 21, pp. 3450–3452, 2000.

[7] O. González-Varona, B. Garrido, A. Pérez-Rodríguez, C. Bonafos, J. Montserrat, and J. R. Morante, *Solid State Phenom.*, vol. 80–81, p. 243, 2001.

[8] T. Müller, K.-H. Heinz, and W. Möller, "Size and location control of Si nanocrystals at ion beam synthesis in thin $\mathrm{SiO_2}$ films," *Appl. Phys. Lett.*, vol. 81, no. 16, pp. 3049–3051, 2002.

[9] ——, "Nanocrystals formation in Si implanted thin $\mathrm{SiO_2}$ layers under the influence of an absorbing interface," *Mater. Sci. Eng. B*, vol. 101, no. 1, pp. 49–54, 2003.

[10] S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbe, and K. Chan, "A silicon nanocrystals based memory," *Appl. Phys. Lett.*, vol. 68, pp. 1379–1381, 1996.

[11] O. Misseau *et al.*, "Technique to measure an in track profile," *IEEE Trans. Nucl. Sci.*, vol. 45, pp. 2563–2570, Dec. 1998.

[12] J. F. Ziegler, J. P. Biersack, and U. Littmark, *The Stopping and Range of Ions in Solids*. New York: Pergamon, 1985.

[13] P. M. Lenahan and J. F. Conley, "A comprehensive physically based predictive model for radiation damage in MOS systems," *IEEE Trans. Nucl. Sci.*, vol. 45, pp. 2413–2423, December 1998.

[14] C. J. Nicklaw *et al.*, "Defects and nanocrystals generated by Si implantation into a-$\mathrm{SiO_2}$," *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 2269–2275, Dec. 2000.

[15] C. J. Nicklaw, Z.-Y. Lu, D. M. Fleetwood, R. D. Schrimpf, and S. T. Pantelides, "The structure, properties, and dynamics of oxygen vacancies in amorphous $\mathrm{SiO_2}$," *IEEE Trans. Nucl. Sci.*, vol. 49, pp. 2667–2673, Dec. 2002.