A Versatile Pseudo-Random Noise Generator

EDWARD D. LIPSON, KENNETH W. FOSTER, AND MICHAEL P. WALSH

Abstract—**A detailed design is presented for a digital pseudo-random noise generator. The instrument is built with standard integrated circuits. It produces both binary noise (pseudo-random binary sequences) and white Gaussian noise of variable bandwidth. By setting front panel switches to match tabulated octal codes, one may select a vast number of independent noise programs.**

INTRODUCTION

RANDOM NOISE is widely and increasingly used as a signal for the testing and identification of physical and biological systems. In particular white Gaussian noise is becoming popular for the determination of the Wiener kernels [1], [2] of nonlinear biological systems [3]–[5].

Physical devices such as resistors and diodes are sometimes used as sources of random noise. However such devices suffer from statistical variability between finite samples of their noise output. Moreover unless special procedures are undertaken [6] physical noise sources are generally unsuitable for low-frequency applications.

Often it is adequate, or even advantageous, to employ deterministic (and reproducible) periodic signals with the essential statistical properties of random noise. Such pseudo-random noise may be generated by computers, or by electronic instruments such as that described here.

BACKGROUND ON PSEUDO-RANDOM SIGNALS

Pseudo-random binary sequences (PRBS; also known as maximal length binary sequences, binary m-sequences, and chain codes) are generated in practice by a *feedback shift register* [7], [8]. In such a device the next input value (bit) is determined as follows. A parity check (or mod-2 addition, or EXCLUSIVE-OR operation) is performed on the values in a fixed subset of the stages of the shift register. The result is fed back to the input.

If the feedback length (i.e., highest order feedback stage) of the shift register is n, then there are 2^n possible states of the feedback shift register as a whole. One special state, namely all zeros, is disallowed since it would be self-perpetuating. In general, the remaining $2^n - 1$ states may be generated periodically in sequence in a number of independent patterns. In such a case, the sequence of $2^n - 1$ bits observed in any given stage constitutes a maximal length or PRBS.

Only certain feedback configurations produce PRBS's. In general, the configuration of a feedback shift register may be represented algebraically by a polynomial over the Galois field with two elements (GF(2)) [9]. For example, the polynomial $X^8 + X^4 + X^3 + X^2 + 1$ represents a shift register with feedback from stages 2, 3, 4, and 8. The degree of the polynomial, here 8, is equivalent to the feedback length n of the shift register. Those feedback configurations which produce PRBS's correspond to polynomials which are "irreducible" and "primitive" [7]. Using a compact octal code, Peterson and Weldon [9] have tabulated irreducible polynomials up to degree 34. In their tabulation, only those polynomials with suffixes *E*, *F*, *G*, and *H* are primitive.

For the example above the octal code is 435, corresponding to the binary code 100011101. The binary code in turn represents the above polynomial, written explicitly as $1{\cdot}X^8 + 0{\cdot}X^7 + 0{\cdot}X^6 + 0{\cdot}X^5 + 1{\cdot}X^4 + 1{\cdot}X^3 + 1{\cdot}X^2 + 0{\cdot}X^1 + 1{\cdot}X^0$. Note that in the shift register, there is no stage corresponding to the zero-order term.

On the front panel of the instrument described here, the operator may dial in an octal code of up to seven digits to produce any feedback configuration with feedback length $n \leq 20$. Thus, in particular, one may generate easily the PRBS for every allowed octal code up to degree 20. A row of 20 lamps is available to display either the binary feedback code or the last 20 values of the ongoing PRBS. By means of a special synchronization signal (*sync*), described later, one may determine whether or not any given octal code produces a PRBS.

PRBS's have a number of properties which qualify them as substitutes for random binary signals [7]. The properties include (periodic) impulse-like autocorrelation functions, equality of the number of occurrences of the high and low states (actually there is an excess of one high), and an exponentially decreasing distribution of lengths of consecutive runs of high (or low) states.

The power spectrum of a PRBS with a clock interval Δt (for the shift register) is a line spectrum, because of the periodicity of the PRBS. The harmonic separation of the lines is $\Delta f = 1/N\Delta t$. The envelope of the line spectrum is proportional to sinc $^2f(t)$ [10]. [Note: sinc $(X) \equiv \sin(\pi X)/(\pi X)$.] Thus the spectrum is approximately flat (within 3 dB) up to $f = 1/3\Delta t$.

By means of filtering, PRBS's may be elaborated into pseudo-random waveforms with a variety of statistical and spectral properties. Analog low-pass filtering pro-

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E. D. Lipson and M. P. Walsh are with the Division of Biology, California Institute of Technology, Pasadena, CA 91125.

K. W. Foster was with the Division of Biology, California Institute of Technology, Pasadena, CA. He is now with the Department of Molecular, Cellular and Developmental Biology, University of Colorado, Boulder, CO 80302.

duces continuous waveforms. Digital filtering produces multilevel step waveforms, which may approximate continuous waveforms. Analog filtering suffers from a number of disadvantages. If one changes the clock interval Δt, the characteristics of the analog filter must be modified, generally not a simple matter. Moreover, analog filters are unsuitable for low-frequency applications, such as the one in which the present instrument was used [5].

These disadvantages are overcome by digital filtering. The availability of the shift register as a digital delay line makes digital filtering very simple [11]. One need only perform a weighted sum of the contents of the shift register stages. The digital filter characteristics scale automatically when the clock interval is changed, such that the waveform remains unchanged in shape. The weighting function applied here to the 32-stage shift register is a truncated sinc (X) function [10], [12]. This choice approaches the ideal of a rectangular low-pass filter. The resultant band-limited white Gaussian noise is just of the form needed for nonlinear system identification [2].

The instrument produces both pseudo-random binary noise and pseudo-random band-limited white Gaussian noise. It is built with TTL digital integrated circuits, as well as passive components and one integrated-circuit operational amplifier. It has been used to measure the Wiener kernels of the light-growth response system of *Phycomyces* [5]. The low bandwidth of that system (2.5×10^{-3} Hz) called for a noise generator capable of operation at very low frequency. The digital design of the instrument permits operation at arbitrarily low frequency.

Circuit Description

The general structure of the noise generator is shown in Fig. 1. The heart of the instrument is the *shift register* shown in the center. Given the present shift register contents and an (allowed) octal code, the *feedback generator* evaluates the next bit of the PRBS and delivers it to the input stage of the shift register. In addition, the feedback generator automatically starts the PRBS after the shift register has been cleared. To produce white Gaussian noise the PRBS is processed by a digital low-pass filter, consisting of the shift register itself in parallel with a suitably weighted digital-to-analog converter [12].

Assuming clock pulses are provided to the shift register, the central pathway of Fig. 1 produces both binary and Gaussian noise signals. The remaining elements are optional, depending on the application. The lamps indicate either the binary representation of the octal code (i.e., which stages are fed back) or the states of the first 20 stages of the shift register. The *sync* generator provides one pulse per period of the PRBS. This paper will not provide detailed designs of the active filter, clock, counter, or display since these are all standard and should be tailored to specific applications.

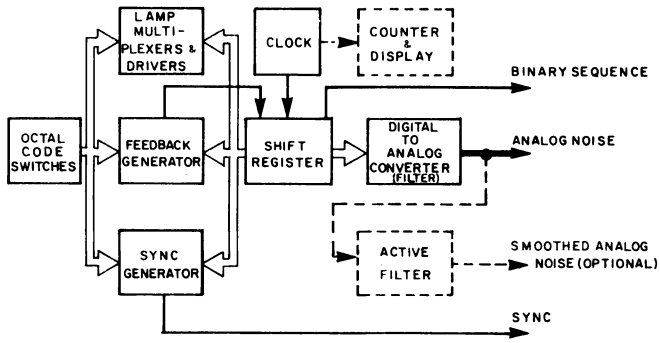


Fig. 1. Block diagram of noise generator. The dashed boxes are optional.

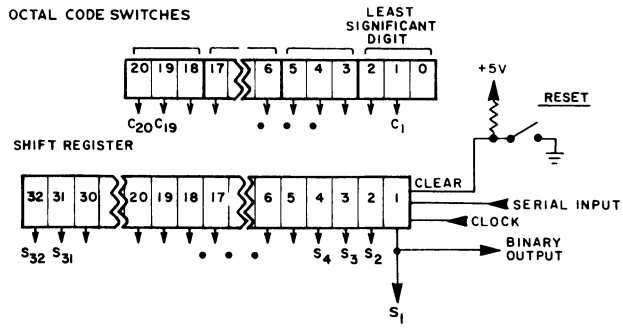


Fig. 2. Showing numbering conventions for outputs of 7 binary-coded octal switches (Digitran 8608) and 32-bit shift register (4 × SN74164 8-bit parallel-out serial shift registers).

Fig. 2 defines the signals and numbering conventions for the octal code, the shift register stages and the indicator lamps. The shift register is cleared by pressing the momentary reset switch. Positive clock pulses may be provided by an internal or external clock. In addition pulses may be applied by a switch to single step the binary sequence for testing. The *binary output* (PRBS) is taken from stage 1 of the shift register.

The feedback generator is shown in Fig. 3. (In this and the other circuit diagram, *positive* logic conventions are used.) According to the settings of the octal code switches, a subset of the bits C_i will be high. The AND gates ***A*** enable the corresponding shift register stages S_i to be tested by the parity checker. The result is fed back to the serial input (stage 1) of the shift register. The combination of the NOR gates ***C*** and the NAND gate ***D***, together equivalent to a 32-input OR, tests for the special case when *all* of the S_j are low. In this case (when all data inputs are low) the ODD and EVEN inputs to the parity checker are set high and low, respectively. This case does not occur during the normal generation of PRBS's. Without this feature, though, the instrument could get stuck (e.g., at turn on) with the shift-register in its all-zero state. Moreover this feature has two applications. By simply clearing (resetting) the shift register, the shift register (and thus the PRBS), regardless of the octal code, is *initialized* (at the next clock pulse) to a standard state with S_1 high and all other S_j low. In addition by simply setting the octal code switches all to zero, a single high state may be circulated re-

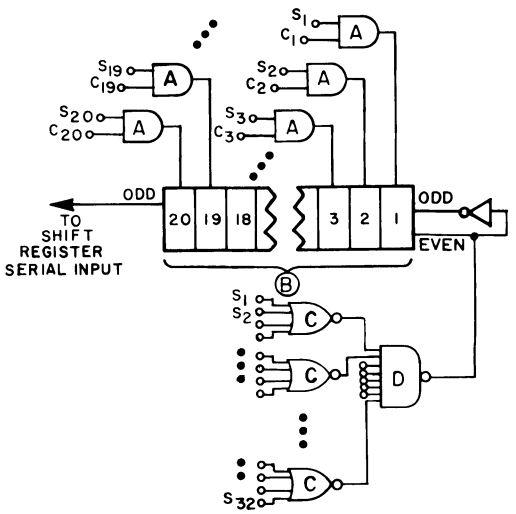


Fig. 3. Feedback generator. ***A:*** ¼ × SN7408 QUAD 2-input positive AND gates. ***B:*** 4 × SN74180 9-bit odd/even parity generators/checkers. ***C:*** ½ × dual 4-input positive NOR gates. ***D:*** SN7430 8-input positive NAND gate.

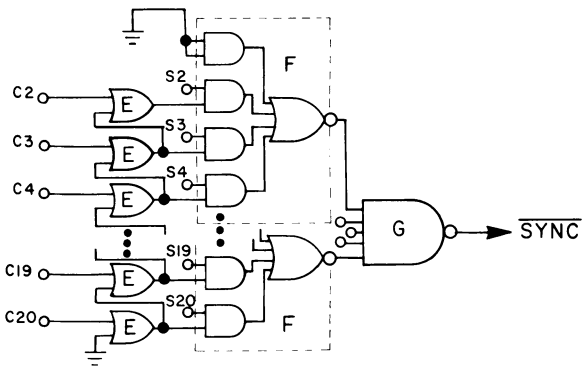


Fig. 4. Sync generator. ***E:*** ¼ × SN7432 quad 2-input positive OR gates. ***F:*** SN7453 expandable 4-wide AND-OR-INVERT gates. ***G:*** SN7430 8-input positive NAND gate.

peatedly through the shift register permitting testing and calibration of the weighting function of the digital filter (see below).

The *sync* generator is shown in Fig. 4. This circuit senses the condition when all stages of the shift register are low from stage 2 up to the highest order stage fed back. (Then for a PRBS, the first stage must necessarily be high.) If n is the degree of the octal code (i.e., feedback length of the shift register) then all OR gates ***E*** up to and including the one for C_n will have their outputs high. The AND-OR-INVERT gates ***F*** together with the NAND gate ***G*** then provide a negative pulse $\overline{\text{SYNC}}$ (with a width of one clock interval) when $(S_j|j = 2,\cdots,n)$ are all low.

The lamp circuit shown in Fig. 5 is straightforward. The bank of lamps has two functions selected via the multiplexer. One is to show the present contents of the first 20 stages of the shift register; in particular the reset state (all 0) is readily checked on the lamps. The other is to decode the octal code into binary to show which stages of the shift register are fed back. In particular, the highest lamp lit indicates the feedback length (degree) of the PRBS. These lamps proved very useful in the debugging of the instrument after construction.

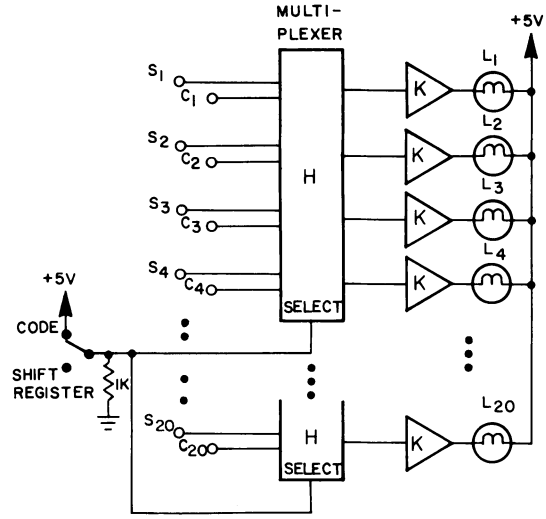
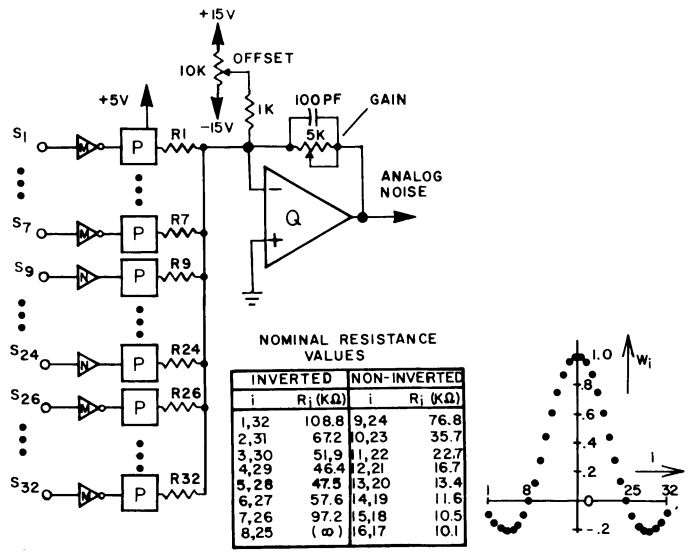


Fig. 5. Lamp multiplexers and drivers. ***H:*** SN74157 quad 2-line to 1-line data selectors/multiplexers. ***K:*** SN7407 hex buffer driver (open collector). ***L_i:*** Raytheon MC-680.



INVERTED		NON-INVERTED	
i	R_i (KΩ)	i	R_i (KΩ)
1,32	108.8	9,24	76.8
2,31	67.2	10,23	35.7
3,30	51.9	11,22	22.7
4,29	46.4	12,21	16.7
5,28	47.5	13,20	13.4
6,27	57.6	14,19	11.6
7,26	97.2	15,18	10.5
8,25	(∞)	16,17	10.1

Fig. 6. Digital-to-analog converter, which functions as a digital low pass filter. ***M:*** SN7406 hex buffer/driver. ***N:*** SN7407 hex inverter buffer/driver. ***P:*** ¼ × CD4016A quad analog FET bilateral switches (RCA). ***Q:*** Analog Devices AD504J low drift IC operational amplifier. The effective weights W_i (see text) are shown graphically. The tabulated resistance values include the on-resistance of the FET switches.

Fig. 6 shows the digital-to-analog converter which transforms the PRBS into band-limited white Gaussian noise. The 32-stage shift register serves as a digital delay line for the PRBS. Digital filtering (nonrecursive) of the PRBS is achieved simply by forming a weighted sum of the values in the shift register stages [10]–[12]. In order to approximate an ideal (rectangular) low-pass filter it is appropriate to use a truncated sinc (x) shaped function [12]. The underlying reason for this choice is that the impulse response of an ideal (rectangular) low-pass filter of bandwidth f_L is sinc $(2f_Lt)$. The relative weights W_i and resistance values R_i are given by

$$R_i = R_0/W_i$$

$$W_i = \text{sinc}\,[(i - 16.5)/8.5].$$

The resistance scale is set by the choice $R_0 = 10$ kΩ.

The implementation of this weighting is as follows. Depending on the polarity of W_i the output S_i is passed through an inverting or noninverting buffer. The buffer outputs control FET switches which selectively tie the appropriate R_i to 5 V and leave the rest open. In Fig. 6 the values W_i are shown graphically and the nominal R_i are tabulated. The latter may be scaled arbitrarily. Note that R_i must include the on-resistance of the FET switches (typically 450 Ω).

The above choice for W_i corresponds nominally to a rectangular low-pass filter with cutoff frequency $f_L = 1/17\Delta t$. The actual filter is inexact in two respects. The discreteness of the digital filtering produces minor peaks at harmonics of the clock frequency $1/\Delta t$. These are strongly suppressed, because the power spectrum of the underlying PRBS, with a shape of $\text{sinc}^2\,(f\Delta t)$, vanishes at those harmonics. In the time domain, the discreteness shows up in the slight stepwise nature of the analog output. The other imperfection of the filter is the truncation of the sinc $(2f_L t)$ waveform at $t = \pm 15.5\,\Delta t$, because of the finite length of the digital-filter (i.e., the 32-stage shift register). As such the filter has a finite (but still very steep) rolloff above a 3-dB cutoff frequency of about $1/20\Delta t$, slightly below the nominal f_L.

Statistics of Analog Noise Patterns

For stage i of the shift register, let S_i be the logical state (0 or 1) and let I_i be the current through R_i, directed toward the summing junction of operational amplifier ***Q***. Further, define $I_0 = V_0/R_0$ where V_0 is the reference voltage for the FET switches and R_0 is the scale factor defined above. Then

$$I_i/I_0 = \begin{cases} S_i W_i, & W_i \geq 0 \;(8 \leq i \leq 25) \\ (1 - S_i)(-W_i), & W_i < 0 \;(1 < i < 7;\; 26 < i < 32) \end{cases}$$

or

$$I_i/I_0 = S_i W_i + (|W_i| - W_i)/2.$$

Let I be the total current into the summing junction, $I = \Sigma_i S_i W_i + I_D$ where

$$I_D = I_0 \sum_i (|W_i| - W_i)/2 = \sum_{W_i<0} |W_i|.$$

Assuming that the binary sequence is random, then one can show

$$\langle S_i \rangle = \tfrac{1}{2}$$

and

$$\langle S_i S_j \rangle = (1 + \delta_{ij})/4$$

where the angle brackets denote expectation values and δ_{ij} is the Kronecker delta function.

Using these relations it is straightforward to derive that

$$\langle I \rangle = I_0(\Sigma|W_i|)/2$$

and

$$\sigma_I = I_0(\Sigma W_i^2)^{1/2}/2.$$

For the design values given above assuming $V_0 = 5$ V, one finds: $I_0 = 0.5$ mA, $I_D = 1.14$ mA, $\langle I \rangle = 3.07$ mA, and $\sigma_I = 0.710$ mA.

The offset potentiometer (Fig. 6) can supply a current to cancel $\langle I \rangle$, if noise with zero-mean level is desired. More generally it can supply to the pattern an arbitrary dc offset of either polarity. The gain potentiometer (of resistance R) can be used to scale the analog noise output V. The standard deviation of V is given by

$$\sigma_V = \sigma_I \cdot R = 0.710 \times R(\text{k}\Omega).$$

For example if $R = 1.4$ kΩ then $\sigma_V = 1$ V. The above derivation depends on the assumption that the binary sequence is random. For PRBS's, especially *short* ones $(n < 12)$, there will be departures from the values above.

The (approximate) Gaussianness of the amplitude distribution arises not by specific design but rather as a consequence of the central limit theorem of probability theory [13], applied to the sum $\Sigma_{i=1}^{32} S_i W_i$. For short sequences $(n < 12)$ the distribution departs significantly from being Gaussian, and depends on the choice of PRBS. Thus in those applications requiring Gaussian noise, longer sequences are preferred.

Construction

The circuitry described above was constructed on seven boards. The 32 stages of the shift register and related circuitry (Figs. 2, 3, 4, 5) were divided on four almost identical printed circuit boards. Three additional boards were used for the control logic, for the analog-to-digital converter, and for the weighting resistors $\{R_i\}$. The control board included a fixed 1-kHz clock, for testing. In our application an external clock was used.

Front panel controls included digital switches for the *octal code* (seven digits) as well as switches for instrument *power, clock source* (external/internal/manual), *clock enable* (run/stop), *reset,* and *mode selection* for the bank of twenty lamps (code/shift register). In addition there were turns-counting dials for the *gain* and *offset* potentiometers. Four BNC connectors were provided for *external clock* input and for *binary sequence, analog noise* and *sync* outputs.

The design above is open to a number of variations depending on the application of such an instrument. Both the length of the shift register (here 32 stages) and the limit of the feedback length (here 20) may be changed. Furthermore, different weighting functions $\{W_i\}$ may be used to obtain analog noise with other properties [10], simply by substituting a board with different weighting resistors R_i. As mentioned above, a

number of features, including the lamps and the *sync* generator, are optional. For most applications the subtle stepwise nature of the "analog" output will not be a problem. In rare cases (such as those involving differentiation) where smooth waveforms are required, a (second-order) low-pass analog filter may be added. Note however that the filter must be modified if Δt is changed.

Operation

The operation of the instrument is straightforward. One selects an octal code, presses reset (if desired) and enables the clock as long as desired. The noise pattern repeats periodically. It should be noted that if the instrument is reset (by clearing the shift register), the first $32 - n$ values of the *analog* noise pattern are slightly in error, compared to all subsequent repetitions. This portion of the analog pattern may be bypassed either electronically or during subsequent computer analysis, depending on the application.

A computer program was written which simulates the operation of the instrument. Given any octal code, the program computes the binary sequence and analog noise pattern. A message is printed if the binary sequence is not of maximal length (i.e., not a PRBS). This program has been useful for checking the instrument and for studying the statistical properties of the noise patterns. Copies of the program, written in Fortran, may be obtained on request from the first author.

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Response Time Measurements Using Walsh Functions

STAMATIOS V. KARTALOPOULOS, MEMBER, IEEE

***Abstract*—The sal- and cal-functions of the well-known Walsh functions are used to construct a simple and minimal Walsh-function generator. Codes at random sequence or a sequence of codes at random time are generated. A generated code automatically enables a particular stimulus (which may be visual or audible) or any appropriate objective external stimulus (depending upon the response time and the reflex action) to be measured. The response time is measured with an accuracy as high as microseconds if TTL family extended to nanoseconds if ECL family is employed. The time accuracy is determined by the particular application and upon the particular response. This particular measuring system is designed for measurements of response time of the man–machine interaction but measurements can be extended with minor modifications to response time of interest to medical, biological, physiological, and psychological fields.**

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The author is with the Department of Electrical Engineering, College of Engineering, University of Toledo, Toledo, OH 43606.

Introduction

SINCE THE RESPONSE time which elapses between an objective stimulus to one of the senses and the reflex action, is what the circuit is designed to measure, let us review what is meant by reflex actions.

In general, the reflex actions are divided into two major groups, the *unconditional reflexes* which occur with no specific learning or experience and which are involuntary acts because a response always occurs when a particular stimulus is presented, and the *conditional reflexes* which work by association and a previous learning or experience is required. For both groups, the response time will be referred to, in the simplest form, as the time it takes for all four mechanisms, reception, conduction, transmission, and response, to be activated.