enhancement in the thermal stability.[15] Without any barrier, the Al/Pd_2Si reaction starts around 300 °C. With an amorphous carbon layer of 1000 Å, no reaction is detected after an anneal of 30 min at 500 °C in N_2-H_2. It is thus interesting to extend the carbon barrier to other Al/silicide structures.

Several concerns regarding the use of carbon include its sensitivity to oxygen at high temperatures, and stress generated in the films. We have found that, using a structure of carbon on Cu, annealing in N_2-O_2 mixtures above 400 °C caused removal of the carbon layer due to the oxidation reaction. On the other hand, using a N_2-H_2 ambient, the carbon layer remains stable at 750 °C for at least an hour.[16] For the device processing, once the Al/C/PtSi metallurgy is buried by subsequent oxide and other insulating layers, the oxidation problem of the carbon layer during subsequent processings involving oxygen plasma can be minimized. As for the stress generated in the structures containing a carbon layer, no film peeling was observed in two separate runs using preformed PtSi processed at different times, with the corresponding Al and carbon depositions also done at different times. Using a different structure, Al/C/Pt/Si, with the Pt, C, and Al layers deposited on Si, film peeling was observed in one of the two separate runs. In such a run where film peeling was observed, the films were found to shrink and peel during the cooling stage after heating to 300–500 °C. In this regard, film peeling was not observed for the C/Cu/SiO_2/Si structure up to 750 °C, but was found for the Au/C/Cu/SiO_2/Si structures at 600 °C. Further studies are needed to understand the origin of such film peeling, and the compatibility of carbon to different materials at elevated temperatures.

In summary, an amorphous carbon layer has been shown to be an effective barrier between PtSi and Al up to 600 °C. This result, coupled with a similar enhancement of the thermal stability of the Al/Pd_2Si structure using the carbon barrier, makes carbon attractive as a barrier for the contact metallurgies containing such silicides.

The author would like to thank G. Coleman for the backscattering measurement, and R. Petkie for the film deposition.

[1] H. H. Hossack, J. Appl. Phys. **44**, 3476 (1973).

[2] H. Grinlods and G. Y. Robinson, J. Vac. Sci. Technol. **14**, 75 (1977).

[3] G. J. van Gurp and W. M. Reukers, J. Appl. Phys. **50**, 6923 (1979).

[4] C. Y. Ting and M. Wittmer, J. Appl. Phys. **54**, 937 (1983).

[5] C. Y. Ting and M. Wittmer, Thin Solid Films **96**, 327 (1982)

[6] M.-A. Nicolet, Thin Solid Films **52**, 415 (1978).

[7] M.-A. Nicolet and M. Bartur, J. Vac. Sci. Technol. **19**, 786 (1981).

[8] M. Eizenberg, R. D. Thompson, and K. N. Tu, J. Appl. Phys. **53**, 6891 (1982)

[9] M. Wittmer, J. Vac. Sci. Technol. A **2**, 273 (1984).

[10] G. Salomonsen, A. Olsen, O. Lonsjo, and T. G. Finstad, J. Appl. Phys. **60**, 1753 (1986).

[11] Chin-An Chang, J. Appl. Phys. **63**, 236 (1988).

[12] Chin-An Chang, in *Tungsten and Other Refractory Metals for VLSI Applications III*, edited by V. A. Wells (Material Research Society, Pittsburgh, PA, 1988), p. 265.

[13] G. Ottaviani, J. Vac. Sci. Technol **16**, 1112 (1979), and references therein; C.-A. Chang, J. Appl Phys. **61**, 1864 (1987).

[14] C.-A. Chang, J. Appl. Phys. **66**, 2363 (1989).

[15] C.-A. Chang, Appl. Phys. Lett **54**, 1656 (1989).

[16] C.-A. Chang, D. S. Yee, and R. Petkie, Appl. Phys. Lett. **54**, 2545 (1989); C.-A. Chang, J. Appl. Phys. **66**, 1163 (1989).

Observation of large peak-to-valley current ratios and large peak current densities in AlSb/InAs/AlSb double-barrier tunnel structures

J. R. Söderström,[a] D. H. Chow, and T. C. McGill
T. J. Watson, Sr., Laboratory of Applied Physics, California Institute of Technology, Pasadena, California 91125

(Received 1 May 1989; accepted for publication 1 August 1989)

We report improved peak-to-valley current ratios and peak current densities in InAs/AlSb double-barrier, negative differential resistance tunnel structures. Our peak-to-valley current ratios are 2.9 at room temperature and 10 at liquid-nitrogen temperatures. Furthermore, we have observed peak current densities of 1.7×10^5 A/cm^2. These figures of merit are substantially better than previously reported values. The improvements are obtained by adding spacer layers near the barriers, thinner well regions, and thinner barriers.

Double-barrier tunnel devices have been a subject of great interest for several years.[1–3] These device structures offer the possibility of making new devices, exploring interesting device physics, and the possibility of making high-speed and high-density devices. To date most of the effort has been concentrated on heterostructures based on GaAs/GaAlAs.[1–3] This heterojunction system suffers from three major problems. First, difficulty in making ohmic contacts to *n*-type GaAs causes a substantial series resistance in the

---

[a] Previous address: Chalmers University of Technology, S-41296 Göteborg, Sweden.

circuit, limiting the performance of the device. Second, small barriers for electrons in this heterojunction system lead to substantial contributions to the room-temperature current from thermally excited carriers. This current substantially reduces the peak-to-valley (P/V) current ratio observed in GaAs/AlGaAs double-barrier structures. Finally, it is difficult to obtain the high current densities that are necessary to obtain high powers from these device structures. There has been some work on InGaAs/AlAs heterostructures which addresses these problems with good results.[4,5] However, the lattice mismatch in these structures makes them difficult to fabricate.

To fix these difficulties, we have proposed the use of double barrier structures consisting of InAs/ZnTe/InAs/ZnTe/InAs.[6] This nearly lattice-matched heterojunction system has a number of advantages. First, it is very easy to make *n*-type, low-resistance ohmic contacts to the InAs. Second, the InAs has a high electron mobility and, consequently, can carry large currents through the requisite cladding layers. Finally, the conduction-band offset between InAs and ZnTe is estimated to be about 1.6 eV. This is in contrast to the conduction-band offset of roughly 1 eV for Γ point to Γ point GaAs/AlAs and roughly 0.2 eV for the Γ point to X point barrier in GaAs/AlAs. We projected that this structure would have substantially higher peak-to-valley current ratios at room temperature and would not suffer from some of the difficulties associated with transport through the ohmic contacts and cladding layers.

A III-V alternative in these attempts to improve performance is the near lattice-matched InAs/AlSb structure.[7] This structure has the same advantages as the ZnTe/InAs structure with low series resistance and high mobility. The Γ-point conduction-band offset is 1.8 eV; the X point is 1.2 eV. Experimentally, negative differential resistance has been observed in this structure by Lou, Beresford, and Wang.[7] They reported P/V ratios of 1.8 at room temperature and 9 at 77 K for a 168-Å InAs quantum well sandwiched between 25-Å AlSb barriers. They further point out that the small effective mass of InAs makes it possible to have thicker InAs layers and still provide substantial separation between subbands. This additional width of the quantum well should facilitate three-terminal device fabrication.[8-10]

In this communication we report results of a study of these new III-V double-barrier structures. In particular, by applying spacer techniques[11] and working with thinner barriers we have substantially improved the performance of the devices. The reason for having undoped spacer layers is the reduction of Si donors that diffuse into the barrier region during growth.[11] This reduces the impurity scattering resulting in a lower valley current. The potential drop in the undoped spacer layers also causes the peak to move to higher voltages compared to a sample with no spacer layers. We have increased the peak-to-valley current ratio to 2.9 at room temperature and to 10 at liquid-nitrogen temperature. Furthermore, we have made substantial increases in the peak currents by working with thinner barriers. The observed peak current densities are as high as 1.7×10^5 A/cm^2.

The structures were grown in a Perkin-Elmer 430 MBE system which included arsenic and antimony cracker sources. The growths were carried out using the techniques described in Ref. 12 which have been demonstrated to produce high-quality InAs and Sb-based layers. The substrates were GaAs which is subtantially lattice mismatched to InAs and AlSb. Growth commenced with a 0.5-μm-thick GaAs buffer layer at 600 °C. This buffer layer was followed by a superlattice consisting of $In_{0.7}Ga_{0.3}As$/GaAs grown at 500–520 °C. The superlattice reduces the number of strain-induced dislocations in the epilayer. The InAs/AlSb structures were grown at 500 °C. The device structure is shown in Fig. 1. A standard lift-off process followed by chemical etching was used to fabricate mesa structures ($5\ \mu m \times 5\ \mu m$ in

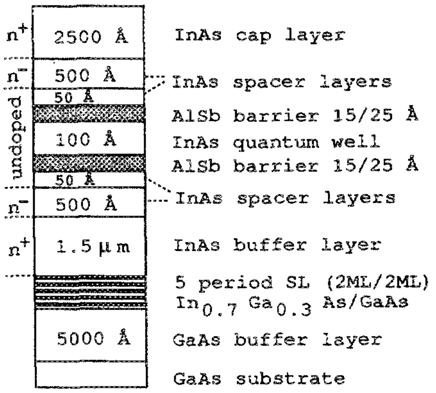

FIG. 1. Schematic diagram of a typical structure used in this study. The doping levels for the layers labeled n^- and n^+ are 2×10^{16} cm^{-3} and 2×10^{18} cm^{-3}, respectively.

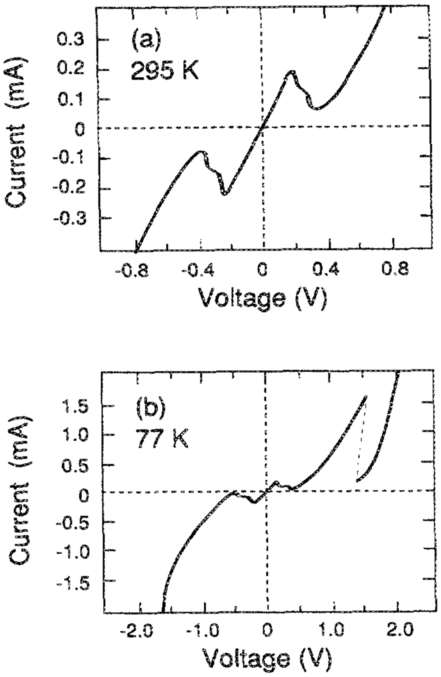

FIG. 2. The current-voltage characteristic of an InAs/AlSb/InAs/AlSb/InAs structure. The upper (lower) curve was taken at room temperature (77 K). The AlSb barriers were 25 Å thick and the InAs well was 100 Å thick.

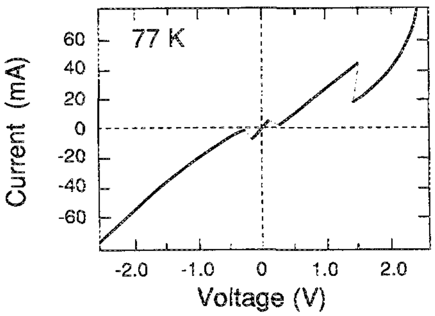

FIG. 3. The current-voltage characteristic at 77 K of InAs/AlSb/InAs/AlSb/InAs structure. The AlSb barriers were 15 Å thick and the InAs well was 100 Å thick.

size) with AuGe contacts on top. The back contact was produced by AuGe deposited on the etched InAs buffer layer.

Current-voltage (*I-V*) characteristics for these tunnel devices are shown in Figs. 2 and 3. The *I-V* characteristics shown in Fig. 2 are for a structure with 25-Å-thick AlSb barriers and an InAs well thickness of 100 Å. As can be seen from these *I-V* characteristics, a single peak is observed at room temperature with a peak-to-valley current (P/V) ratio of 2.9. At liquid-nitrogen temperature, two peaks are observed in forward bias and one in reverse. For the first peak, we observed a P/V ratio of 6 and for the second peak a P/V ratio of 10.

The *I-V* characteristic at 77 K from a second sample with 15-Å AlSb barriers and InAs well layer thickness of 100 Å is shown in Fig. 3. Again, this structure shows one peak at room temperature and two peaks at liquid-nitrogen temperature. For the second peak at liquid-nitrogen temperature, we observe a peak current density of 1.7×10^5 A/cm^2 and a P/V ratio of 2.3. This compares favorably to the previous results for InAs/AlSb structures where peak current densities less than 400 A/cm^2 were obtained.[7] Our result is also close to what has been obtained for the extensively studied GaAs/AlAs system for which peak current densities $\approx 2\times10^5$ have been reported.[13] These very large peak current densities are in the range of interest for making high speed tunnel devices.[4]

In summary, we have reported the results of a study of a new heterojunction system for double-barrier tunnel structures. By the application of some of the simple techniques of improving negative resistance, that is the addition spacer layers and the use of thinner barriers, we have substantially improved the performance over those previously reported. In particular, we have increased the peak-to-valley current ratio by roughly a factor of 2 at room temperature and have observed substantial improvements in the peak current densities. In different structures, we have been able to demonstrate very large current densities and peak-to-valley current ratios which if they could be produced in the same structure would bring them near the region of interest as defined in Ref. 4. These performance goals seem well within the range that one might hope to attain in these structures. We believe that these new device structures based on the AlSb/InAs heterojunction will be very interesting for further applications in tunneling devices.

The authors gratefully acknowledge the support of the Air Force Office of Scientific Research under Grant No. 86-0306. One of us (J.R.S.) gratefully acknowledges the support of the Sweden-America Foundation. Another (D.H.C.) gratefully acknowledges the support provided by a TRW-PAT Fellowship.

[1] R. Tsu and L. Easki, Appl. Phys. Lett. **22**, 562 (1977).
[2] T. C. L. G. Sollner, W. D. Goodhue, P. E. Tannewald, C. Parker, and D. D. Peck, Appl. Phys. Lett. **43**, 588 (1983).
[3] A. R. Bonnefoi, R. T. Collins, T. C. McGill, and R. Burnham, Appl. Phys. Lett. **46**, 285 (1985).
[4] S. Hiyamizu, T. Fujii, S. Muto, T. Inata, Y. Nakata, Y. Sugiyama, and S. Sasa, J. Cryst. Growth **81**, 349 (1987).
[5] T. Inata, S. Muto, Y. Nakata, S.Sasa, T. Fuji, and S. Hiyamzu, Jpn. J. Appl. Phys. **26**, L1332 (1987).
[6] E. T. Yu and T.C. McGill, Appl. Phys. Lett. **53**, 60 (1988).
[7] L. F. Luo, R. Beresford, and W. I. Wang, Appl. Phys. Lett. **53**, 2320 (1988).
[8] A. R. Bonnefoi, T. C. McGill, and R. D. Burnham, IEEE Electron Device Lett. **EDL-6**, 636 (1985).
[9] A. R. Bonnefoi, D. H. Chow, and T. C. McGill, Appl. Phys. Lett. **47**, 888 (1985).
[10] J. N. Schulman and M. Waldner, J. Appl. Phys. **63**, 2859 (1988).
[11] C. I. Hwang, M. J. Paulus, C. A. Bozada, S. C. Dudley, K. R. Evans, C. E. Statz, R. L. Jones, and M. E. Cheney, Appl. Phys. Lett. **51**, 121 (1987).
[12] J. R. Söderström, D. H. Chow, and T. C. McGill, Proceedings of the Spring MRS Meeting, San Diego, California April, 1989 (*to be published*).
[13] S. K. Diamond, E. Ozbay, M. J. Rodwell, D. M. Bloom, Y. C. Pao, E. Wolak, and J. S. Harris, IEEE Electron Device Lett. **EDL-10**, 104 (1989).