Push clocks: a new approach to charge-coupled devices clocking*

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A new approach to charge-coupled device clocking has been developed—dynamic push clocks. With dynamic push clocks, the charge is transferred by pushing it from one storage site to another. The push clock approach results in a larger signal dynamic range, larger signal-to-noise ratio, and better performance at both high and low frequencies.

The operation of charge-coupled devices (CCD's) as introduced by Boyle and Smith,[1] depends on the storage and transport of charge packets representing information in potential wells at the semiconductor-insulator interface under closely spaced electrodes. The charge packets are minority carriers injected in response to a digital or analog signal or generated by photons. The closely spaced electrodes (gates) are driven by clocking pulses that may have various shapes and waveforms to control the storage and transfer of the charge packets along the interface. In general, clocking pulse waveforms could be classified into two basically different types: drop clocks and push clocks. With drop clocks the signal charge is stored below a gate at a holding voltage V_1 which is a fraction of the largest clock voltage V_m that the MOS structure can tolerate; charge transfer occurs when V_m is then applied to the adjacent gates and the charge flows to the potential minimum thus created. With push clocks the charge is stored under a gate held at V_m, and is transferred to a nearby gate, also at V_m, by raising the potential of the gate where the charge has been residing and thus "pushing" the charge to the next gate. CCD's can be operated with two-phase, three-phase, or four-phase clocking schemes by push clocks, drop clocks, or a combination of push and drop clock.[2-4] In this letter we describe the use of push clocks to control the storage and transfer of charge in CCD's and discuss their advantages over the commonly used drop clocks.[1,5,6]

A detailed explanation of push clock operation and comparison with drop clocks can be made with the aid of Figs. 1 and 2. These figures depict charge storage and transfer in two-phase and four-phase CCD's, with both drop and push clocks; in all cases, the complete charge transfer mode[7] is used. We have used the overlapping gate structure, as it is the most technically promising CCD structure for the potential large-scale applications of these devices.[4,6,8,9] The particular clock voltages shown apply to the case of p-channel devices, in which all clock voltages are negative. V_m is the minimum (most negative) clock voltage that can be used, as determined by some constraint such as field oxide threshold; V_1 is the holding voltage (in the drop clock case) and V_2 is a resting (gate off) voltage, thus $V_2 > V_1 > V_m$.

The drop clock case is shown first; the signal charge is stored under a gate at potential V_1 [Figs. 1(a) and 2(a)]. To effect charge transfer, the voltage of the adjacent gate (transfer gate) and the next storage gate, are lowered to V_m [Figs. 1(b) and 2(b)]; the charge flows to the local potential minimum which is under the last-mentioned gate. In the push clock case, the signal charge is initially held under a storage gate which is at V_m [Figs. 1(a′) and 2(a′)]. At the beginning of the charge-transfer operation, the voltages of the adjacent transfer gate and the next storage gate are lowered to V_m. The potential of the original storage gate is then *gradually* raised, and the charge stored there begins to "spill" over the area beneath the transfer gate and into the area under the next storage gate [Figs. 1(b′) and 2(b′)]. As the potential of the original storage gate continues to rise, more of the charge under it is brought to a potential higher than that under the transfer gate, and so the charge is able to flow to the next storage gate. Finally the original storage gate reaches it resting potential, V_2.

It can be seen from the preceding discussion that the push clocks allow a greater fraction of V_m to be used in storing the signal charge, and thus provide a greater dynamic range and signal-to-noise ratio than drop clocks. Also, as will be shown below, the push clock scheme yields better charge-transfer efficiency at both high and low frequencies. Finally, the push clock alone allows a definite advantage in high-speed operation to be obtained from the use of a four-phase clock. In Figs. 1 and 2, it is clear that the charge transfers for the two-phase drop clock and four-phase drop clock are similar; therefore, increasing the clock complexity from two-phase to four-phase with drop clocks does not improve the performance of the device. However, the dynamic push clock takes full advantage of the more flexible control of the surface potential under the different electrodes. For example in Fig. 2(a′) during storage times the transfer gates can be turned off by the resting voltage V_2 and the storage gates can be heavily turned on by the minimum voltage V_m. The maximum signal charge which may be stored under the storage gate is thus almost a full bucket.[10] Also, since the transfer gates are controlled independently, they can be turned on heavily during the first stages of the transfer process, as shown in Fig. 2(b′), to enhance the rate of charge transfer. Thus, increasing the clocking-scheme complexity with push clocks allows better control of the storage and transfer of the signal charge and hence provides larger signal dynamic range, larger signal-to-noise ratio, and better performance, especially at high frequency.

The limitations on the performance of CCD's are mainly due to incomplete free-charge transfer at high frequencies and trapping in the interface state at moderate and low frequencies.[1-4,9,11-15] In order to quantitatively compare the performance of CCD's with push and drop clocks, we have used a detailed numerical simulation of charge transfer in the two cases. The transport dynamics were analyzed in terms of thermal diffusion, self-induced fields, and fringing fields under all the relevant electrodes and the interelectrode regions with

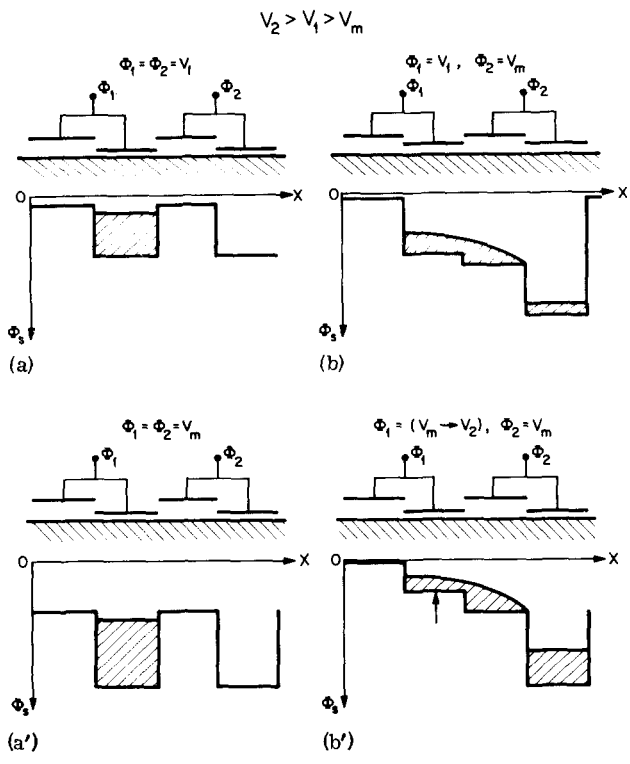

FIG. 1. Storage and transfer of charge in two-phase overlapping-gate CCD's. Surface potentials ϕ_s with and without charges are plotted along the interface. (a) and (b) are for two-phase drop clocks; (a′) and (b′) are for two-phase push clocks.

time-varying gate potentials. The self-induced fields were evaluated using the gradual channel approximation, and a constant surface mobility of 200 $cm^2/V\,sec$ was assumed.[2–4] A realistic model[15] of interface-state traping was included; a constant interface-state density of $2\times10^{10}/cm^2\,eV$ was assumed, with a capture cross section of 10^{-15} cm^2. The refilling of interface states during charge transfer was taken into account.

The above-mentioned model was applied to a two-phase overlapping-gate CCD with electrode dimensions consistent with typical silicon-gate MOS technology; the storage gates are poly-silicon electrodes overlapped with aluminum transfer gates. The "fat-zero" (background-charge) scheme was used, as it considerably improves the performance of the device.[4,13–15] We have chosen a suitable background charge q_0 to represent a "fat zero" and a larger charge q_s to represent the signal, as would be used, for example, to represent the zero and one bit in a digital serial memory. The limitations on the device performance due to incomplete charge transfer are best described by the signal degradation factor ϵ defined by Berglund.[9,16] If Δq_f is the difference in the residual charge due to the signal and the residual charge due to the fat zero resulting from the incomplete charge transfer, and Δq_t is the difference resulting from trapping in interface states, then

$$\epsilon = (\Delta q_f + \Delta q_t)/(q_s - q_0).$$

Δq_t in general depends on the information content of the signal. In Fig. 3 we have plotted the calculated signal degradation per transfer vs bit time and bit rate for the device just described. The solid-line and dashed-line curves are the signal degradation factor when two-phase push and drop clocks are used, respectively. These results are based on a sequence of alternating signal and fat-zero charges. Although the exact values obtained for the signal degradation ϵ are dependent on the particular geometries and other model parameters chosen, the general features of the performance of drop clocks relative to push clocks are not; in general, the transfer efficiency is higher for the push clock at both low and high clock frequencies. The improvement in transfer efficiency is due mainly to an important property of push clocks: The differences in the charge-transfer characteristics and the mobile-charge profiles under the CCD gates, depending on whether a large or small charge is being transferred, are minimized with push clocks. With a push clock the transfer of charge does not start until the surface potential under the initial storage gate is larger than that under the next transfer gate. This condition occurs earlier or later in the transfer cycle, depending on whether more or less charge was originally stored. Thus, provided the zero signal or zero bit is represented by a background charge, the charge profiles under the gates during the remainder of the transfer cycle are almost independent of when the actual movement of charge began; that is, they are independent of the initial charge to be transferred. Hence, the residual charges after each transfer with push clocks are almost independent of the initial charges. Therefore the signal degradation due to in-

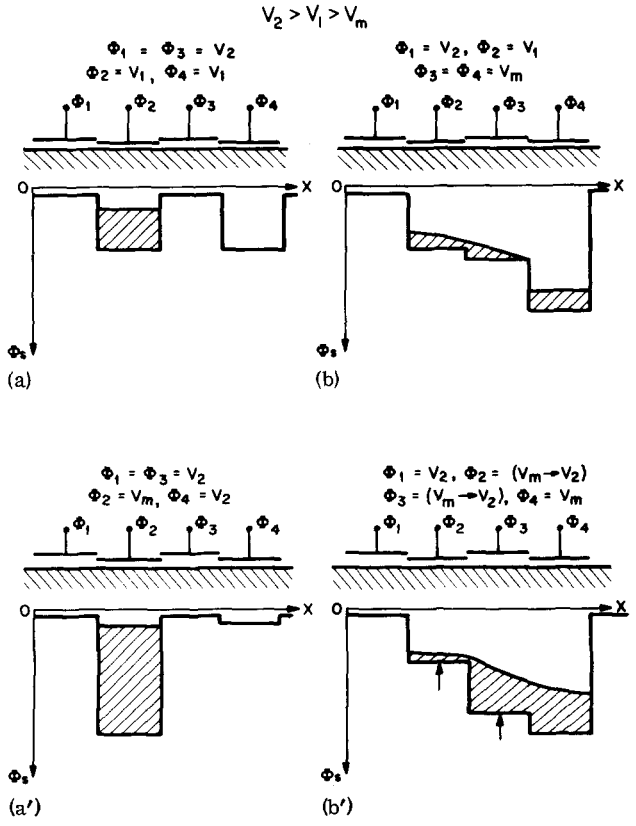

FIG. 2. Storage and transfer of charge in four-phase overlapping-gate CCD's. Surface potentials ϕ_s with and without charge are plotted along the interface. (a) and (b) are for four-phase drop clocks; (a′) and (b′) are for four-phase push clocks.

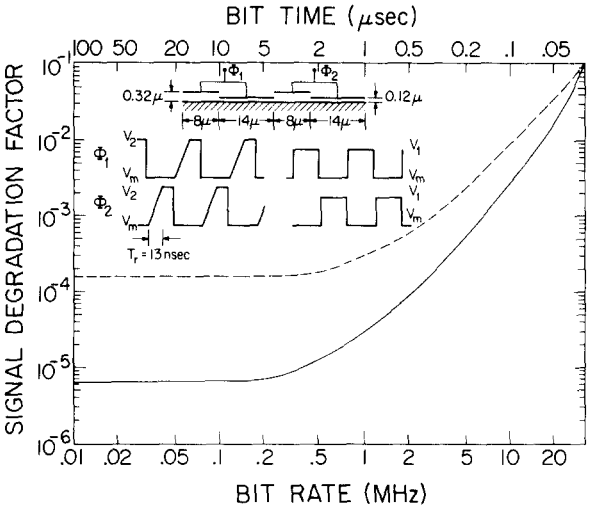

FIG. 3. Signal degradation factor vs bit time and bit rate for a two-phase minimum-geometry p-channel overlapping-gate CCD. The solid-line and dashed-line curves are for the push clock and the drop clock, respectively. The storage gates are poly-silicon electrodes 14 μ long and 8 μ apart. The transfer gates are aluminum electrodes. The channel width is 8 μ. The oxide thickness under the storage and transfer gates is 1200 and 3200 Å, respectively. The substrate doping is 8×10^{14} donors/cm^3. In the calculations, zero fall and rise times, $V_m = -15$ V, and $V_1 = -7$ V were used for the drop clock; zero fall time, 13 nsec rise time, $V_m = -15$ V, and $V_2 = -6$ V were used for the push clocks. Surface mobility was 200 cm^2/sec V. A constant interface-state density of 2×10^{10}/cm^2 eV and a constant capture cross section of 10^{-15} cm^2 were assumed. The signal degradation due to interface-state trapping was calculated by assuming an alternating sequence of signal and fat-zero charges.

complete free-charge transfer at high frequency is less when the device is operated with push clocks than when the device is operated with drop clocks.[17]

At moderate and low frequencies, charge trapping in the interface states limits the performance of CCD devices.[10,12–15] In the overlapping-gate structure, the interface states under the storage gates, transfer gates, and edges of the gates perpendicular to the active channel capture charge from both the signal and the background charge. Hence the background charge is effective in reducing the effect of trapping in these interface states on the incomplete charge transfer. Also, for a sufficiently large background charge the effective equilibration time constant of these interface state (~1 nsec) is much smaller than the rise and fall times obtained with practical clock drivers (~tens of nanoseconds). Therefore, these interface states can effectively equilibrate with both the signal and background charges. Hence, the incomplete charge transfer due to trapping in these interface states varies directly with frequency and becomes very small at sufficiently low frequency.[15] Thus, the most dominant effect in the overlapping-gate CCD is trapping in the interface states under the parallel edges (areas parallel to the active channel at the interface under the storage and transfer gates covered by the signal charge and not covered by the background charge).[15] With push clocks, the effective parallel edge area is smaller than with drop clocks, as both the signal and fat-zero charges cover almost the same area under the gates during the pushing of the charges. Also with push clocks, the charges under the storage and transfer gates and the time at which the emptying of the interface states begins tend to be less dependent on the initial charge. This is because with push clocks the residual charges are much less dependent on the initial charges and a larger portion of the clocking voltage is used to store the signal charge. For example, when the device is operated with a two-phase push clock, the signal degradation due to interface-state trapping at low frequency is reduced by more than an order of magnitude than when it is operated with two-phase drop clock.

The waveforms of the different phases of the dynamic push clocks must be overlapping. Since the rate of charge transport along the interface is finite, the rise times T_r of the clocking pulse have minimum permissible values. If these values are exceeded, the surface potential under the gates exceeds $2\phi_F$ and some of the signal charge will be injected into the substrate where it is lost by recombination. For example, the minimum rise time of the two-phase push clock is given by[4]

$$T_{r_{\min}} \approx 2(l_{st}l_{tr}/\mu)(C_{st}/C_{tr})(1/V_c),$$

where l_{tr} and l_{st} are the lengths of the aluminum transfer gate and poly-silicon storage gate, μ is the surface mobility, C_{st} and C_{tr} are the effective oxide and depletion layer capacity under the storage and transfer gate, respectively, and V_c is equivalent to the clocking voltage amplitude. For minimum-geometry electrodes (~10 μ) and reasonable clock voltage amplitudes (~5 V), $T_{r_{\min}}$ is much smaller than the finite rise and fall times which are unavoidable in practical clock drivers (~tens of nanoseconds). Hence, the finite rise and fall times that would delay the charge transfer with drop clocks are advantageously used with push clocks to push the charge from one storage site to another.

In conclusion, the key features of dynamic push clocks are that a larger portion of the clocking voltage is used to store the signal charge; hence, larger signal charges can be transferred, which results in larger signal dynamic range and signal-to-noise ratio. Also, with push clocks the characteristics of the charge transfer are more independent of the value of the signal charge than with drop clocks. Hence, the residual charges after each transfer are much less dependent on the initial charges, and the interaction of the different charges with the interface states is more similar. This results in better performance at both high and low frequencies. The pushing of the charge from one storage site to another is easily achieved by the finite fall and rise times which are unavoidable in practical clock drivers.

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[17]Note that the two-phase drop clock used in Fig. 3 has zero rise and fall times. Any finite rise and fall times of the pulses of the drop clock will delay the charge transfer; hence, the shown results actually overestimate the performance of the device with drop clocks at high frequency, but with push clocks, the finite rise times are advantageously used to push the charge from one site to another.