

CACTUS: A depleted monolithic active timing sensor using a CMOS radiation hard technology

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ABSTRACT: The planned luminosity increase at the Large Hadron Collider in the coming years has triggered interest in the use of the particles' time of arrival as additional information in specialized detectors to mitigate the impact of pile-up. The required time resolution is of the order of tens of picoseconds, with a spatial granularity of the order of 1 mm. A time measurement at this precision level will also be of interest beyond the LHC and beyond high energy particle physics. We present in this paper the first developments towards a radiation hard Depleted Monolithic Active Pixel Sensor (DMAPS), with high-resolution time measurement capability. The technology chosen is a standard high voltage CMOS process, in conjunction with a high resistivity detector material, which has already proven to efficiently detect particles in tracking applications after several hundred of Mrad of irradiation.

KEYWORDS: Timing detectors, Particle tracking detectors

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Contents

1	Introduction	1
2	Architecture of the sensor	2
2.1	Theoretical timing resolution limits	2
2.2	Pixel Design	2
2.3	Chip Design	4
3	In-lab characterisation	5
3.1	I-V measurements	5
3.2	Signal to noise characterisation	6
3.3	Timing measurements with ^{90}Sr source	7
4	Test beam	8
4.1	Test beam infrastructure	8
4.2	Test beam results	10
4.2.1	Detection efficiency	10
4.2.2	Response uniformity	11
4.2.3	Timing performance	12
5	Conclusions and perspectives	13

1 Introduction

Time measurements with a resolution of 100 ps or better are rapidly gaining interest in detector development for high energy physics. Such a time resolution on individual Minimum Ionizing Particles (MIP) gives the potential to associate individual particles to their production vertex in high pile-up environments like the high luminosity upgrade of the Large Hadron Collider (HL-LHC) with up to 200 average interactions per bunch crossing.

Several timing detector projects within the ATLAS and CMS experiments are being developed right now, with the aim of resolutions of the order of 30 ps per MIP. Prominent examples include the High Granularity Timing Detector (HGTD) in ATLAS [1] and the MIP Timing Detector (MTD) in CMS [2, 3], which both use LGAD (low-gain avalanche diode) technology.

We present in this paper the design, simulation and test results of an integrated timing detector based on a Depleted Monolithic Active Pixel Sensor (DMAPS), using an industrial 150 nm CMOS process from LFoundry with High Resistivity (HR) wafers. The choice of a CMOS process is based on the three main benefits expected from standard DMAPS technology: low cost, radiation hardness, and good time resolution.

High Voltage (HV) CMOS processes are relatively low cost since they are the process of choice for high volume consumer electronics used in the automotive industry. In addition, a monolithic architecture eliminates the need for costly bump bonding operation [4]. Altogether, the DMAPS opens the possibility for relatively cheap sensors, which is crucial for future large projects such as the FCC. HV–HR CMOS technologies such as the LFoundry 150 nm LF15A have proven to accept a high bias voltage of the order of 300 V applied on the sensor backside, over a thickness of 200 μm , fully depleting several hundred micrometers of silicon material. They have been tested under irradiation for tracking applications, and a suitable signal to noise ratio has been measured for doses up to 150 Mrad [5, 6]. Recently, dedicated monolithic sensors developed in a SiGe BiCMOS process for a Time-Of-Flight PET application have proven a timing resolution of the order of 50 ps [7]. This demonstrates the high potential of CMOS processes for timing applications.

2 Architecture of the sensor

2.1 Theoretical timing resolution limits

Reference [8] gives analytical expressions for the time resolution of silicon detectors without intrinsic signal multiplication. The charge deposit of high energy particles is described with the Landau theory. The three components contributing to the time resolution, namely the charge deposit fluctuations, noise and fluctuations of the signal shape are all estimated analytically. The effect of leading edge discrimination is also taken into account. The main conclusions are :

- For MIP detection, the thinner the sensor, the better the time resolution. Assuming the sensor is biased at 200 V, the time resolution should be 180 ps and 60 ps for a sensor thickness of 200 μm and 100 μm respectively.
- To not degrade the time resolution using leading edge discrimination, the peaking time should be rather large (of the order of 1 ns), and the threshold set at low values, typically below 40 % of the total signal charge.

The main parameters of the sensor discussed in this work are close to these settings in terms of depletion depth, electric field and front end architecture.

2.2 Pixel Design

The pixel design of the CACTUS (Cmos ACTIVE pixel Timing μ Sensor) chip presented in this paper is largely based on previous pixel designs, with many modifications to improve the timing performance. The pixel designs we started from are two tracking demonstrator chips, LF-CPIX [9, 10] and LF-MONOPIX [11], originally intended for the 5th layer of the ITK, the upgrade of the ATLAS internal tracker for the HL-LHC. The design technology used for these demonstrators is the same as for the CACTUS, and uses the LFoundry 150 nm LF15A process, with high resistivity substrate ($\geq 2 \text{ k}\Omega \cdot \text{cm}$).

Compared to LF-CPIX and LF-MONOPIX, we have chosen to implement large surface collecting diodes of $1 \times 1 \text{ mm}^2$ and $1 \times 0.5 \text{ mm}^2$. There are several reasons to use such large collecting diodes for a timing detector:

- A pitch of about 1 mm is the order of magnitude of what is intended for detector projects like the HGTD and is representative of the required pitch for future timing oriented detectors.
- To speed up the output signal and reduce as much as possible its rise time, it is needed to increase significantly the bias currents of the front-end electronics. Small pixel pitches would lead to an unacceptable power dissipation per surface unit. In our case, for an estimated bias current of $800 \mu\text{A}$ per pixel, the static power consumption of the active area is $145 \text{ mW}/\text{cm}^2$.
- To ensure the best possible timing resolution, the electric field lines within the collection diode have to be as parallel as possible. A large collection diode allows reducing the fraction of the surface where fringe effects are significant, and large pads help to minimise the influence of shared hits.

The cross-section of a pixel of CACTUS is shown in figure 1 (not to scale). Due to the deep n-well (DNW) and buried p-well (DPW) layers available in this process, it is possible to implement complementary (NMOS and PMOS) transistors inside the pixel. The in-pixel electronics occupy only a small part of the area of the pixel. On the other hand, the power rails are quite large to minimize the resistivity of the supplies.

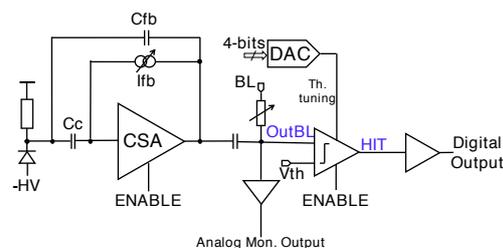
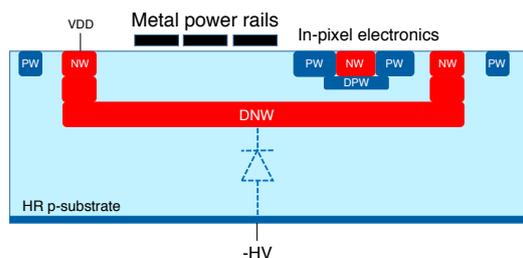


Figure 1: Cross-section of a pixel showing the in-pixel electronics and the metal power rails (drawing is not to scale). **Figure 2:** Block diagram of the CACTUS pixel analog front-end.

The in-pixel front-end electronics of each pixel is made of a fast charge-sensitive amplifier (CSA) followed by a leading-edge discriminator (see figure 2). Each pixel has a 4-bit DAC to correct any threshold non-uniformity from the discriminators. The analog output of the CSA (OutBL) and the digital output of the discriminator (HIT) can be monitored out of the chip through dedicated on-chip buffers. The charge collection diode is continuously biased through a very high impedance device (a diode-connected NMOS transistor [9]). There is no leakage compensation circuit.

To ensure good timing resolution with such a configuration, the time walk effects have to be measured and corrected. If the signal shape has sufficient uniformity over the sensitive surface, a unique time-walk correction can be used independent of the impact point of the particle.

The implementation of two pixel sizes allows to study the front-end performance for two detector capacitance values. The pixel capacitance values have been estimated from the Sentaurus TCAD simulation software [12] and the Cadence Integrated Circuit (IC) design tools by simulating the contribution of the diode and the in-pixel electronics. The capacitance values are around 1.5 pF

and 1 pF for pixel sizes of 1 mm^2 and 0.5 mm^2 respectively. Other critical parameters concerning the detection diode have also been checked using Sentaurus software: the breakdown voltage, the total charge collected, and the charge collection as a function of time. Typically, for a $100 \mu\text{m}$ thin sensor, according to these simulations almost all of the charge generated from a MIP is collected within 5 ns, with a rise time of the order of 1 ns [13].

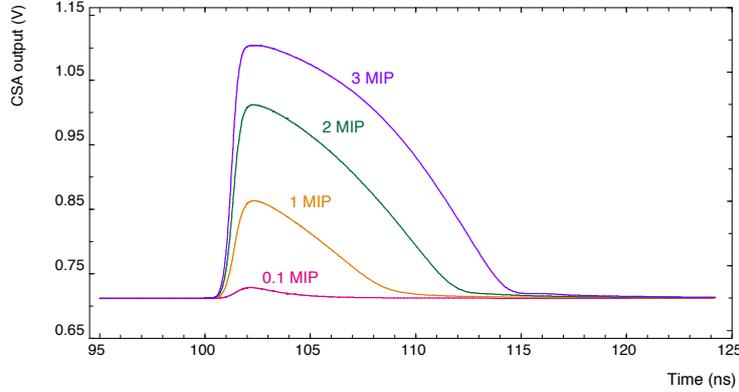


Figure 3: Cadence transient simulation result of the analog front-end for a $100 \mu\text{m}$ thinned sensor. The input charge varies from 1 ke^- (0.1 MIP) to 24 ke^- (3 MIP). The front end rise time is about 1 ns ($V_{\text{DD}} = 1.8 \text{ V}$, $I_{\text{bias}} = 800 \mu\text{A}$).

The front-end performance has been studied using Cadence simulations tools. Transient simulation results with an injected charge varying between 1 ke^- and 24 ke^- (corresponding to about 0.1 MIP to 3 MIP for a $100 \mu\text{m}$ thinned sensor) are shown in figure 3 for a detection capacitance of 1.5 pF ($V_{\text{DD}} = 1.8 \text{ V}$, total bias current = $800 \mu\text{A}$). According to these simulations, the rise time is about 1 ns and the input-referred noise 300 e^- .

2.3 Chip Design

The global layout of the chip is shown in figure 4. The total chip surface is about 100 mm^2 . In addition to the detection pixels with their front-end electronics, the chip features a slow control system allowing to enable or disable any individual pixels and to set the bias currents of global DACs. The control data are loaded using a SPI-like bus implementation and stored on-chip in a shift register of 281 bits. The chip includes a column-encoding logic, giving the coordinate of the hit pixel on dedicated output channels.

For each column, the pixels share a common readout line which sends the discriminator signals to a fast output (LVDS and/or CMOS). There is also a global digital output signal (HITOR) and an analog monitoring output that can be connected to any of the pixels (only 1 chosen pixel at a time). The analog monitoring buffer, which is a cascade of 2 distributed source followers, has a limited bandwidth compare to the in-pixel CSA. Its gain is around 0.6.

Two versions of the chip have been designed and submitted to fabrication. The main difference between them is the external guard-rings used to apply the HV on the substrate. While the version A uses the guard-rings from LF-CPIX (V2) with a proven breakdown voltage (BV) of about 220 V [10], the version B uses an improved guard-ring strategy. The expected BV voltage for the version B is greater than 350 V. The width of the guard-rings for both versions is $250 \mu\text{m}$.

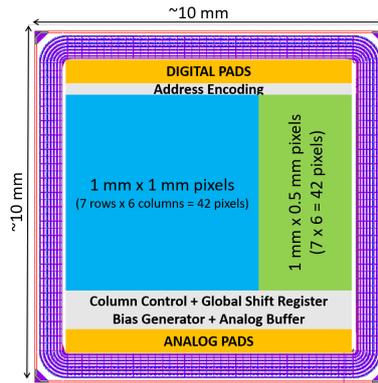


Figure 4: Simplified block diagram of CACTUS. The external guard ring width is $250\ \mu\text{m}$ for CACTUS versions A and B.

3 In-lab characterisation

After the fabrication of CACTUS sensors, one wafer has been diced without post-processing. The thickness of a standard wafer is $725\ \mu\text{m}$. The increase of depletion depth increases the total collected charge but increases also the charge collection time and the fluctuations on the charge deposition. An optimum should be found for this critical parameter. Two additional wafers have been thinned to $200\ \mu\text{m}$ and $100\ \mu\text{m}$ and then post-processed with boron implant and metallization, to allow back-side polarization of the sensor. Some $100\ \mu\text{m}$ chips sensors have been tested in lab, and $200\ \mu\text{m}$ sensors have been characterized in-lab and in test-beam.

For laboratory tests of the sensor, a dedicated test-bench has been developed. A proximity board (called the "CACTUS board") holds the CACTUS sensor and some drivers. This board is connected to a General-purpose Programmable Analog Card (GPAC) which provides the low voltage power supplies, references, and buffering of fast CACTUS signals. A Raspberry-Pi connected to the GPAC via a small adapter board is used to generate the slow control signals and also to read out the addresses of the hit pixels. A WaveCatcher, an 8 channel 12 bit fast digitizer [14] based on a switched capacitor array, is used for fast sampling of analog and digital outputs.

3.1 I-V measurements

The BVs of the charge collection diodes have been evaluated by increasing the substrate bias voltage of the chip while measuring the supply current. Figure 5 shows the BVs measured on four different non-thinned and thinned CACTUS chips. The BV measured on version A is $230\ \text{V}$. The BV measured on version B is around $350\ \text{V}$. The value for version A was also confirmed on other thinned and non-thinned sensors. According to previous tests with similar structures and the same substrate resistivities on the same process, these voltages are enough to fully deplete thinned substrates ($-15\ \text{V}$ needed for $100\ \mu\text{m}$ and $-60\ \text{V}$ for $200\ \mu\text{m}$ [15]). The ability to bias the sensor with higher voltages is beneficial to compensate for the charge losses after neutron irradiation [16].

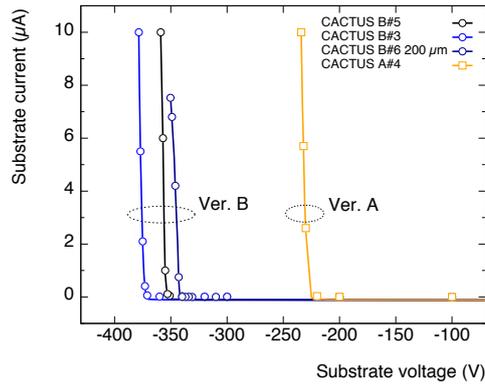


Figure 5: Break-down voltages measured on different CACTUS chips (versions A and B).

3.2 Signal to noise characterisation

The temporal noise and threshold (off-set) dispersions have been evaluated for each pixel from S-curves obtained by scanning the external threshold voltage (V_{th} in figure 2). Figure 6 shows the distributions of these parameters obtained from a non thinned sensor (version B) with $V_{DD} = 1.8$ V, $V_{BL} = 700$ mV, a total bias current of $800 \mu\text{A}$, and an $HV = 0$ V. From figure 6.a, the mean RMS noise is 3.56 mV for small and 5.20 mV for large pixels (this should correspond to $230 e^-$ and $300 e^-$ input-referred noise respectively according to initial simulations). The threshold dispersions are high before tuning (large distributions in figure 6.b), but after tuning to an arbitrary value of 740 mV, due to in-pixel DACs, they become lower than the temporal noise values: 1.46 mV_{RMS} for small pixels and 1.68 mV_{RMS} for large pixels (corresponding to $94 e^-$ and $96 e^-$ respectively according to simulations). The mean values are 747 mV before tuning and 740 mV after tuning (corresponding to $\approx 3100 e^-$ and $\approx 2600 e^-$ respectively according to simulations). The results are the same when $HV = -300$ V. Similar tests done on thinned sensors show that thinning and post-processing do not change the electrical characteristics of the front-end. This is also valid for the high voltage sensor bias.

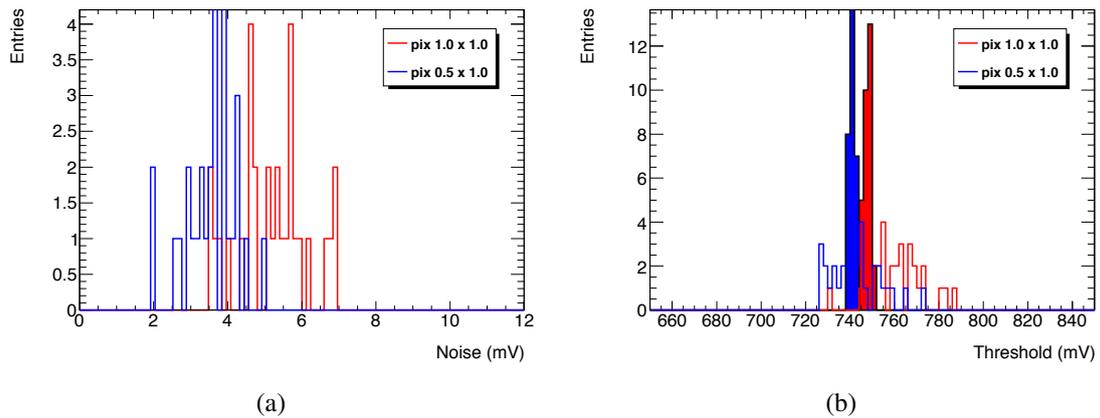


Figure 6: a) Temporal noise and b) threshold distributions of all pixels of a CACTUS ver. B before (wide distribution) and after tuning (narrow distribution).

The signal to noise measurements have been done using a radioactive ^{133}Ba source, whose main emission line is at 31 keV (corresponds to $\approx 8.5 \text{ ke}^-$ in silicon). The ASIC (application-specific integrated circuit) tested is a non-thinned version B sensor, biased at $\text{HV} = -300 \text{ V}$.

Figure 7 shows the spectrum obtained for one $1 \times 0.5 \text{ mm}^2$ pixel at the analog monitoring output. The signal amplitude measured is almost six times lower than expected from simulations (measured MPV around 14 mV instead of 96 mV). The source of the reduced gain was found to be an underestimated extraction of the in-pixel power rail capacitances with the extraction software tools (capacitances between metal layers and the large HR p-type area inside the DNW of the pixel, shown in figure 1). New estimations of the actual capacitance lead us to the conclusion that the input diode capacitance is more than an order of magnitude larger than expected (more than 15 pF, see simulation results in table 1). The open loop gain of the charge sensitive amplifier is not large enough to compensate for the very high input capacitance value and the overall gain of the pixel is highly degraded. If the input diode capacitance is around 15 pF then the input referred temporal noise levels should be of the order of 2 ke^- instead of 230 e^- .

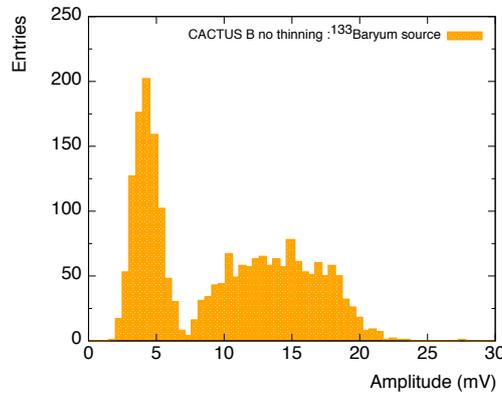


Figure 7: Spectrum from a ^{133}Ba source obtained at the analog monitoring output of a $1 \times 0.5 \text{ mm}^2$ pixel. The noise and the signal are clearly separated. The MPV of the signal is measured around 14 mV, six times lower than simulated.

Table 1: Simulated analog monitoring output amplitude as a function of CSA input capacitance (8.5 ke^- input charge).

C_{det} (pF)	Signal amplitude (mV)
1.0	96.4
1.5	88.8
15.0	17.8
20.0	13.4

3.3 Timing measurements with ^{90}Sr source

For timing measurements, a collimated ^{90}Sr source is placed on top of the Device Under Test (DUT) at a distance of 8 cm. A photomultiplier (PMT) (Hamamatsu 11934) coupled to a plastic

scintillator and placed below the DUT provides the reference time measurement. Both CACTUS digital outputs and PMT signals are sent to a WaveCatcher digitizer [14].

The data coming both from the Raspberry-Pi (the address of the hit cell and the trigger) and from the WaveCatcher (CACTUS signals) are collected on a computer. The arrival time difference of the PMT and CACTUS signal is used to estimate the CACTUS timing resolution. Independently the PMT resolution has been measured around 80 ps using two PMTs and a ^{22}Na source.

The CACTUS used in these measurements is a 200 μm thick sensor biased at $\text{HV} = -300\text{ V}$. At the price of a high trigger threshold (80 mV corresponding to ≈ 2.9 MIPs), using an ad hoc TOT correction (figure 8.a) we obtained a CACTUS time resolution of 105 ps (figure 8.b). The TOT correction accounts for the PMT timewalk, the CACTUS timewalk and the correlations between time of flight and energy deposit. The result shown in figure 8.b includes the contribution of the PMT time resolution. On figure 8.a, the highest amplitude energy deposits correspond to the slowest β particles, and hence to the highest time difference between the PMT and the sensor, and also to the highest PMT TOT. At lower thresholds, the timing resolution degrades: 278 ps at 1.7 MIPs and 303 ps at 1.0 MIPs.

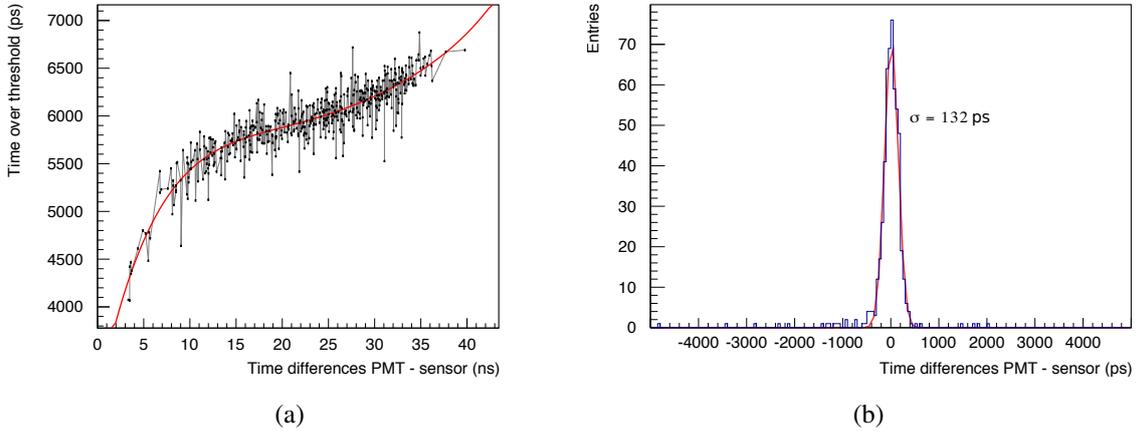


Figure 8: Time differences between sensor and PMT a) versus TOT and polynomial parameterization. b) After TOT correlation corrections. The 132 ps dispersion corresponds to the quadratic sum of the PMT 80 ps resolution and the CACTUS 105 ps resolution (threshold ≈ 2.9 MIPs).

4 Test beam

A test beam campaign has confirmed the signal to noise ratio estimated from X-ray sources and allowed us to study the uniformity and charge collection of the sensor. It also gave an estimation of the time resolution for MIPs.

4.1 Test beam infrastructure

Test beam measurements were performed at the Fermilab Test Beam Facility (FTBF) [17], which provides a unique opportunity to characterize prototype detectors for collider experiments. A typical application is to place a DUT in the high energy beam, and measure its response to the

beam particles passing through its active area. FTBF provides a 120 GeV proton beam from the Fermilab Main Injector accelerator. The FTBF beam is resonantly extracted in a slow spill for each Main Injector cycle delivering a single 4.2 sec long spill per minute, tuned to yield approximately 60 000 protons per single spill. The primary beam (bunched at 53 MHz) consists of 120 GeV protons. All measurements presented in this paper were taken with the primary beam particles.

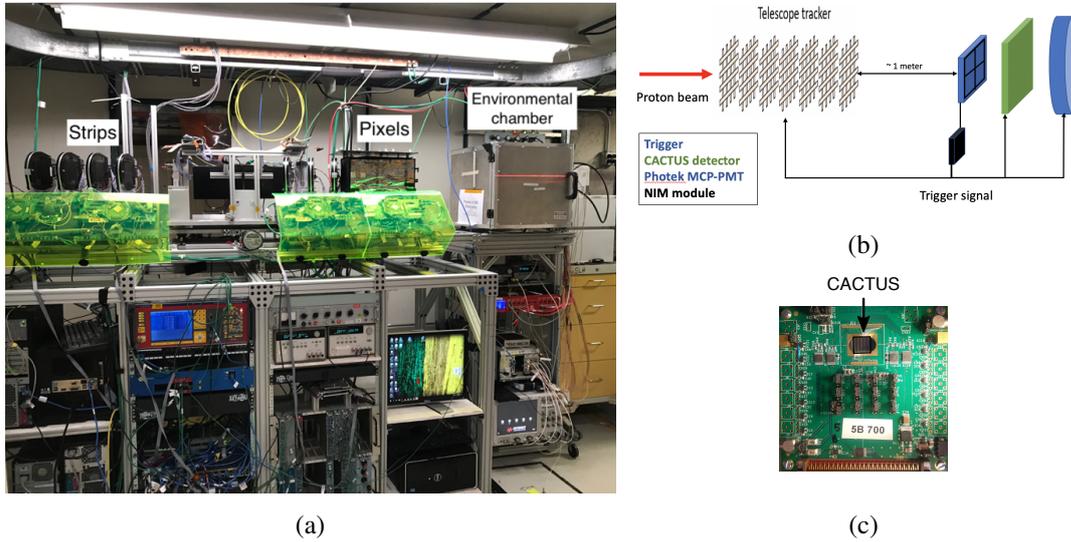


Figure 9: a) A photo of the CACTUS characterization experimental station and the telescope tracker at FTBF, b) a schematic diagram of the test beam setup at FTBF, and c) a photo of the CACTUS board.

The prototype CACTUS sensor was mounted on a remotely operated motorized stage, placed inside an environmental chamber with controlled temperature and humidity, shown in figure 9.a. A schematic diagram of the experimental setup are shown in figure 9.b, which presents the arrangement of CACTUS sensor with respect to the telescope and triggers. The DUT board used in test beam measurements to characterize the CACTUS sensor is shown in figure 9.c. The relative alignment was mechanically constrained to be around one mm, and we estimate the slant angle to be less than 5 degrees. The FTBF is equipped with two silicon telescopes aligned along the beam line and configured to operate synchronously. It has a pixel telescope assembled from eight planes and a telescope with strip modules made up of fourteen detector planes. Each microstrip plane consists of 639 microstrips, each $60\ \mu\text{m}$ wide, placed orthogonal to each other, and the pixel telescope's cell sizes are $100 \times 150\ \mu\text{m}^2$. The strip telescope increases the coverage of the pixel telescope and improves its tracking performance. The Data Acquisition (DAQ) hardware is based on the CAPTAN (Compact And Programmable daTa Acquisition Node) system developed at Fermilab. The CAPTAN is a flexible and versatile data acquisition system designed to meet the readout and control demands of a variety of pixel and strip detectors for high energy physics applications.

A Photek 240 micro-channel plate (MCP-PMT) detector was placed furthest downstream behind the CACTUS sensor, inside the environmental chamber, and provided a very precise reference timestamp. Its precision has been previously measured to be less than 10 ps [18]. The trigger to the telescope, the CACTUS sensor, and to the DAQ system was provided by a scintillator coupled

to a PMT. The DAQ system is based on a Keysight MSOX92004A oscilloscope, which provides digitized waveforms sampled at 40 GS/s. At the control room PC, the data from each CAPTAN node are saved in a binary file for each Run. Data from the CACTUS, the silicon telescope, and Photek were merged offline by matching the trigger counters of each system.

4.2 Test beam results

4.2.1 Detection efficiency

Several adjacent pixels of $1 \times 0.5 \text{ mm}^2$ in the middle of a CACTUS version B sensor thinned to $200 \mu\text{m}$ and backside polarized to $\text{HV} = -300 \text{ V}$ were tested during the testbeam.

The analog signal amplitude, defined as the height of the signal pulse in mV is shown in figure 10.a for events where the telescope track crosses the pixel area. Only one pixel was read out at a time. A $50 \mu\text{m}$ margin on the pixel's border was excluded to avoid possible bias due to the telescope tracking resolution. This distribution is fitted to the sum of the signal and noise distributions, with their relative normalization floated. The signal amplitude distribution is modeled by a convolution of a Landau distribution and a Gaussian. A template for the noise amplitude distribution has been obtained from data using events where the telescope track points outside the pixel area. The blue histogram shows the total data, while the red distribution shows the signal contribution after statistical subtraction of the fitted noise distribution. The fit is shown in green, with the most probable value (MPV) measured at about 16.2 mV and a smearing (signal shape distorted by the noise) of about 3.7 mV. The efficiency as a function of the threshold is deduced from the cumulative distribution of the signal and shown in figure 10.b. The slight 3% inefficiency that can be seen for a threshold of about 10 mV is due to multiple scattering after the telescope tracker, shifting the corresponding tracks out of the pixel surface. The ratio between signal and background is estimated to be 5.5 for a threshold of 10 mV.

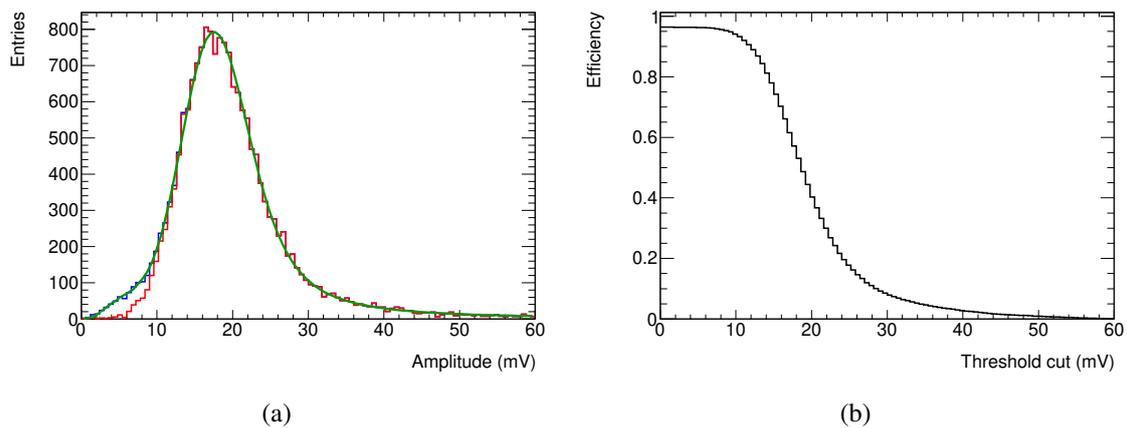


Figure 10: a) Analog signal amplitudes measured on a pixel close to the center of the sensor. The data distribution is shown in blue while the noise-subtracted signal contribution is shown in red. The distribution is fitted to the sum of a Landau distribution convoluted with a Gaussian and a noise contribution. b) Efficiency as a function of the amplitude threshold in mV.

4.2.2 Response uniformity

The analog signal uniformity has been evaluated by fitting the edges of the hit map of the pixels to an *erfc* function. A hit is defined as a signal in the pixel with a maximum amplitude higher than 20 mV, in time coincidence with the test beam tracker. From the fits, the position of the active edges have been extracted for the three pixels measured in the data. The position of the active edge is defined as the position where the *erfc* function reaches half of its asymptotic value.

Figure 11 shows a projection of the hit maps along the x axis, superimposing hit maps obtained from two adjacent pixels. Only one pixel was read at a time. It can clearly be seen that there is a small hit rate reduction at the boundary between two adjacent pixels. From the active edge position obtained from the fits, we observed a small inactive lane of 20 μm width in the x direction, where the pixel pitch is 1000 μm , and of 10 μm in the y direction, where the pixel pitch is 500 μm . As a cross-check, the pixel sizes in x and y have also been measured and values that are consistent with 1000 μm and 500 μm were found.

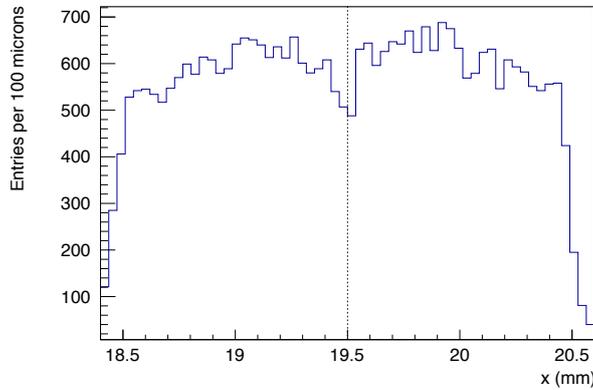


Figure 11: Hit map projection on the x axis, for two adjacent pixels. The vertical line indicates the boundary between two adjacent pixels.

The signal shape uniformity has also been checked as a function of the particle impact point position on the pixel. The pixel surfaces in strips of 100 μm wide, in both directions, have been binned and the average of all the pulse shapes corresponding to particles impacting the pixel in each of these strips have been computed. A small 10 % variation of the amplitude as a function of the track impact point position within the pixel was observed. However, normalized pulse shapes computed with the same procedure, but normalizing each pulse to its amplitude, did not show any difference. This indicates that the shape itself is not correlated to the track impact point position.

In addition to the same procedure, using five different bins in amplitude chosen to have the same number of events for all bins, it has been checked whether the pulses had the same shape for all amplitudes. No difference has been found. This implies that the amplitude differences can be corrected within one pixel by implementing a simple TOT correction.

Finally, the uniformity has also been checked by reproducing the fit on the amplitude distributions described in section 4.2.1 for several slices of X or Y of the tested pixel (excluding the 50 μm margin in the other dimension). Figure 12 shows the MPV of the Landau and the efficiency as a function of X or Y .

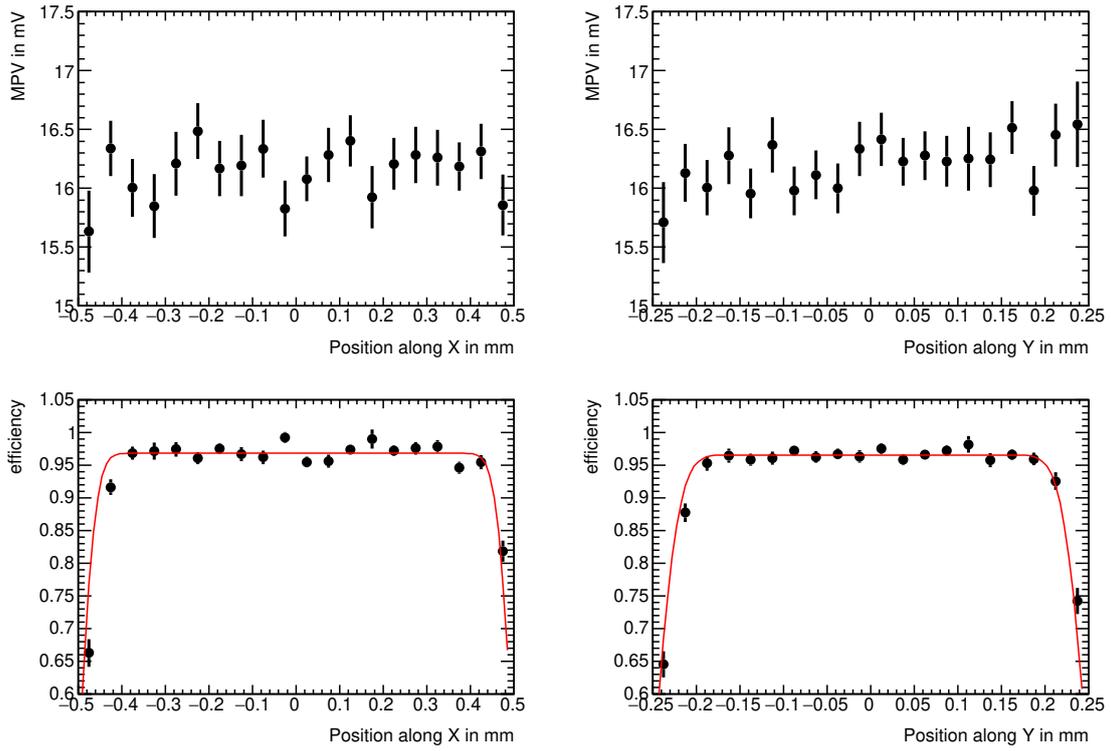


Figure 12: MPV and efficiencies determined in slices of X or Y. For the efficiencies, the red curves show the expected efficiency when a 97 % plateau efficiency is convoluted with a 25 μm telescope resolution.

4.2.3 Timing performance

Test beam data have been used to evaluate the timing resolution of the sensor with MIPs. Due to the lower than expected signal to noise ratio, it was expected that the time resolution would be worse than 180 ps for that thickness and that it would be needed to cut strongly on the amplitude to obtain reasonable signals. Furthermore, the analog monitoring output is much slower than the analog front-end signal and was not intended to be used for timing studies (see section 2). Only one pixel was read out, which explains the efficiency drop visible at the edge of the pixel.

The signal measured from the sensor is compared to the signal from the Photek 240 MCP-PMT to obtain time measurements. For the analog readout, a quadratic time walk correction is obtained by measuring the time difference as a function of the amplitude. No time walk correction has been applied for the digital readout due to low statistics. The arrival time differences between the sensor and the PMT are shown for the analog output and the digital output in figure 13.

To minimize the distortion of the signal shape by the noise, which significantly degrades the time resolution at small signal amplitudes, we require the signal amplitude to be larger than 30 mV for analog data, corresponding to a threshold of ≈ 1.9 MIPs. A lower threshold was used for the test beam digital runs (≈ 0.3 MIPs).

The timing results from the MIPs are consistent with the results obtained with the ^{90}Sr source (figure 13).

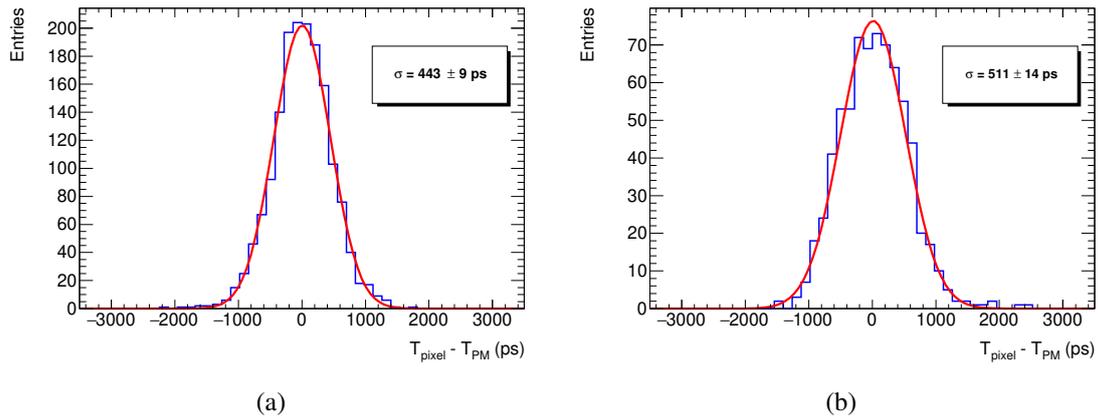


Figure 13: Time differences between sensor and PMT in ps with a) analog monitoring output (threshold ≈ 1.9 MIPs) and b) digital output (threshold ≈ 0.3 MIPs).

5 Conclusions and perspectives

A monolithic timing sensor prototype in a radiation hard CMOS 150 nm process has been designed and tested. The test results are promising but some problems have been observed with this first CACTUS prototype. During the tests with radioactive sources, the observed analog signal to noise ratio has been found to be lower than expected from simulations and previous tracking prototypes as explained in section 3.2. This observation has been confirmed with MIPs at test-beam. This effect is likely due to the in-pixel power metal rails, which increase significantly the capacitance of the charge collection diode. This problem will be overcome in future designs by modifying the pixel layout, mainly putting the front-end electronics outside of the charge collecting diode.

Other parameters of the chip have been shown to be very promising. The measured breakdown voltages are high enough to deplete more than 200 μm . Thinning and backside processing of fabricated wafers have been done reliably and successfully. The charge collection uniformity inside the pixel has been checked with MIPs, and no significant dead areas have been observed.

A lower than expected signal to noise ratio presently limits the detection efficiency and the timing resolution of the detector. Nevertheless, the excellent global performance of the chip and our understanding of the observed imperfections call for a new design iteration of the CACTUS concept, and is already well under way.

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