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Subtractive photonics

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Abstract: Realization of a multilayer photonic process, as well as co-integration of a large number of photonic and electronic components on a single substrate, presents many advantages over conventional solutions and opens a pathway for various novel architectures and applications. Despite the many potential advantages, realization of a complex multilayer photonic process compatible with low-cost CMOS platforms remains challenging. In this paper, a photonic platform is investigated that uses subtractively manufactured structures to fabricate such systems. These structures are created solely using simple post-processing methods, with no modification to the foundry process. This method uses the well-controlled metal layers of advanced integrated electronics as sacrificial layers to define dielectric shapes as optical components. Metal patterns are removed using an etching process, leaving behind a complex multilayer photonic system, while keeping the electronics' metal wiring intact. This approach can be applied to any integrated chip with well-defined metallization, including those produced in pure electronics processes, pure photonics processes, heterogeneously integrated processes, monolithic electronic-photonic processes, etc. This paper provides a proof-of-concept example of monolithic electronic-photonic integration in a 65 nm bulk CMOS process and demonstrates proof-of-concept photonic structures. The fabrication results, characterization, and measurement data are presented.

1. Introduction

While optics played a major role in the advent of the information age by enabling the global telecommunication network, the ubiquitous and faster advancing field of integrated electronics established silicon-based platforms as a low-cost mainstream fabrication process providing the bulk of processing power, and more recently, storage [1]. Consequently, research in silicon photonics has been pursued with the goal of leveraging the immense infrastructure of silicon electronics (particularly CMOS) for the manufacturing of integrated photonic systems [2–5]. Central to this goal is the promise of monolithic integration with complex high-performance electronic systems, which could offer far-reaching benefits beyond what each platform can offer individually [5–7]. Compact structures, enabled by the high index contrast between silicon and silicon dioxide, are often cited as an additional advantage of such platforms [4,6]. However, the need for full containment of a higher index waveguide core by a lower index cladding puts silicon photonics at odds with bulk CMOS, a problem which is often addressed through some form of silicon-on-insulator (SOI) guided mode [8,9].

Two options for integrating electronics with photonics immediately present themselves, and both have been pursued with reasonable success. The first option of hybrid integration is to simply package a bulk CMOS chip with a photonic chip, which can be accomplished using wire bonding, flip-chip mounting, or through-silicon vias [10]. This method has been employed to build optical transceivers [11], electronically controlled optical phased arrays (OPA) [12], and LiDAR systems [13]. Although hybrid integration can offer highly optimized platforms for the electronics and photonics separately, the parasitics associated with packaging those systems and the parameter variability can diminish the overall benefit. Refinement of an existing monolithic platform potentially offers a simpler and more economical path forward.

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The second option is to move forward with an SOI electronic process [14], including the so-called "zero-change"platform [15–17]. This platform makes use of partially depleted SOI processes with the highest f_t and f_{max}, which allows these photonic systems to compensate for any attendant disadvantages by making use of complex electronic systems [17]. Overall, the primary drawback of this platform is that the backside of the wafer must be etched under photonic components to avoid high losses associated with leakage into the substrate. However, the advent of more specialized silicon photonics processes [14] has not only shown that this difficulty is surmountable through the inclusion of backside etching in a foundry process, but also that the use of RF-specific SOI processes for photonics has been entirely superseded.

Another option is that of modifying a bulk CMOS process to include SOI components. A method has been proposed involving the deposition of a high-quality poly-silicon layer on top of a thick oxide layer, which is in turn deposited between the electronic active regions [18]. Doping of the active photonic devices can then use the same process steps as the doping for transistors, minimizing the number of lithography masks. An entire suite of photonic components, including modulators, detectors, grating couplers, and a wavelength division multiplexing (WDM) chiplet demonstrated the feasibility of system-scale integration [18]. However, the necessity of modifying the process still presents a major roadblock to mainstream adoption, and the waveguide loss is substantially higher than competing platforms (The reported loss of the rib waveguides is 8-15 dB/ cm, although it could possibly be improved [18].).

Adding to the demand for the integration of electronics and photonics is the need for multilayer photonic platforms, a need which is rising as integrated photonic systems scale and novel designs with thousands of on-chip components emerge [19–21]. Most of today's low-cost integrated photonic platforms provide a single photonic layer, with multiple etch depths to provide extra thickness options. This planar photonic structure presents optical routing difficulties for the implementation of certain complex systems as the number of components scales [12]. Although SOI-based platforms have been modified to achieve multilayer photonics by embedding extra routing layers [22–24], this approach is not fully compatible with electronic integration and significantly increases the fabrication cost for every added layer.

In this paper, we explore a subtractive photonics platform in which the interconnect metal layers of standard bulk CMOS chips are etched to leave behind complex 3D dielectric (e.g., SiO_2 or SiN) structures. These dielectric structures may be suspended in air or additional materials with a higher refractive index may be deposited through spin coating as a guiding core. This platform offers a number of advantages, but utmost among them is that it is compatible with many integration platforms since the *only* requirement on the manufacturing process is that it must be able to produce well-defined patterned metal and dielectric layers. This includes many platforms such as almost all modern electronic processes and silicon photonics processes, opening up a large range of possible fabrication options. The broad transparency window of silicon dioxide (commonly used for the dielectric layers) is also attractive for operation in the visible range. Furthermore, the many layers available for on-chip interconnect naturally enable multilayer photonic structures, opening up the design space significantly. The presented structures need only one post-processing step of etching. The standard fabrication process for CMOS is not modified and the same platform which is used to make electronic chips is utilized. There is no extra lithography and only one etching step is added after the chip is fabricated in a standard platform. This etching step is a sequence of applying multiple etchants to remove both metals and etch stop layers. The etching patterns and mask are created by designing the proper patterns using the existing metal stack. As a result, while the photonic chip will have a different mask design, the fabrication process remains the same. For the case that a secondary material is added, a second step of spin coating this material after the etching step is used. This is the key feature of this approach, which enables a low-cost solution on unmodified (bulk) CMOS platforms. Although suspended waveguides have been proposed and demonstrated [25–28], to our knowledge this is

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the first proposal of 3D multilayer photonics in conjunction with electronic chips produced in an unmodified CMOS process. The post-processing etching of metal structures on silicon chips has been used in the past in other applications, such as MEMS systems [29,30] and biomedical sensors [31]).

2. Subtractive photonics on integrated electronic platforms

A bulk silicon platform [32–35] utilizes purified crystalline silicon wafers as a substrate on which various components are integrated. Fabrication steps of such platforms are divided into the two general categories of front-end-of-line (FEOL) and back-end-of-line (BEOL) stages [36] (Fig. 1). FEOL includes realization of all the electronic devices on the silicon substrate excluding the metal wiring and interconnects. In contrast, BEOL consists of a set of steps to fabricate multiple metal layers, providing the electrical interface between the components on-chip and between the components and the external devices. Electrical isolation of each metal layer is achieved by depositing a dielectric material after forming each metal layer. These layers are etched and filled with conductors to form vias that go through the dielectric and connect the routing metal layers, thereby forming a binary metal-dielectric pattern at any layer as shown in Fig. 1(a). In other words, any point on each layer can be chosen to be metal or dielectric by defining the routing metal and via patterns as long as the fabrication rules for minimum size features are not violated. These layers are often not composed of one single metal, but are often formed by a combination of layers of different metals. The same applies to the dielectrics. The first metal layer, closest to the components, is commonly referred to as *metal 1* (M1) with sequential numbering of the metals on the upper layers. Moreover, the via layer connecting metal 1 and metal 2 is referred to as *via 1* (V1) and the rest of the upper via layers are also sequentially numbered (Fig. 1(c)). Several metal layers are used in modern silicon processes with thicker layers closer to the top. They serve not only as interconnects but also as passive components (e.g., capacitors and inductors) that require high lateral and vertical etching and polishing precision to achieve high yield in mass production [36,37]. The top-most metal layer is often covered with protective passivisation layers with selective openings for electrical connection pads, as shown in Fig. 1(b).

The subtractive photonic method here relies on the controlled and accurate dimensions of the BEOL process and employs a post-processing step of etching the metals to form photonic structures. Figure 2 shows the process steps to fabricate subtractive photonic structures. Figures 2(a)-(h) are fabricated by the fabrication foundry without any change in their process flow, and steps (i) to (l) show the post-processing steps taken after the chips are fabricated to etch the metal masks and realize the photonic structures. Metal structures are patterned in the design phase to serve as a sacrificial layer. By defining the patterns of the metal and via layers, a multilayer structure of metal-dielectric is fabricated by the fabrication foundry. The metals are connected to a top pad layer through a metallic pathway. Therefore, once the metal etchant is introduced to the chip in the post-processing step, it dissolves the targeted metallic sacrificial layer, starting with the exposed pads, flowing into the chip, and removing other metallic structures that are connected to the pads through metal routing. As a result, this process leaves behind a dielectric structure which is designed to form a photonic component (Fig. 3(a)). For instance, a dielectric slab surrounded by metal that will be replaced by air after etching can serve as an optical waveguide. These suspended structures may need mechanical supports which are formed using the same dielectric by defining proper metal patterns. Figure 3(a) shows these support structures for the photonic components that are periodically repeated along the waveguides and other components. Moreover, for the rib waveguides, the rib slab that runs along the waveguide and is part of it, plays the role of the support structure as well. The photonic components are fabricated in multiple layers and can interact with each other either through physical connections or evanescent coupling. Moreover, the fabrication of 3D photonic structures is feasible using a stack of multiple dielectric layers. The minimum and maximum feature sizes depend on the capabilities of the

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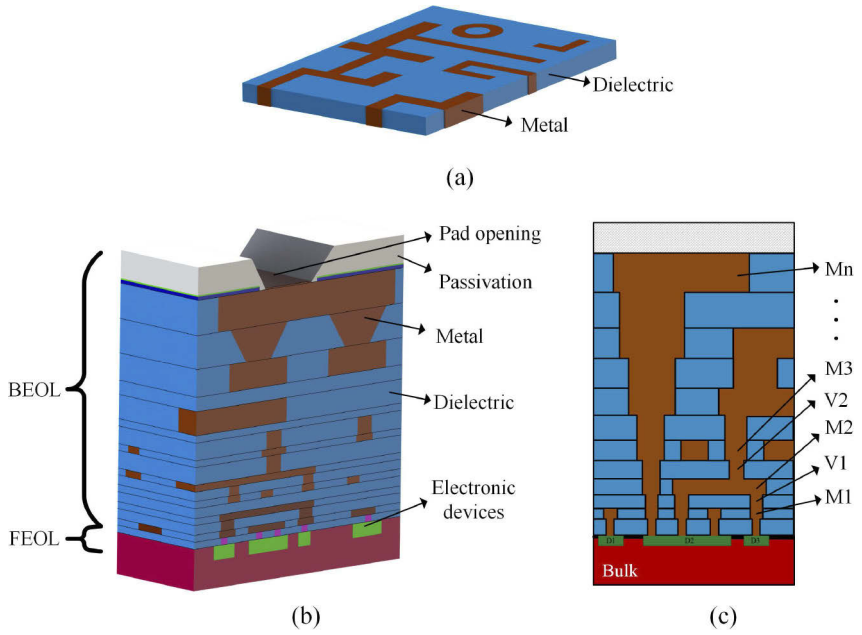

Fig. 1. Graphical representations of (a) a single layer of the stack, which is a binary layer of metal and dielectric (the metal and dielectric regions are defined by a patterning process), (b) a typical bulk silicon electronics platform with several metal layers, and (c) a typical cross section view of the chip showing metal routing and via layers used for interconnect.

fabrication process. The minimum feature size is limited by the minimum via size (which is roughly 0.1 µm by 0.1 µm in the presented work for the lower layer vias, up to via 7, and less than 0.4 µm by 0.4 µm for upper layer vias) and the maximum is limited by the minimum metal density rules (which allows for components as large as 100 µm in the presented work here).

The dielectric material of each layer is uniform horizontally, so metal is etched in the post-processing to form the photonic, support, and wall structures. While the dielectric material is different for some layers (for example SiN is used for the upper layers), most of the layers have similar material, which is often the common material used in similar process flows across different foundries. While support is on the same layer as the waveguides and has the same dielectric material, the walls extend to the bottom of the stack and if different dielectrics are used for the bottom layers by the foundry, the bottom part of the wall will consist of those dielectric types. However, the walls are just for mechanical support and do not interfere with the photonic design.

An alternative approach to form photonic structures is using the dielectric as cladding and filling the vacancies after metal removal with a secondary material, such as liquid crystal, under a vacuum chamber (Fig. 3(b)). This secondary material plays the role of the core for the waveguides and other components. Therefore, higher index photonic components surrounded by the lower index dielectric layers are formed that not only have better optical confinement, but also potentially have nonlinear optical properties that can be used for various applications. Figure 4 shows the post processing steps taken after the fabrication of the chip to realize these types of photonic structures.

Apart from the sacrificial metal parts that are intended to be removed by etching, some of the metal interconnects can be left for electrical access to the components. Since any electrically active circuit needs pad access (at least for the voltage supplies), the electrical pads are designed without passivation openings and are accessed by removing the passivation after the etching

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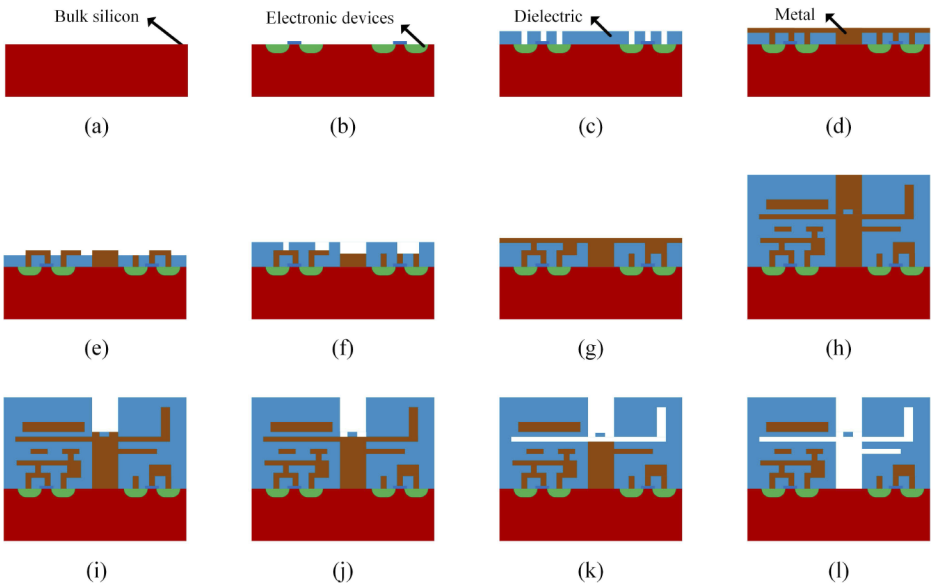

Fig. 2. Simplified process steps of subtractive photonics that leads to the fabrication of a dielectric waveguide surrounded by air. The support structures of the waveguide are not shown in this cross section. (a)-(h) Standard fabrication flow of the foundry used which is not affected by the method presented here and (i)-(l) are the post processing steps. (a) Prepared silicon substrate (b) Electronic devices are fabricated via several steps of the FEOL (c) first dielectric layer is deposited (d) dielectric layer is etched to form the first layer via (d) first mental layer is deposited (e) first metal layer is patterned and etched (f) second layer dielectric is deposited and etched (g) second metal via layer is deposited (h) performing the steps (c) to (e) successively the full metal stack of BEOL is fabricated with passivation layers on the top. (i) First etching step which dissolves the top layer metal and stops at the etch stop layer. (j) second etching step to remove the etch-stop-layer (k) third etching layer to remove metal layers (l) successive application of the etchants to remove the metals of the stack which are connected to an exposed top-layer metal.

process. This leaves the electronic circuits' interconnects intact. Since these photonic structures are built on an advanced electronic integration platform, the available high performance transistors can be used to implement circuit networks that actively interface with the photonics. Moreover, for light in the visible range, the bulk silicon can be used to realize photodetectors [38] in close proximity to transimpedance amplifiers (TIA), providing compact, integrated, and potentially high speed integrated electronic-photonic systems. It should be noted that the planarity of the BEOL layers is not affected by the implementation of these structures if the minimum and maximum metal density rules requested by the fabrication flow is satisfied. Since the metal structures are usually only a multiple of a wavelength wide, they do not face the restrictions of maximum metal density. However, the spacing between photonic components and the dielectric wall width can always be increased to reduce the metal density if needed. Furthermore, to satisfy the minimum density rules, dummy metals can be added across the surface at each layer. The design rules in the processes are optimized by the foundry to guarantee high yield for electrical connections such as metal structures with low resistivity and high quality. However, in many analogue circuit designs when multiple inductors are used these rules can be waived. The process will still be reliable but the chance of having some faulty electronic chips increases. Here, the metals are etched and the electrical resistance of the vias are not important for the

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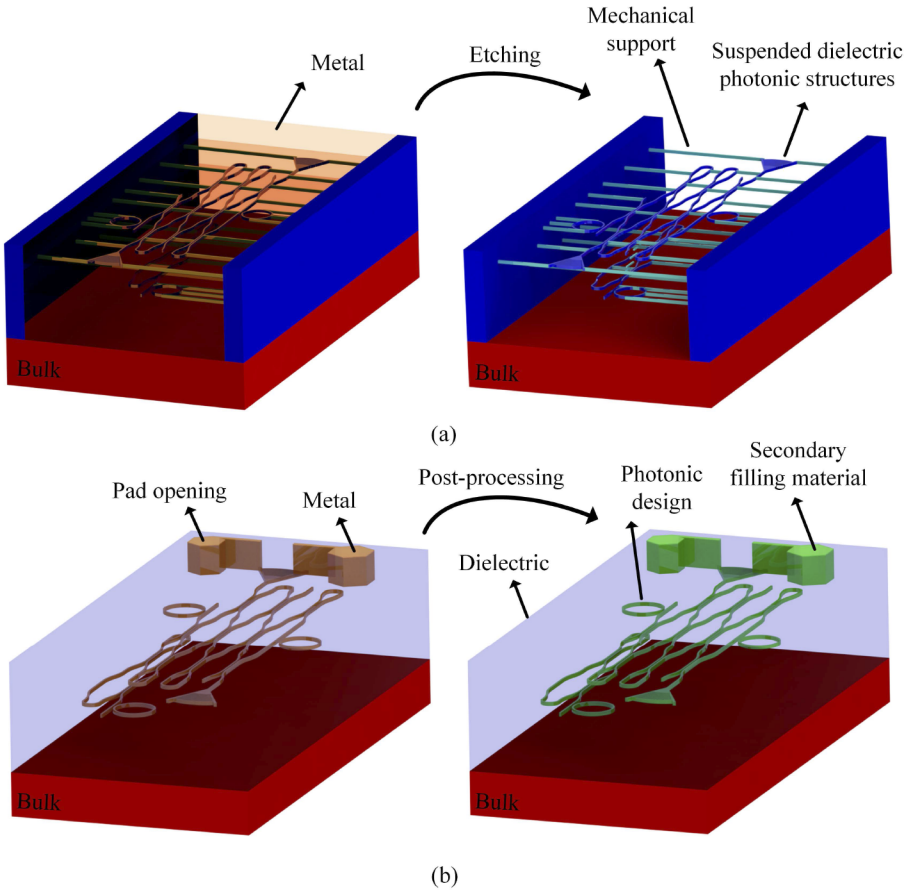

Fig. 3. Schematic of the realized photonic structure through subtractive photonics. (a) Interlayer dielectrics are used to form waveguides and other photonic components, while the metals serve as sacrificial layers. (b) The empty space left after etching the metals is filled with a higher index material as the guiding core.

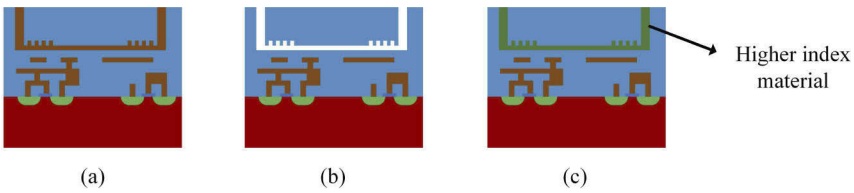

Fig. 4. Simplified process steps of subtractive photonics with a higher index secondary dielectric spin coated on the structure to fill in the vacancies. This secondary material plays the role of the core for the waveguides and other components. Here, it is shown how the support structures of two grating couplers are used to provide a channel for the secondary material. (a) the fabricated chip by the foundry (b) etching and removing the metals (c) filling the vacancies with the secondary material through spin coating.

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designs. Therefore, many of the electronic design rules can be ignored, allowing a broader range of photonic components.

Since there are several metal and dielectric layers available on any modern process, a variety of single- and multilayer dielectric waveguides and photonic components can be fabricated. These dielectric layers usually have different thicknesses ranging from a hundred nanometers to several micron, which provides an extra degree of freedom for designing optical components at different wavelengths. Additionally, a stack of multiple adjacent layers can be used to form a thicker dielectric layer or a photonic structure with a varying vertical profile. To form a dielectric waveguide with air cladding, a dielectric slab should be surrounded by top and bottom metal layers which are connected by metal vias such that after etching the metal, a dielectric core with air cladding is formed. In general, the optical properties of electronic processes'layers are not often measured extensively in the optical range, and so additional measurements of such optical properties may be necessary using test structures. The refractive index of bulk silicon dioxide, n=1.44, is used here for mode analysis and photonic design. Although this platform can support a wide range of optical wavelengths, here the two wavelengths of 1.55 µm and 633 nm are used. The wavelength of 1.55 µm is commonly used for telecommunication applications, and so many low cost pieces of equipment are available, while 633 nm falls in the visible range of the spectrum, and so can be detected by silicon photodiodes formed in the bulk.

Figure 5 shows the design of multiple single-mode waveguides at λ=1.55 µm on bulk CMOS platforms using different dielectric layers. It is possible to construct a variety of integrated waveguides, including the two most commonly used in integrated photonics, channel and rib waveguides. Although each waveguide supports at least one TE and one TM mode, rectangular waveguides with a width-to-thickness ratio greater than 2 (similar to silicon waveguides on standard SOI silicon photonic platforms) have a poorly confined TM mode and suffer from relatively large scattering loss. To account for small refractive index deviations from silicon

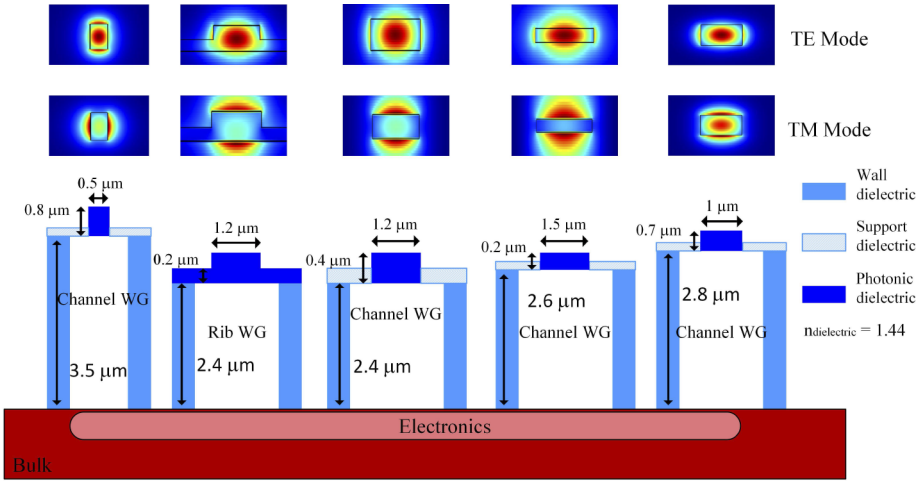

Fig. 5. Cross section schematic of certain generic waveguide design examples for $\lambda = 1.55\mu m$ and their simulated supported mode profiles, with the possible support structures made of dielectric materials connecting the suspended waveguides to a dielectric wall using periodic slabs. The refractive index of the dielectric at this wavelength is $n_{dielectric} = 1.44$. It should be noted that the support structures in the figure shown with a different color are not uniformly extended along the waveguides and periodically repeat at certain lengths as Fig. 3 demonstrates. The three labels, photonic, support, and wall dielectrics are used to show the role of each section in the design not the composing material.

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dioxide, the width of the waveguides are chosen with a safe margin to avoid the propagation of higher order modes while achieving sufficient mode confinement. Figure 6 shows the designs of single-mode waveguides for λ=633 nm. Supporting a wide range of wavelengths not only provides the possibility of multi-wavelength operation, but also enables harmonic generation and handling for the complementary structures discussed above, in which a secondary material with nonlinear properties is applied after etching to form the core of the waveguides. In addition to the waveguides, a support structure network has to be designed to mechanically stabilize the components. In this work, the support structure consists of periodic slabs connecting to the cavity wall.

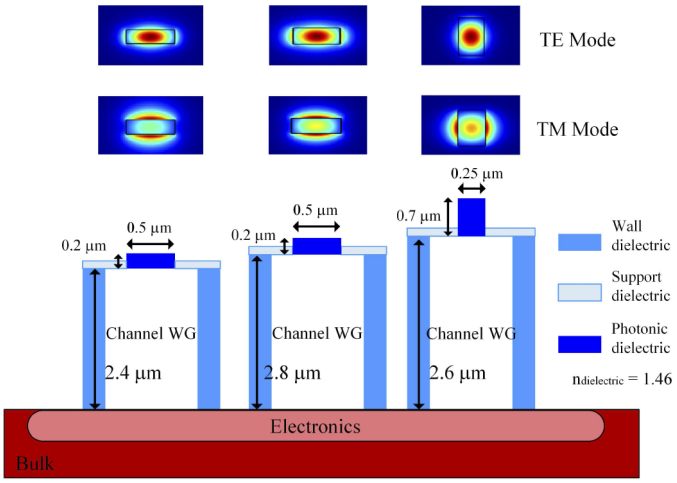

Fig. 6. Cross section schematic of various waveguide designs for $\lambda = 633nm$ with their supported mode profiles. The refractive index of the dielectric at this wavelength is $n_{dielectric} = 1.46$. The support structures are made out of the same dielectric material that connects the suspended waveguides to a dielectric wall using periodic slabs. The three labels, photonic, support, and wall dielectrics are used to show the role of each section in the design not the composing material.

3. Component design and experimental results

To demonstrate the feasibility of the method, as well as characterize the optical properties and the performance of the photonic components, several structures at the two wavelengths λ=1.55 µm and λ=633 nm are fabricated. In order to measure the material and scattering loss of the optical waveguides, several channel and rib waveguides for each wavelength, for different layers, and for different lengths, are designed. Edge coupled waveguides, which are identical apart from their length, are used to determine the optical loss. With the waveguide loss known, the optical loss of other components can be determined through direct measurement. The edge couplers are implemented as waveguide tapers which are followed by a full metal stack. This metal stack will be removed through the etching step and create space for fiber coupling. Therefore, a nicely defined surface for the couplers will form without the need for chip dicing and polishing performed in standard photonic platforms.

To characterize the refractive indices of the dielectric layers, diffraction properties of the grating couplers are used. Grating couplers offer a promising path in light of the phase matching condition

$$k_a sin(\theta) = \beta_o + \frac{2\pi\nu}{d}, \quad \nu = 0, \pm1, \pm2, \ldots \tag{1}$$

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where λ_a is the wavelength in air, $k_a = 2\pi/\lambda_a$, d is the grating period, and β_o is the propagation constant along z of light coupled into the grating, which should be nearly matched to the propagation constant of the waveguide that is being coupled into [39]. For a grating coupler designed with a particular λ, θ, β_o, and ν, a measurement of $\theta + \Delta\theta$ gives an estimate of $\Delta\beta$, where $\beta + \Delta\beta$ is the effective propagation constant of the fabricated waveguide. Repeating this measurement for grating couplers designed for various angles and various waveguides reduces the uncertainty. Moreover, the characterization of grating coupler performance is inherently valuable, as they are an important component in integrated photonic design. It should be noted that an alternative structure to determine the optical loss and refractive indices are Mach–Zehnder interferometers (MZI) with a fixed length difference between their two arms. In the spectral response of the MZIs, the extinction ratio can be used to determine the waveguide loss [40] and the transmission versus wavelength yields the refractive index. In addition to the photonic structures, etching test structures consisting of metal paths with differing widths, geometries, and stacked layers are designed to determine a post-processing condition that yields a reliable and clean etching of the metals in various scenarios.

Square shape openings with dimensions 75 µm by 75 µm are used to access the etchant channels on the chip which are less than 150 µm apart from each other. The channels used for the etchant to flow are 11 µm wide and have a height from the silicon substrate up to the top dielectric layer that is used to envelop the channels. Since the components are realized by patterning the dielectric layers with metals, most of the area around each photonic component is covered with metals to prevent the formation of dielectric layers above and below, in order to avoid unwanted evanescence coupling. There are abundant opportunities to introduce openings at the top of the chip to expose the metal stack to the etchant, as well as sufficient room around the structures for the acid to flow. It should be noted that the metal structures turn into etchant channels after the metal is dissolved. The flexibility in adding additional openings all over the chip relaxes any limitations on etchant flow. In the most extreme case, the entire top of the chip can be designed as a large opening. Moreover, since the photonic structures are much smaller than the metal structures, having multiple photonic waveguides on different layers next to each other has negligible effect on the etchant channel sizes and will not be a limiting factor.

Different metals with different thicknesses are used at each layer for fabrication of the chip, which requires a controlled etching process to realize the designed structures. The quality of the etch in the post-processing step depends on the type of the etchants used and its environmental conditions. After some experimentation, the following etching process was found to be successful: one hour in Transene Aluminum Etchant Type A at 80 °C followed by one hour in a 1:1 solution of H_2O_2 and EDTA at 80 °C, repeated until the photonic structures are fully exposed.

Figures 7(a) displays the state of a test structure after an hour in aluminum etch. The etchant has dissolved through most of the metal (Type A is also an excellent copper etchant [41]) and left a thin layer over the grating coupler that has been naturally peeled back in some cases. This thin layer appears to be the etch stop layer used in interconnect formation, and can be effectively removed with the hydrogen peroxide/EDTA solution. Figures 7(b)-(e) show the etching result subsequent to applications of H_2O_2/EDTA etch. To protect the photonic structures, the top passivation layer can be retained by not including the pad opening mask except in particular locations. Therefore, photonic structures can be enclosed inside the chip in cavities. However, to achieve an efficient metal etching, there should be regular openings neighboring the structures for the etchant to flow freely. Waveguides can be seen in Fig. 7(d) through the etchant openings (square) and underneath the oxide between openings.

Figure 8(a) shows a scanning electron microscope (SEM) image of the dielectric stack after etching the full metal stack next to it. Since metal layers should enclose the via layers by the fabrication rules, the dielectric layers have a step profile in the horizontal direction. As explained earlier, these layers have different thicknesses, with the upper layers typically being thicker, up to

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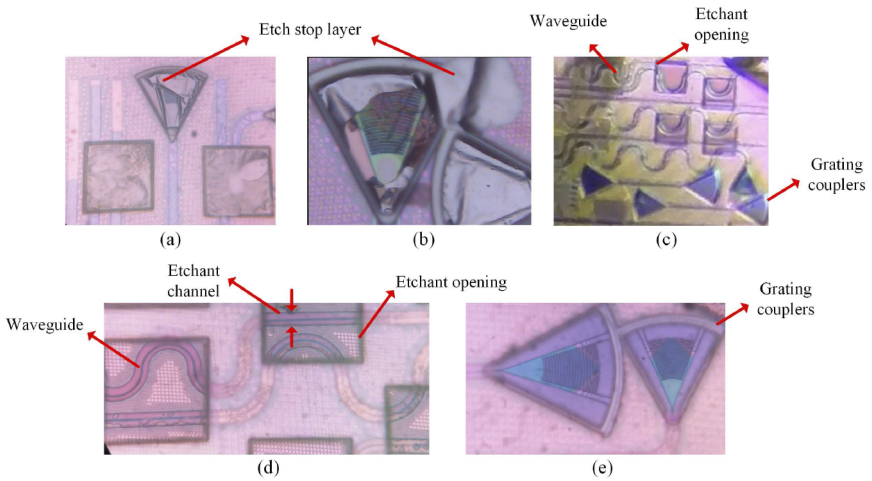

Fig. 7. (a) Test structures after initial aluminum etch. (b), (c), (d), & (e) Test structures after H_2O_2/EDTA etch.

a few microns. A cross-sectional view of a waveguide before etching created using a focused ion beam (FIB) is shown in Fig. 8(b). The outline of the dielectric waveguide, which has a trapezoidal shape, is clear from the surrounding metals. The partially etched metals are shown in Fig. 8(c) for a better view of the structure. Figure 8(d) shows an SEM image of the cross section of a rib waveguide test structure, with the top passivation removed after the post-processing metal removal step. The thin dielectric slab of the rib waveguide allows the waveguide to remain suspended in the cavity between the top passivation and the bottom substrate after removal of the metal layers. The controlled geometry of the metal layers yields a relatively smooth waveguide surface with small surface roughness. Figure 8(e) shows a zoomed-in view of the waveguide, which shows surface roughness of less than ten nanometers. A suspended channel waveguide with its mechanical support structure is shown in Fig. 8(f). Mechanical supports are narrow to minimize the optical mode disturbance and are an extension of the same dielectric material.

The mature BEOL process of advanced electronic fabrication processes allows for well-defined photonic structures. Figure 9 shows the zoomed SEM images of a waveguide, Y-junction splitter, and gratings of a grating coupler, demonstrating a smooth surface with less than 10 nm surface roughness. The small index difference between the dielectric and the surrounding air leads to a relatively small loss for surface roughness with rms values of less than 10 nm. Simulation of the waveguide on via 7 layer with 7 nm rms roughness shows a waveguide loss of 0.4 dB/mm.

Figure 10 shows SEM images of some of the fabricated components. Figures 10(a) & (b) show a symmetric Y-junction splitter on Via 7 layer with an input dielectric waveguide delivering the light and the two output waveguides collecting the equally split power. A 3 dB splitter is a frequently used component in integrated photonic platforms and a Y-junction splitter performs this function with a relatively small footprint. Moreover, one of the fabricated grating couplers is shown in Figs. 10(c) & (d). The focusing grating couplers are used to couple the light into and out of the on-chip waveguides. It should be noted that not all the structures were successfully fabricated. Depending on the number of mechanical supports, thickness, and material composition of the dielectric layers, some of the fabricated components either got detached from the chip or ended up resting on the bottom of their cavities. This happened in particular in the lower dielectric layers, which are relatively thin. However, it is advantageous to study these structures in order to evaluate the possibilities for future design, and understand what number of mechanical supports are required to realize specific components in each layer.

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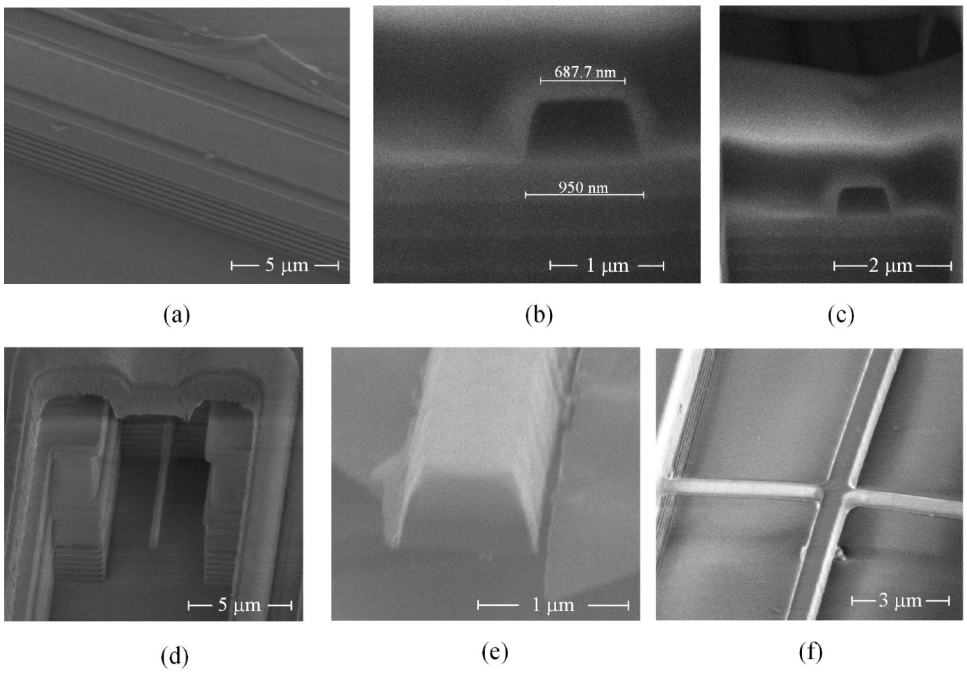

Fig. 8. SEM images of (a) a stack of metal layers etched, showing the side wall of all the entire dielectric layers, (b) a cross-sectional view of a dielectric channel waveguide created using focused ion beam (FIB) prior to etching of the metal layers, (c) the same structure in part b with the upper metal partially etched, (d) a fully etched rib waveguide structure leaving a suspended dielectric waveguide, (e) a dielectric waveguide with small surface roughness, and (f) a dielectric channel waveguide with a supporting structure.

The method of etching an electronic chip to create photonic structures presents several challenges that future works must address. The primary concern is the mechanical strength of the waveguides. This challenge can be addressed by using rib waveguides with a large cross section, which provide superior strength and modal confinement, but are also likely to support many modes. Analytic criteria for single mode large cross section waveguides have been proposed [42,43], but it has been shown that these criteria are insufficient for ensuring single mode behavior in general, so waveguide geometries must be determined numerically [44]. Moreover, several MEMS systems [29–31] have used the technique of etching metal structures on silicon chips in post-processing, which can be used to analyze and design structures with better mechanical stability.

The test setup for characterizing a waveguide and its input/output grating couplers is shown in Fig. 11. This test structure (TS1) consists of two grating couplers connected by a 300 μm long waveguide designed at wavelength λ=1.55 μm. Figures 12(a) & (b) show the optical power measured passing through the structure by raster scanning a fiber over each grating coupler, with the fiber slightly backed off from touching the chip surface. The peak coupled power is −33 dBm, giving a total fiber-to-fiber loss of 46 dB. Sweeping the polarization resulted in 12 dB variation in the coupled power. In addition to TS1, an empty cavity with no waveguide and grating coupler is fabricated as shown in Fig. 11, called test structure 2 (TS2). An empty test structure is useful as a control to determine how much power is actually coupled into the waveguide of TS1, rather than propagating through the cavity. Figures 12(c) & (d) display the power coupled through the empty test structure (TS2), with a maximum coupled power of −45 dBm giving a fiber-to-fiber

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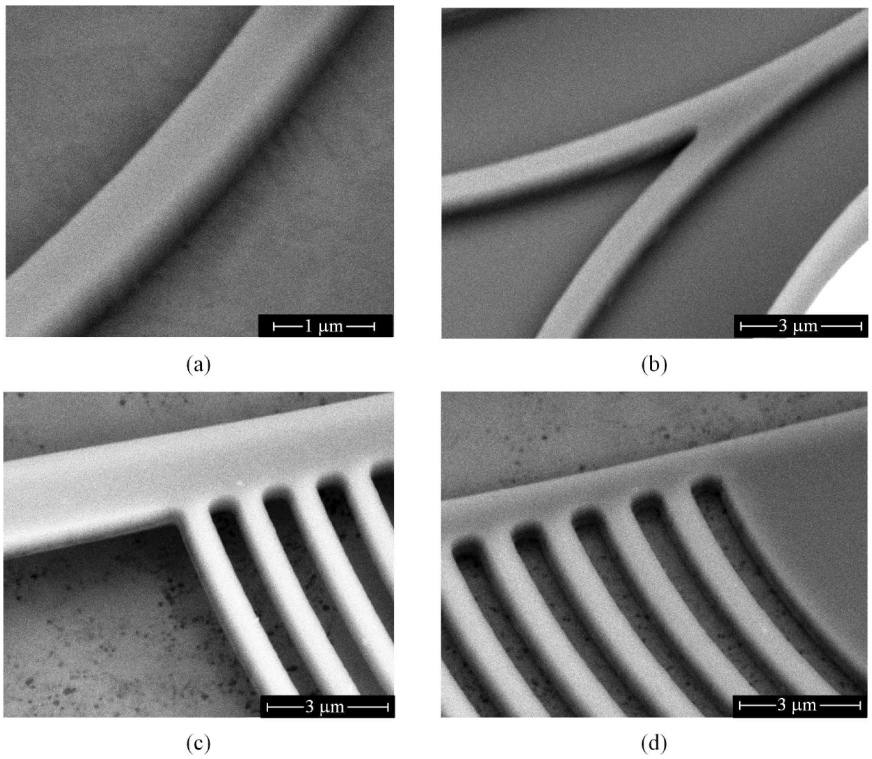

Fig. 9. SEM images of photonic structures that show a smooth surface after etching the top-layer metal (the etch stop layer underneath the waveguides are not fully etched). These images are taken with the maximum SEM resolution available and show little surface roughness.

loss of 58 dB. Varying the polarization resulted in 16 dB variation in the coupled power. The 12 dB difference in coupled power between TS1 and TS2 indicates that power is indeed coupling into the waveguide of TS1. However, these proof-of-concept measurements should not be taken as the final performance limits of this approach. There is potential for significant improvement in the waveguide coupling through optimization of the structural design and the etching process.

The loss reported here is the total loss of the two grating couplers and the 300 µm long waveguide (in contrast to the mature processes that report the waveguide loss separately). Given that good performance grating couplers on silicon photonics platforms have typically 6 dB of loss, we expect to have 10 dB loss from the grating couplers at this stage of development. Therefore, we estimate 20 dB of loss being originated from the two grating couplers. The waveguide is 300 µm long with several support structures. Since the optical characteristics of an electronic process are not characterized by the foundries, we expect a significant loss from the mismatch caused by several support structures along the waveguide which can be avoided in future designs.

The waveguides are 300 µm long and are collapsed on the bottom of the cavity. In many cases the waveguide is also pushed against the sidewall of the cavity. The consequent coupling into the substrate greatly inflates the loss of the waveguide compared to a properly supported freestanding structure. While here, the port-to-port coupling loss is reported, future works will improve on various aspects of this method and report the loss of the waveguide, support network, and grating couplers separately. Considering the low dielectric loss and the fabricating results presented here for waveguides, we believe that the optical loss of this platform can be competitive with the state-of-the-art processes when fully developed.

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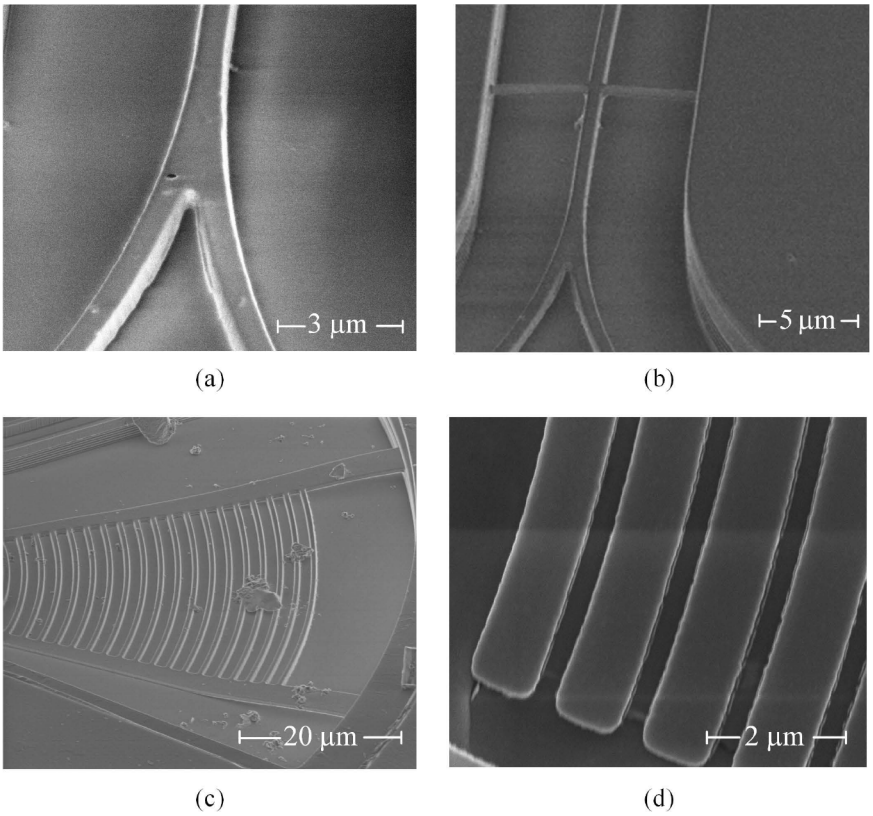

Fig. 10. SEM images of (a) a Y-junction splitter, (b) the same suspended Y-junction splitter with input waveguide, (c) a grating coupler, and (d) gratings of a grating coupler.

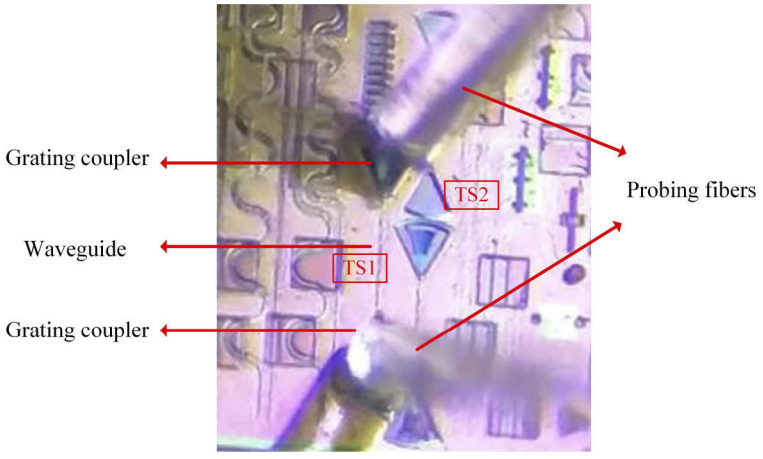

Fig. 11. The fabricated chip with various photonic structures in a measurement setup.

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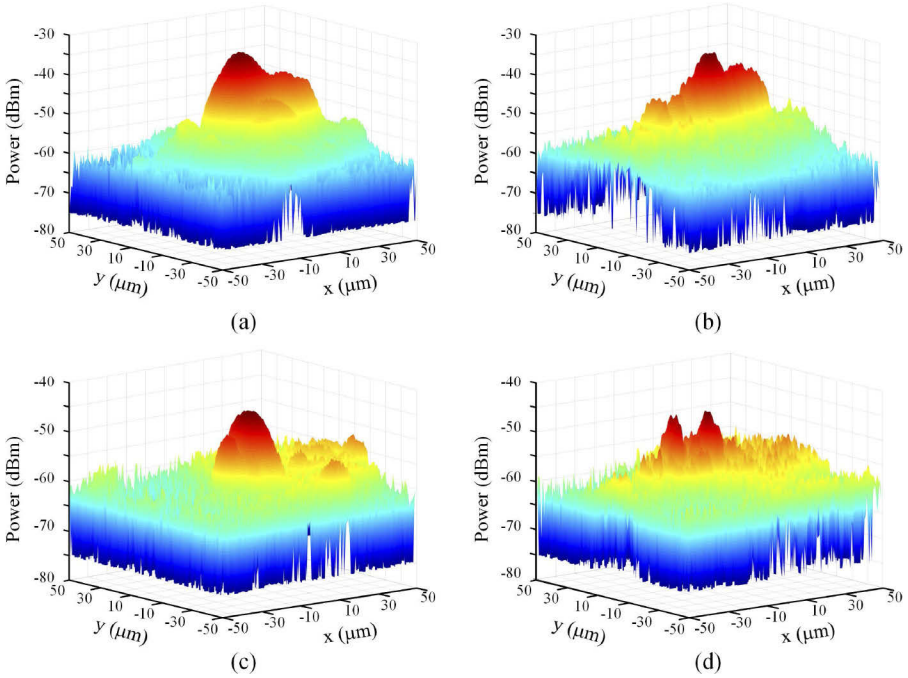

Fig. 12. Power collection of the fiber probe over a 100 μm by 100 μm area with 13 dBm input power at λ=1.55 μm. (a) & (b) Raster scan over the first and second ports of TS1 (Fig. 11), yielding a peak power of −33 dBm. (c) & (d) Raster scan over the ports of TS2 (Fig. 11), yielding a peak power of −45 dBm.

One of the challenges is the uncertainty about the exact materials used in the process and their properties. The variety of materials present in a CMOS chip present difficulty in determining the relevant optical, thermal, and mechanical properties, as they require a large number of test structures to independently evaluate each property. As a proof-of-concept, our test chip was merely intended to determine the viability of etching metal layers on a CMOS chip to form photonic structures, and can be applied to future works on extensive evaluation of the platform.

It is worth noting that several functionalities such as photodetection, modulation, and light generation can be added to the presented method much easier and more efficiently than conventional methods. For photodetection, silicon in the bulk can be used to form visible photodetectors (these kinds of photodetectors are currently used for image sensors). Moreover, there are heterogeneous electronic processes that use Si-Ge to form BJT transistors and if such a process is used, photodetectors at telecom wavelengths (such as 1550 nm) can also be implemented. It should be noted that photodetectors appeared much later in silicon photonics processes and even today, growing germanium for photodetection is the bottleneck of the process yield. However, the possibility of using the germanium layers used in electronics can offer an easier and more efficient path to achieve this functionality. In addition to these integrated solutions, discrete photodetectors can be flipped on the chip in a manner similar to some photonic platforms.

Regarding light generation, due to the numerous challenges in implementing optical sources on the chip, even in dedicated and mature silicon photonic processes, an external source is coupled to the chip or a laser die is flipped on the chip. While the same approaches can be used in this method as well, the presented method can have the possibility of adding a secondary material to

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the chip that can be used in constructing a light source on the chip. This is an interesting subject well suited to the future research and development.

Thermal modulators can be implemented using metal resistors that dissipate power and change the dielectric temperature similar to the thermal modulation mechanism used in standard silicon photonic platforms. Moreover, with the option of spin coating a secondary material (which can be a nonlinear material), more efficient modulators compared to standard photonic structures can be achieved. It should be noted that integration of nonlinear materials in standard silicon photonics platforms adds a great deal of complexity, while it is easy and natural to implement in the subtractive photonics approach.

4. Conclusion

In this work, a subtractive photonic fabrication method for realizing complex multilayer photonic structures in a low-cost electronic integration platform is demonstrated. This concept is investigated and the capabilities of this process are demonstrated by fabricating various proof-of-concept structures. To characterize the optical properties and fabrication quality of this technique, photonic structure components are implemented and fabrication and measurement results are presented.

Disclosures. The authors declare no conflicts of interest.

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