Graphene photo memtransistor based on CMOS flash memory technology with neuromorphic applications - Supporting Information

Christian Frydendahl[1,†,*], S.R.K. Chaitanya Indukuri[1,†], Meir Grajower[1,2], Noa Mazurski[1], Joseph Shappir[1], and Uriel Levy[1,*]

[1] *Department of Applied Physics, The Faculty of Science, The Center for Nanoscience and Nanotechnology, The Hebrew University of Jerusalem, Jerusalem 91904, Israel.*
[2] *Thomas J. Watson Laboratory of Applied Physics, California Institute of Technology, Pasadena, CA 91125, USA.*

†*These authors contributed equally to this work*
**christia.frydendahl1@mail.huji.ac.il and ulevy@mail.huji.ac.il*

Number of pages: 4

Number of figures: 3

Full IV-sweeps

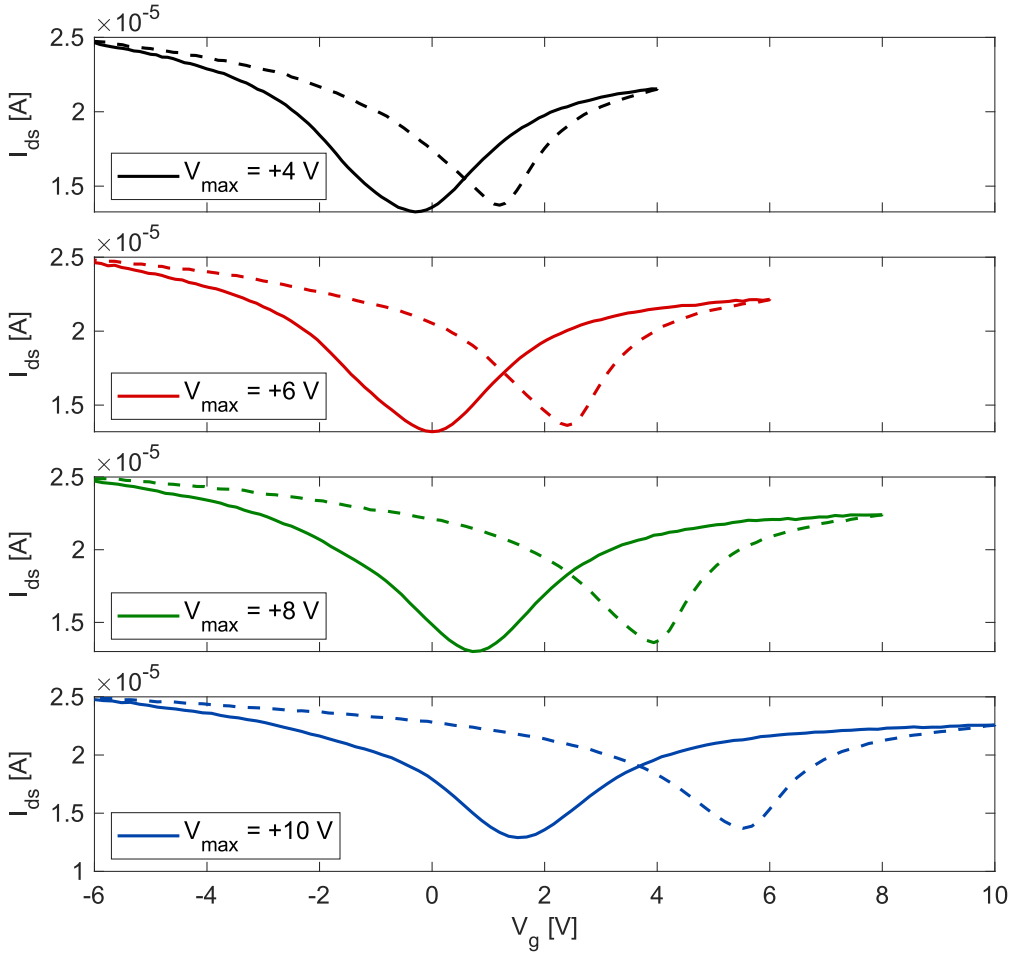

Figure S1: Full IV-sweeps of the graphene memory transistor. The sweeps all start at -6 V and increase in voltage until V_{max} (solid lines). Then, the sweep goes down from V_{max} back to -6 V (dotted lines). The sweeps are measured in sequence, starting with V_{max} = 4 V, and sequentially increasing V_{max}.

Retention time measurements

We find that to fit the decay of the current seen in main paper Fig. 4, we need fit with a two-term exponential function:

$$I(t) = I_0 e^{-t/\tau_0} + I_1 e^{-t/\tau_1}. \tag{1}$$

The resulting fits for right after a positive and right after a negative gate spike can be seen in Fig. S2. The respective time constants can also be seen in Fig. S2.

If we ignore the fast decays times, τ_0, we find that the average of the two τ_1 values is $\sim$45 min. This means that roughly 50% of the current is expected to be maintained after 45 min.

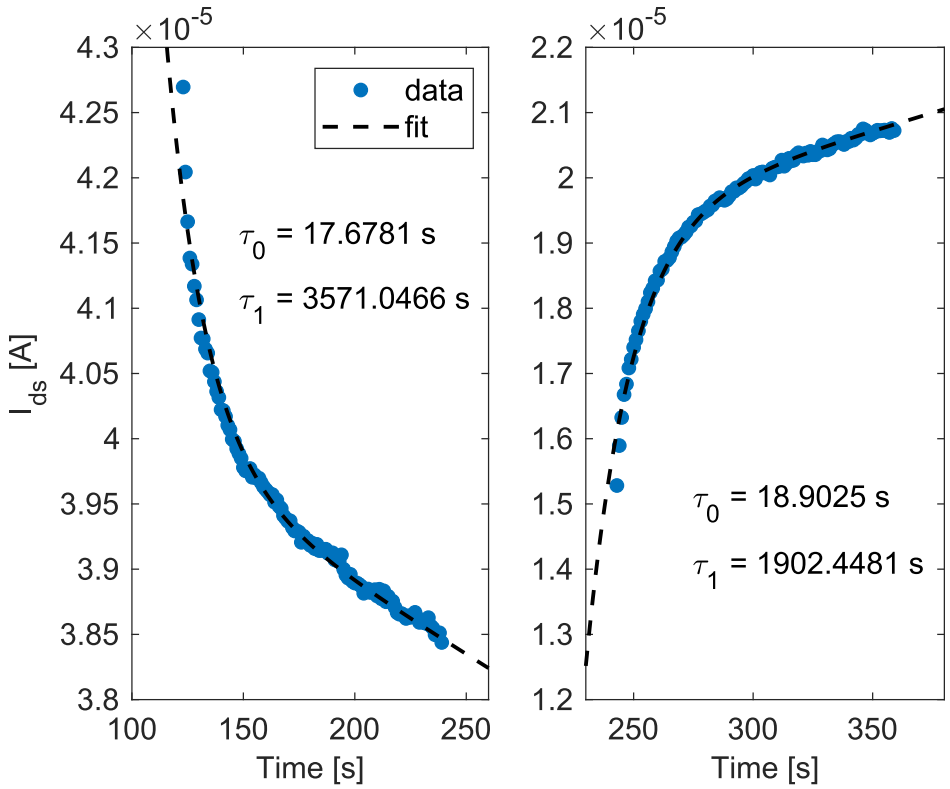

Figure S2: **Left:** Decay of current right after a positive +15 V gate. **Left:** Decay of current right after a negative -10 V gate.

Supplementary discussion

Improving On/Off ratio: To explain how the On/Off ratio can be improved, we need to introduce a few general concepts common to graphene field-effect devices, see Fig. S3 below. Here we show the conductivity ($G = 1/R$) of a graphene conductive channel, versus an applied electric field from a gate electrode, V_{G}. This is analogous to our device, except here there is no floating gate/nitride trapping layer.

In Supplementary Fig. 1 we have defined two concepts, the intrinsic doping G0, and the Dirac point voltage, VD. The intrinsic doping sets the minimum conductivity of the graphene sheet, i.e. the conductivity at the charge neutrality point, VD. This is exactly the point at which the applied external field brings the graphene's Fermi level to 0.

The on/off ratio of the device is then given by how much the conductivity changes versus the applied gate, i.e. the slope of the curve in Fig. S3:

$$\frac{dG}{dV_{\mathrm{G}}} \sim \frac{\Delta G}{\Delta V_{\mathrm{G}}}.$$

This slope is largely determined by the mobility of the charge carriers in the graphene, μ. The mobility is determined by the overall quality of the graphene, i.e. how pure it is from external contamination, is it free from lattice defects, etc. This is because such contamination and defects add local scattering sites for the charge carriers, inhibiting their uninterrupted movement through the graphene sheet.

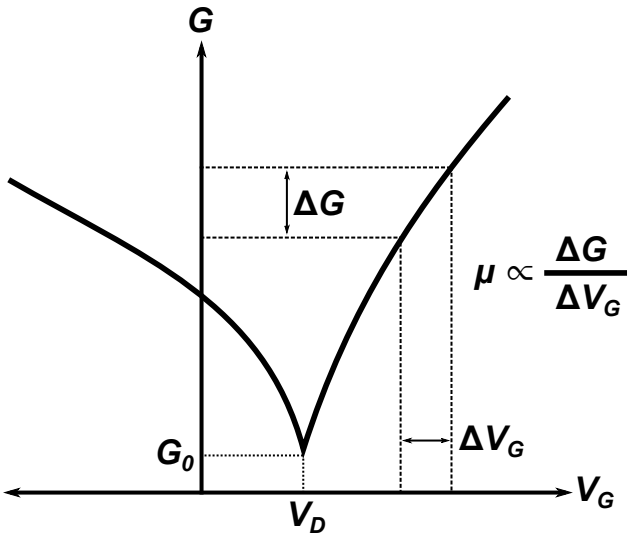

Figure S3: Graphene conductivity, G, versus applied electrostatic potential via a gate, V_{G}.

Apart from optimizing the graphene sheet's quality, it is also important to operate the device in the regime of the largest slope. Generally, this is in the low doped n-doped region, as the electrons normally have higher mobilities than the holes, and too high doping in general will limit the charge carrier's mobilities from electron-electron scattering and the energy dependent mobility in graphene (higher doping means higher Fermi level for the charge carrier distribution function as well).