TSV-Last Integration to Replace ASIC Wire Bonds in the Assembly of X-Ray Detector Arrays

Jennifer Ovental Hicks
Micross AIT
Durham, NC, USA
Jennifer.Ovental@micross.com

Dean Malta
Micross AIT
Durham, NC, USA
Dean.Malta@micross.com

David Bordelon
Micross AIT
Durham, NC, USA
David.Bordelon@micross.com

Daniel Richter
Micross AIT
Durham, NC, USA
Daniel.Richter@micross.com

Jaesub Hong
Center for Astrophysics
Harvard & Smithsonian
Cambridge, MA, USA
jhong@cfa.harvard.edu

Jonathan Grindlay
Center for Astrophysics
Harvard & Smithsonian
Cambridge, MA, USA
josh@cfa.harvard.edu

Branden Allen
Center for Astrophysics
Harvard & Smithsonian
Cambridge, MA, USA
ballen@cfa.harvard.edu

Daniel P. Violette
Center for Astrophysics
Harvard & Smithsonian
Cambridge, MA, USA
daniel.violette@cfa.harvard.edu

Hiromasa Miyasaka
Space Radtiation Laboratory
California Institute of Technology
Pasadena, CA, USA
miyasaka@srl.caltech.edu

2021 IEEE 71st Electronic Components and Technology Conference (ECTC) | 978-1-6654-4097-4/21/$31.00 ©2021 IEEE | DOI: 10.1109/ECTC32696.2021.00038

***Abstract*— This paper will describe the use of through-silicon vias (TSVs) in a readout application-specific integrated circuit (ASIC) chip to replace wire bonds in the assembly of cadmium zinc telluride (CZT) X-ray detector arrays for space telescope applications. The TSV packaging approach includes solder bump connections from the back of the ASIC to the underlying board. This approach will greatly reduce the spacing between adjacent detectors in an array, eliminate potential damage to wires during assembly, and avoid any interference, which the wires can pick up during operation.**

We report a TSV-last integration process for the mixed signal ASIC chip used to read signals from the CZT detectors. The TSVs were integrated into existing ASIC wafers without any required redesign, and formed as blind vias from the frontside of the ASIC in metal-free areas adjacent to the wire bond pads. The TSVs were then connected to the bond pads using a routing metal layer. The wafers were bonded to temporary carriers and thinned from the backside, revealing the TSVs. After forming the redistribution lines (RDL) and under bump metallization (UBM), the wafers were released from the carriers and solder bumps were attached for subsequent assembly processes.

In the sections that follow, we will review the details of the ASIC wafer post-processing, including TSV fabrication, wafer thinning, frontside and backside metallization layers, and solder bumping. We will report electrical testing of TSV daisy chains and isolation test structures. Also, results of ASIC functionality testing, performed before and after TSV insertion, will be discussed.

Keywords— Through-silicon via, TSV, 3D Integration, X-ray detector, CdZnTe, CZT

I. INTRODUCTION

Three-dimensional (3D) integration, featuring through-silicon vias (TSVs) has emerged as a promising way to increase microelectronic circuit density while decreasing the size, weight, and power consumption of systems. TSV applications are varied, and come in the form of 2.5D interposers or true 3D integration with TSVs being directly inserted into integrated circuit (IC) chips [1, 2]. Fabrication of TSVs in IC wafers can potentially be done through one of three general process flows: 1) Vias-first, where TSVs are inserted before the fabrication of active transistors, 2) Vias-middle, where TSVs are inserted after transistor fabrication, but before back-end-of-line (BEOL) metallization, or 3) Vias-last, where vias are inserted after BEOL [3].

Vias-first is typically not feasible due to incompatibilities with transistor fabrication. Vias-middle is the most common production method for TSV insertion in device wafers. However, TSV availability from commercial semiconductor foundries is limited to specific products and wafer technologies. Companies making 3D products such as high bandwidth memory (HBM) or CMOS image sensors (CIS) are using TSVs in their products. Of the pure-play wafer foundries, which provide wafer fabrication services to external customers, some do not have TSV capability and others may offer TSVs only in select device technologies (usually the most recent nodes). The main driver for using the vias-last approach is to gain access to TSVs for applications and wafer technologies in which they are

NASA APRA Grant NNX17AE62G

2377-5726/21/$31.00 ©2021 IEEE
DOI 10.1109/ECTC32696.2021.00038

not available through the commercial wafer suppliers. If a few design requirements can be met, the TSV-last approach can potentially be used in nearly any wafer type from any foundry. In previously published work, Micross has demonstrated examples of successful TSV-last integration for infrared focal plane array detectors and phased array radar transceivers [4, 5].

In the present demonstration, we use a vias-last approach to insert TSVs into an already fabricated application-specific integrated circuit (ASIC) readout chip for an X-ray detector application. The ASICs are used in combination with cadmium zinc telluride (CZT) detectors to form high resolution x-ray imagers for use in space telescopes [6]. In a typical system, the CZT detector is bonded to the ASIC, which is then wire bonded to a printed circuit board (Fig. 1). However, to produce a high resolution imager, a large array of detectors needs to be assembled to the circuit board in close proximity. Wire bonding introduces a gap between detectors, wires are prone to damage during array assembly, and the wires can also pick up interference. The use of TSVs in place of wire bonds significantly reduces the gap and eliminates the potential wire damage and interference issues.

Our vias-last approach is unique in that TSV insertion is done from the frontside of the completed ASIC wafers (Fig. 2). Prior work in this area utilized a backside vias-last approach [7] from another supplier, which inserted TSVs into already thinned wafers from the backside, landing on aluminum bond pads on the frontside. This approach has some unique challenges and it can be difficult to achieve consistent, low resistance contact to the frontside metal with proper TSV isolation. A variety of difficulties were observed in the earlier attempts at backside TSV integration. In this work, the frontside vias-last process was demonstrated in the same ASIC wafers by forming the TSVs near the bond pads, in areas with no routing metal. A few of the wafer processes were performed through external suppliers, as indicated in the Acknowledgment section. All other steps were performed at Micross. In the sections that follow, we will describe some initial design and development activities, provide details of the TSV formation and related ASIC processing, and review the results of electrical testing of TSV test structures and ASIC chips.

II. Mechanical Wafer Processing and Assembly

In commercial TSV applications, such as high bandwidth memory stacks [8] and silicon interposers [9], the final wafer thickness is typically in the range of 50-100 µm. After wafer thinning, the debonding, singulation, and assembly operations are conducted using specialized methods and handling equipment, in order to minimize mechanical yield losses. For the lab prototyping effort described in this paper, we chose a greater final wafer thickness to make the ASIC layer robust enough to withstand more manual handling procedures through the required backend wafer operations and detector assembly processes. There are trade-offs with increasing thickness and TSV depth, as some TSV processes, such as liner depositions and plating, become more challenging as the TSV depth is increased. Also, with increased TSV depth, it is necessary to increase the via diameter to maintain the aspect ratio at a level compatible with these TSV processes. However, larger and deeper vias can increase stress-related concerns stemming from the coefficient of thermal expansion (CTE) mismatch between the copper TSV fill and the silicon substrate [10].

In order to identify a wafer thickness which could meet the TSV process and reliability requirements, as well as the chip assembly and handling requirements, we fabricated mechanical wafers of three different thicknesses for evaluation: 150, 200, and 250 µm. Two wafers of each thickness were fabricated using silicon test wafers. These were patterned with frontside aluminum pads to match the final I/O pads on the ASIC device wafers. The wafers were bonded face-down to glass carrier wafers and thinned by back-grinding and polishing to achieve the desired thicknesses. Following thinning, a spin-on dielectric passivation was applied and Ni/Au pads were formed for the solder bump interconnections to the board. Because the presence of solder bumps on the back of the wafer would complicate debonding from the carrier, wafers were debonded before bump placement occurred.

The thinned, released wafers were processed through flux application, solder ball drop, reflow, and flux cleaning steps. Next, the wafers were mounted to tape frames and diced. Crack formation was observed in half of the wafers, one wafer of each thickness, resulting from debonding, handling, and residual temporary adhesive. Based on the causes of these cracks, we

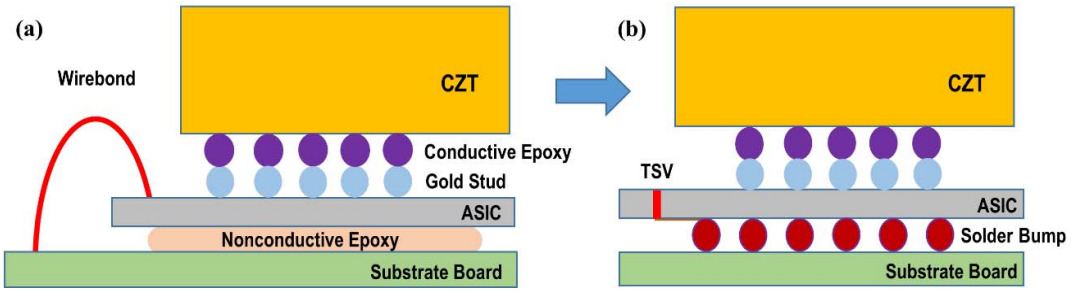

Fig. 1. (a) A CZT/ASIC assembly using traditional wire bonding to the substrate board (b) A CZT/ASIC assembly with TSVs in the ASIC chip providing connections to the substrate board [7]. The ASIC has 87 wire bond pads along one edge of the 20 mm chip. TSVs are inserted between pads.

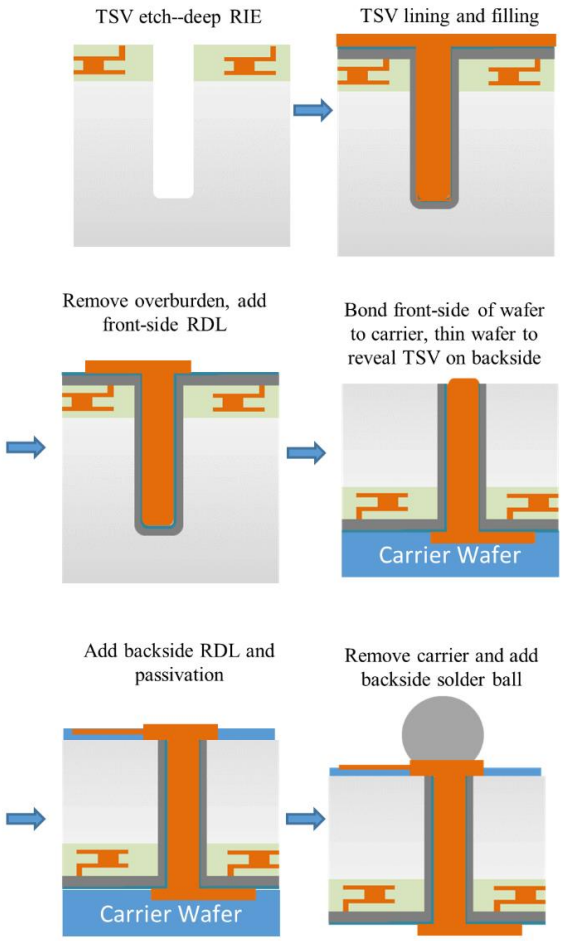

Fig. 2. Process flow for frontside vias-last TSV insertion into an already-fabricated ASIC device.

determined that any of these wafer thicknesses could be processed successfully with minor improvements in wafer handling and adhesive removal methods.

The bumped and diced mechanical chips were sent to the Harvard College Observatory to evaluate the required detector assembly operations. This includes a gold stud bumping operation on the front of the chips for bonding of the CZT layer, as well as a solder bump connection between the back of the silicon chip and the organic board. These assembly trials were completed successfully on chips of all three test thicknesses.

Based on the results of these mechanical wafer trials, we selected 150 µm as the target thickness for the ASIC wafers, as this was most favorable for the TSV etching, liner deposition, and plating processes. A thinner wafer with smaller TSVs would also help to lower the TSV-related stresses and potential for resulting wafer bow. A TSV diameter of 20 µm was selected to stay consistent with prior Micross process experience and to maintain the aspect ratio within the process window for the TSV liner depositions and plating. At an aspect ratio of 7.5, the 20 x 150 µm TSVs are fairly straightforward to line and fill. Furthermore, the 20 µm diameter is small enough that 3 vias could be inserted for every wire bond pad connection in the existing ASIC design, adding redundancy to ensure TSV interconnection for all wire bond pads. The addition of these redundant vias also increased the total TSV pattern density across the wafer, which was important for the TSV plating process, as will be discussed in a later section of this paper.

III. Fabrication of ASIC

The ASIC wafers, which provide readout of signals from the CZT X-ray detector layer, were designed at the California Institute of Technology (Caltech) [11]. They were fabricated on 200 mm wafers using ON Semiconductor's C5N process for mixed signal applications. This process uses low resistivity (≤0.02 Ω-cm) P+ silicon substrates. The wafers had aluminum I/O pads, which were part of a final unplanarized metal level (Fig. 3). The final passivation was opened over the I/O pads and detector pixel contacts at the wafer foundry. This resulted in some starting topography for the wafers, as shown in Fig. 3. In a frontside TSV-last insertion process, it is ideal to start with a planar surface. This is because the wafers need to receive chemical mechanical polishing (CMP) after TSV plating to remove the copper overburden layer from the wafer surface. Starting with a planar surface allows uniform removal of the plated overburden and TSV liners, with a consistent stopping surface. In the present work, the starting topography from the nonplanar final metal level and passivation openings required additional CMP process considerations. In the process of removing the metal overburden from the different surface heights, the CMP process was tailored to also eliminate the topography and produce a planar wafer surface for subsequent

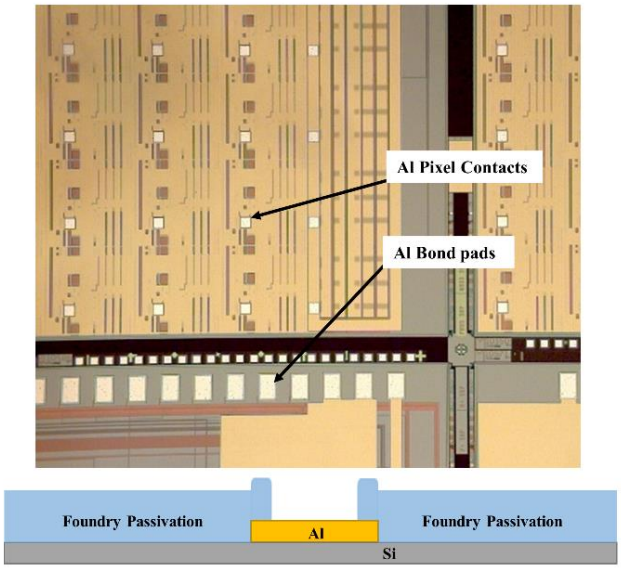

Fig. 3. Top image: the ASIC as received from the foundry. The Al pixel contacts and Al bond pads were exposed. Bottom image: a basic sketch of the incoming surface topography with the open Al pads.

process levels. Further details on the CMP process will be provided in the next section of this paper.

IV. TSV INSERTION AND RELATED ASIC PROCESSING

A. Blind TSV Formation and Frontside Metallization

Three ASIC device wafers were processed through the TSV insertion and related processing steps in preparation for assembly. After photolithography, TSV etching was done in two parts: 1) oxide via etching through the foundry dielectric stack using an inductively coupled plasma (ICP) etcher, and 2) silicon via etching using a Bosch deep reactive ion etching (DRIE) process. The ASIC wafers had several microns of foundry dielectric containing the high-density routing metal layers. There was no metal in the designated TSV etch areas adjacent to the wire bond pads. The total etch depths for all 3 device wafers were measured to be ~155-157 µm, within the targeted range of 155 +/- 2 µm. Cross-sections showed a vertical sidewall profile with low sidewall roughness.

The vias were lined with plasma-enhanced chemical vapor deposition (PECVD) TEOS oxide, which deposited approximately 0.25 µm minimum thickness near the bottom of the TSV. Next, a Ti/TiN barrier and Cu seed layer were deposited using ionized physical vapor deposition (iPVD). The iPVD Cu seed metal was supplemented with an additional layer of highly conformal metal organic CVD (MOCVD) Cu to ensure continuous coverage and achieve consistent void-free bottom-up plating.

The next step in the process was electrolytic deposition using a 3-component bottom-up copper plating chemistry. In addition to seed metal coverage, the via pattern density is another important consideration for TSV plating. When the TSV pattern density is below a certain threshold (~0.1% for this chemistry), large copper nodules can form across the surface of the wafers. These nodules can complicate the removal of the Cu overburden by CMP. While most nodules form in the open areas away from the TSVs, some can also form directly over TSVs, resulting in unfilled vias. Since our pattern density was below the 0.1% threshold, we anticipated that nodules would be formed. To reduce the risk of electrical discontinuities due to unfilled TSVs, we designed redundancy, forming 3 TSVs for each wire bond pad. The redundant TSVs also helped to increase the pattern area, which likely helped to limit the density of nodules. In no instances were all three vias blocked at any wire bond pad site. Therefore, the TSV redundancy prevented any yield losses from occurring during the plating process.

The plated Cu overburden and TSV liners were removed from the wafer surface by CMP processing (Fig. 4a). Due to the starting surface topography, which resulted from the unplanarized final metal level in the ASIC fabrication, we adapted the CMP process to remove the plated overburden from the high and low step heights while also planarizing the wafer surface. This was done by co-polishing the plated metal and TEOS oxide layers after the plated Cu had started clearing from the highest areas. To ensure full metal removal and achieve a uniform surface planarity, a small amount of additional TEOS oxide was removed after the last of the metal had been visibly cleared from the lowest pattern areas. Following CMP, the Cu TSVs were exposed and the wafers underwent a 210°C stabilization anneal under a nitrogen blanket for 1 hour. This anneal profile was selected based on the thermal requirements of the subsequent wafer processes and assembly steps, and to minimize the potential for Cu diffusion through the TSV liners.

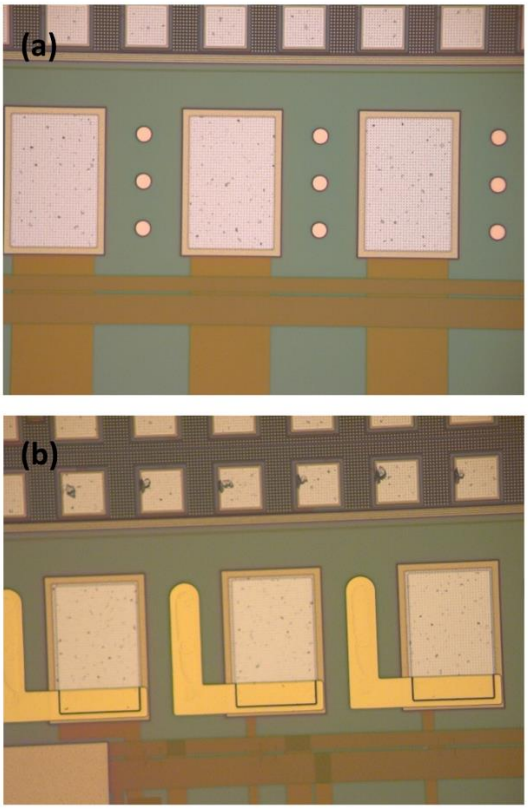

Fig. 4. (a) TSVs after CMP to remove Cu overburden (b) Ni/Au plated RDL connecting TSVs to existing Al bond pads

At this point, the Al bond pads remained passivated by the TEOS oxide layer. These Al pads were re-opened using photolithography and ICP oxide etching. Finally, Ni/Au redistribution lines (RDL) were patterned and plated to electrically connect each set of 3 TSVs to their corresponding Al bond pad as shown in Fig. 4b.

B. Temporary Bonding, Thinning, and Backside Metallization

Following the completion of frontside process levels, the ASIC wafers proceeded through the temporary bonding and thinning steps. A glass carrier wafer was bonded to the frontside of each device wafer using a laser-releasable bonding material. The ASIC wafers were thinned by back-grinding and CMP to

the target wafer thickness, stopping ~5-10 μm before the exposure of the TSVs.

The wafers were dry etched in an SF_6 plasma to remove the several microns of field silicon necessary to reveal the TSVs. Prior to etching, the wafers were cleaned with solvent and oxygen plasma to minimize residues and particles that could block the silicon etch. Following the silicon etch, the TSVs protruded by ~2-5 μm above the new silicon surface. At this point in the process, the TSVs were still passivated by the TEOS oxide liner. A spin-on BCB dielectric film (DuPont-Cyclotene™) was deposited on the wafers to repassivate the exposed silicon, coating over the exposed TSVs and creating a nearly planar surface. Via openings to the TSVs were created by photolithography and dry etching of the BCB and TSV liner. Following the dry etching of backside vias, the TSVs were open and ready for subsequent interconnection.

Fig. 5 shows optical inspection images relating to the remaining backside process steps. The RDL metal was formed through electroplating of Cu lines connecting to the exposed TSVs (Fig. 5a). A second layer of BCB was deposited and photopatterned to open via connections down to the Cu RDL. Over these openings, a Ni/Au under bump metallization (UBM) layer was formed by electroplating (Fig. 5b). The Ni/Au UBM served as connection points for solder balls to be deposited for the later assembly to the board (Fig. 5c). However, addition of the solder balls while the wafers were still on carriers was not possible because their presence would interfere with the debonding process. The wafers were returned to the bonding vendor for laser release of the glass carriers and the ASICs were returned to Micross on UV-release tape with the original frontside exposed.

Fig. 6 shows a TSV cross-section of a device die after all backside processing and singulation. Fig. 6a shows the full profile with straight, smooth sidewalls and void-free fill. Fig. 6b shows the via top through the foundry oxide and making good connection to the plated Ni/Au pad. Fig. 6c shows the TSV bottom overcoated in BCB, with a via of ~4 μm depth connecting the Cu TSV to the backside Cu RDL. The RDL is overcoated with a second 5 μm BCB layer, with vias connecting to the UBM metal (not shown in the image).

C. Backside Ball-drop of Thinned Wafers

For the reasons described previously, the solder bumps had to be placed after debonding of the ASIC wafers from the carrier. In industry, there are production processes and equipment established for the bumping and handling of thinned wafers. In the current demonstration, manual handling of the thinned wafers was required for the bumping process. Following debonding, the wafers were partially diced to prevent propagation of some edge cracks observed after the thinning process and other backside process steps. The bumping process was performed on the remaining wafer sections, which were carefully removed from the UV tape and mounted frontside down to a carrier using Kapton® tape. This exposed the backside Ni/Au pads for solder bump placement using a ball drop/stencil process. The wafers went through the flux application, solder ball drop, and reflow while still on the carriers. Yield was high after ball drop, with only occasional missing bumps. These were rectified by manually placing solder balls on missed Ni/Au pads. Many of the applied bumps function only as mechanical bumps for uniform support of the ASIC in the board assembly. Only those bumps connecting to TSVs through the RDL metal lines were electrically active. Following reflow, the wafer sections were removed from the carriers and rinsed with hot deionized water and isopropanol to remove the flux and any surface particles. Finally, the wafers were mounted face-down on dicing tape and diced from the backside.

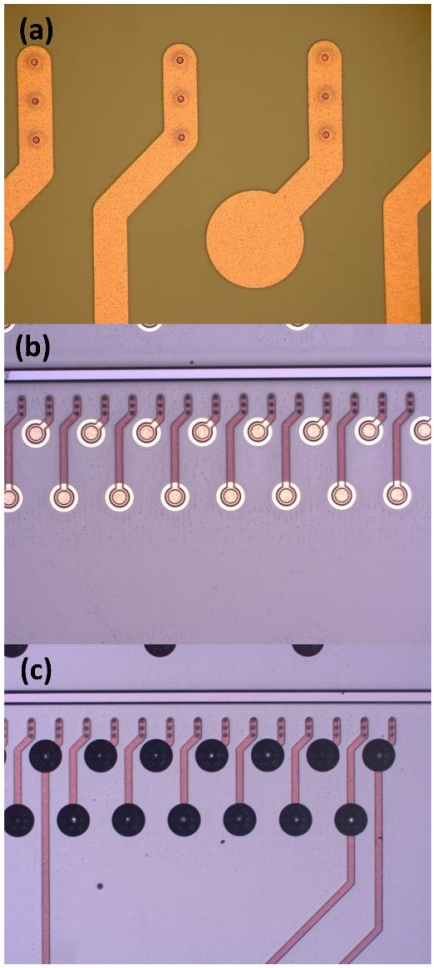

Fig. 5. Backside process levels: (a) Plated Cu RDL on top of the first BCB passivation, which is open to the three TSVs below, (b) Ni/Au UBM plated over a second BCB passivation, which is open to the Cu RDL below. (c) The solder balls on the Ni/Au UBM. (a) and (b) were completed while the wafers were still on carriers and (c) was completed while the thinned wafers were on tape.

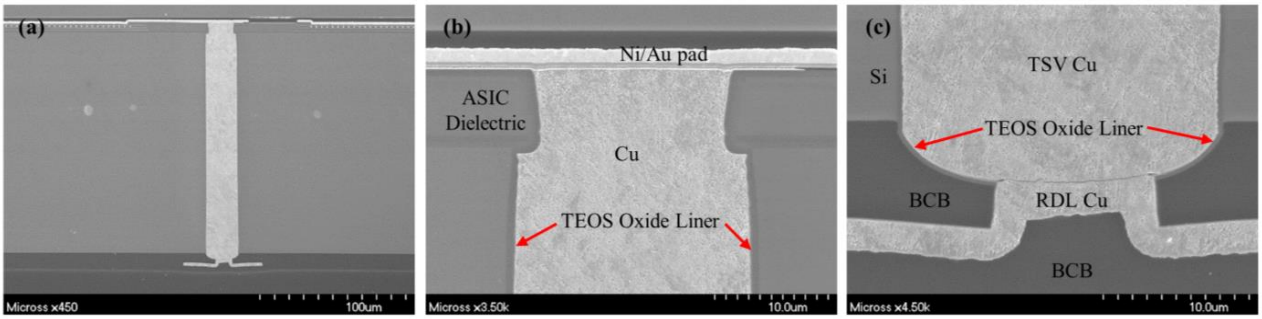

Fig. 6. Cross-sections of the final ASIC. (a) Full profile of the TSV connecting the frontside Al I/O pad to the backside Ni/Au UBM. (b) High magnification image of TSV top showing good contact between the Cu TSV and frontside Ni/Au pad. (c) High magnification image of TSV bottom showing good connection between the Cu TSV and backside Cu RDL through the etched BCB via.

V. ELECTRICAL TESTING

We designed test structures to monitor the functionality and electrical characteristics of the TSVs and placed these in open areas near the edges of the chips. These structures, shown from the back wafer surface in Fig. 7, include TSV daisy chains and isolation test structures, fabricated as a product of the TSV formation, frontside Ni/Au electrodes, backside Cu RDL, and backside Ni/Au UBM (serving as probe pads). The daisy chains (labeled "DC" in the image) allowed for the probing between 28 TSVs connected in series. These structures provided an indication of TSV yield and resistance, while also verifying adequate contact interfaces between the TSVs and the subsequent metallization layers on the front and back of the wafers. Isolation structures (labeled "ISO") were designed to confirm electrical isolation between two groups of 4 vias each, separated by a 30 µm gap. The ISO structures are primarily intended to characterize the TSV insulator layer, in this case PECVD TEOS oxide. Measurements of these structures can include DC resistance and I-V characteristics, including leakage current and breakdown voltage.

Measured at a fixed test current of 100 mA, all daisy chains showed resistance values of less than 15 Ω. This indicates an average resistance of ≤0.5 Ω for each of the 28 TSV links. That includes the TSV resistance, top and bottom metal traces, and contact interfaces. These results were consistent from wafer to wafer and at all locations measured. No tested die exhibited discontinuity or high resistance in the daisy chain structures. This suggests all TSVs in the test structures were sufficiently filled with Cu, properly revealed on the backside of the thinned wafer, and in good contact with the subsequent metallization layers. These observations are consistent with the information we observed in the SEM cross-section images.

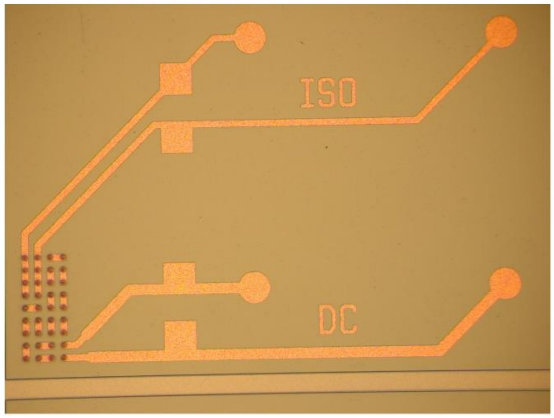

Fig. 7. TSV test structures. Daisy chains ("DC") contain 28 TSVs. Isolation structures ("ISO") contain 4 TSVs per probe line.

The power requirement of the mixed signal ASIC chip is 5V. Therefore, the TSVs should be sufficiently isolated up to 5V to avoid cross talk or shorting (between power and ground TSVs, or from TSVs to the device circuitry). We performed 2-wire I-V tests from 0 to 5V. Results were mixed across the wafers. In some cases, the current draw was below the level of detection of our 2-point probe, even at 5V. Some of those die were held at 5V for up to 10 minutes with current draw staying low (<1 µA) or increasing to <100 µA. In some instances, elevated leakage was observed at lower voltages. Fig. 8. shows representative I-V sweeps for such instances. The compliance was set to 105 µA for these measurements. These die typically reached compliance at 3-5 V. However, for some die, the compliance was met at lower voltages (1-2V). The discrepancy between die did not correlate with specific wafers or with locations on the wafers (i.e. center versus edge effects).

The TSV isolation results, including elevated leakage currents, are inconsistent with previous TSV-last process demonstrations by Micross. In earlier projects, we have inserted similar 20 x 150 µm TSVs into both silicon test wafers and foundry device wafers. Test structures in these projects showed good isolation between groups of TSVs, often well above 5V. We are in the process of further analyzing the current project results and troubleshooting through additional experimental work. One difference between the prior projects and the current TSV integration effort is the starting silicon wafers. The ON Semiconductor C5N ASIC wafers for this work were fabricated on low-resistivity P+ silicon (≤0.02 Ω-cm), whereas our test grade wafers and the foundry device wafers in other projects used higher resistivity silicon, such as 1-10 Ω-cm and above. At a minimum, this may lower the series resistance of the silicon conduction path between TSVs, which could yield

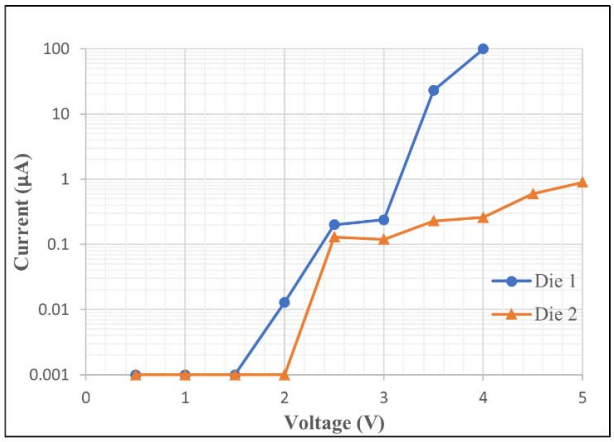

Fig. 8. Representative I-V sweeps of die that showed elevated leakage before reaching the 5V target.

higher leakage currents at a given voltage if, in fact, there is a leakage path through the TEOS oxide insulator lining the TSVs. We are actively looking into possible contributors to the elevated leakage, relating to insufficient insulation by the TSV dielectric liner or the potential for any surface conduction paths across the top of the chips between TSVs and/or pads.

The functionality of the ASIC die were tested before and after TSV insertion at Harvard University and/or Caltech. Using a probe card, the die were powered on at 5V and circuit outputs were monitored. Prior to TSV insertion, the die functioned normally. After TSV insertion, the die typically performed in two different fashions: a few die were seen to short out at 5V as soon as they were powered up, but in many cases, the die initially functioned at 5V, then showed an increase in leakage over time until the circuit failed to respond. It should be noted that for the isolation test structures measured at Micross, there were some die that exhibited stable behavior at 5V for long periods of time, which is somewhat contradictory to the ASIC testing results. As stated previously, work is ongoing to troubleshoot and resolve this problem.

VI. Conclusions

In this work, we have demonstrated the full process flow related to a TSV-based packaging approach for CZT X-ray detectors and their ASIC readout chips. Specifically, we performed a frontside, TSV-last fabrication by post-processing completed ASICs from an existing design. The TSVs were connected to the ASIC I/O pads on the front, the wafers were thinned, and backside processing provided RDL and a UBM layer for solder bump connections to the board. Solder bump placement on the back of the thinned ASICs was also demonstrated. Wafer inspections and cross-sectional SEM analysis indicated successful completion of the primary process steps (via etch, line, fill, CMP, thinning, and front/back metallizations). Electrical testing of TSV daisy chains indicated consistent Cu TSV plating yield with low resistance contacts made to subsequent metal levels on the front and back of the ASIC. The assembly operations required for the CZT-ASIC and ASIC-board attachments were demonstrated using thinned mechanical silicon chips with frontside metallization and backside UBM/bumps.

However, a full X-ray detector demonstration including CZT hybridization, ASIC-board assembly, and detector testing could not be completed due to some observed concerns with the ASIC's electrical functionality after TSV formation and other post-processing steps. The ASIC chips showed signs of high current draw and were often unstable, degrading with time when powered at 5V. Measurement of Micross TSV test structures also showed elevated leakage currents below 5V in some chips. The TSV isolation concerns seen here were inconsistent with results of similar TSV demonstrations in prior Micross projects involving different device technologies and applications. We are actively analyzing these results and troubleshooting efforts are underway to identify possible root causes and solutions, ahead of a future possible X-ray detector demonstration with TSV-based packaging. If and when a successful demonstration is achieved, we anticipate that to be the focus of a follow-on publication.

Acknowledgment

This work was supported with funding from NASA APRA grant NNX17AE62G. The authors wish to thank additional Micross technical staff members who supported the wafer processing and SEM characterization, in particular Pedro Colón and Dana Fox. We would also like to acknowledge Syagrus Systems for temporary bonding/thinning/debonding support, Entrepix for CMP processing, and Hionix for ionized PVD support.

References

[1] R. Beica, "3D integration: applications and market trends," in *International 3D Systems Integration Conference (3DIC)*, Sendai, Japan, 2015.

[2] E. Beyne, "The 3-D Interconnect Technology Landscape," *IEEE Design & Test,* vol. 33, no. 3, pp. 8-20, 2016.

[3] Handbook of 3D Integration, Volume 3: 3D Process Technology Edited by: P. Garrou, M. Koyanagi and P. Ramm, Weinheim, Germany: Wiley-VCH, 2014.

[4] D. S. Temple, D. Malta, E. P. Vick, M. R. Lueck, S. H. Goodwin, M. S. Muzilla, C. M. Masterjohn and M. R. Skokan, "Advanced 3D mixed-signal processor for infrared focal plane arrays: fabrication and test," in *International 3D Systems Integration Conference (3DIC)*, Kinsdale, Ireland, 2014.

[5] D. Malta, E. Vick, M. Lueck, A. Huffman, S. Woodruff, P. Ralston, J. Hartman, N. Bushyager, G. D. Ebner, S. Quade, A. Young, C. Hillman and J. Hacker, "TSV-Last, heterogeneous 3D integration of a SiGe BiCMOS beamformer and patch antenna for a W-band phased array radar," in *IEEE 66th Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, 2016.

[6] F. A. Harrison, W. W. Craig, F. E. Christensen, C. J. Hailey, W. W. Zhang, S. E. Boggs, D. Stern, W. R. Cook, K. Forster and P. Giommi, "The Nuclear Spectroscopic Telescope Array (NuSTAR) High-Energy X-Ray Mission," *The Astrophysical Journal,* vol. 770, p. 103, 2013.

[7] J. Hong, J. Grindlay, B. Allen, D. P. Violette, H. Miyasaka, D. Malta, J. Ovental, D. Bordelon and D. Richter, "Proof of Concept for Through Silicon Vias (TSVs) in Application Specific Integrated Circuits (ASICs) for Hard X-Ray Detectors," *Journal of Astronomical Telescopes, Instruments, and Systems (JATIS),* in press., 2021.

[8] H. Jun, J. Cho, K. Lee, H.-Y. Son, K. Kim, H. Jin and K. Kim, "HBM (High Bandwidth Memory) DRAM technology and architecture," in *IEEE International Memory Workshop (IMW)*, Montery, CA, 2017.

[9] B. Banijamali, S. Ramalingam, K. Nagarajan and R. Chaware, "Advanced reliability study of TSV interposers and interconnects for the 28nm technology FPGA," in *IEEE 61st Electronic Components and Technology Conference (ECTC)*, Lake Buena Vista, FL, 2011.

[10] D. Malta, C. Gregory, M. Lueck, D. Temple, M. Krause, F. Altmann, M. Petzold, M. Weatherspoon and J. Miller, "Characterization of thermo-mechanical stress and reliability issues for Cu-filled TSVs," in *IEEE 61st Electronic Components and Technology Conference (ECTC)*, Lake Buena Vista, FL, 2011.

[11] F. A. Harrison, W. R. Cook, H. Miyasaka and R. McLean, "Cadmium Zinc Telluride Pixel Detectors for Hard X-Ray Astrophysics," in *Semiconductor Radiation Detection Systems*, Boca Raton, FL, CRC Press, 2010.