

# A 2.4-GHz, 2.2-W, 2-V Fully-Integrated CMOS Circular-Geometry Active-Transformer Power Amplifier

Ichiro Aoki, Scott D. Kee, David Rutledge, and Ali Hajimiri  
Department of Electrical Engineering, California Institute of Technology, Pasadena, CA 91125, USA

## Abstract

A 2.4-GHz, 2.2-W, 2-V fully integrated circular geometry power amplifier with  $50\Omega$  input and output matching is fabricated using 2.5V,  $0.35\mu\text{m}$  CMOS transistors. It can also produce 450mW using a 1V supply. Harmonic suppression is 64dB or better. An on-chip circular-geometry active-transformer is used to combine several push-pull low-voltage amplifiers efficiently to produce a larger output power while maintaining a  $50\Omega$  match. This new on-chip power combining and impedance matching method uses virtual ac grounds and magnetic couplings extensively to eliminate the need for any off-chip component such as wirebonds. It also desensitizes the operation of the amplifier to the inductance of bonding wires and makes the design more reproducible. This new topology makes possible a fully-integrated 2.2W, 2.4GHz, low voltage CMOS power amplifier for the first time.

## Introduction

The design of a power amplifier with a reasonable power level, efficiency and gain remains one of the major challenges in today's pursuit of a single-chip integrated transceiver. Although several advances have been made in this direction, a truly integrated CMOS power amplifier has not been reported to this date.

Multiple external components such as bonding wires and external baluns have been used as tuned elements to produce output power levels in excess of 1-W using CMOS [1,2] or Si-Bipolar transistors [3,4]. Alternative technologies with higher breakdown voltage devices and higher substrate resistivity have been used to increase the output power and efficiency of integrated amplifiers. In particular, LDMOS transistors with a breakdown voltage of 20V [5] and GaAs MESFETs on insulating substrate [6] have been used to integrate power amplifiers.

Two main problems in a fully-integrated CMOS power amplifier are the low breakdown voltage of the drain and the low resistivity of the substrate which increases the loss of on-chip inductors and transformers. These problems are exacerbated as CMOS transistor's minimum feature size is scaled down for faster operation.

The low breakdown voltage of CMOS transistors will limit the maximum allowable drain voltage swing of the transistor making it necessary to perform some form of impedance transformation to achieve a larger output power. For example, a  $\pm 2\text{V}$  drain voltage swing delivers only 40mW to

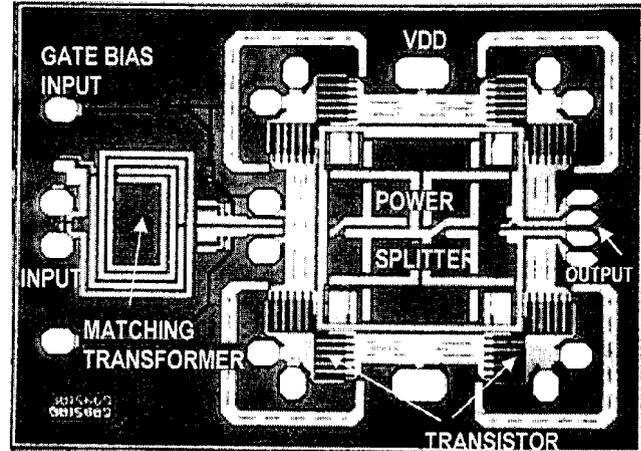


Figure 1- Microphotograph of 2.4GHz-2.2W fully integrated circular geometry active transformer power amplifier, chip size: 1.3 mm x 2.0 mm

a  $50\Omega$  load if no such impedance transformation is performed. This impedance transformation can be achieved using an ideal  $1:n$  transformer. Unfortunately, an on-chip spiral  $1:n$  transformer on a standard CMOS substrate is very lossy and will degrade the performance of the amplifier greatly [7,8].

This paper describes a *novel circular-geometry active-transformer power amplifier* as a means for power combining and impedance transformation to achieve a high output power and to overcome the low breakdown voltage of short-channel MOS transistors. Fig. 1 shows the microphotograph of the fabricated amplifier. This new circular geometry can be used to implement both linear and switching power amplifiers. It allows efficient drain harmonic control to combine multiple class-E/ $F_3$  amplifiers. Class-E/ $F_3$  is a member of the new family of  $E/F_n$  switching amplifiers [9], whose basic principle of operation was recently demonstrated by a 1.1kW, 85% PAE *discrete* power amplifier at 7MHz using two power MOSFETs [9].

## Circular Geometry Power Amplifier

This section describes the design evolution leading to the circular-geometry active-transformer power amplifier shown in Fig. 1.

### A) Push-Pull Driver

Fig. 2 shows the basic push-pull amplifier, which is used as the main building block for the circular-geometry active-transformer power amplifier. This topology creates a virtual

ac ground at the supply node for the fundamental frequency and all the odd harmonics of the drain voltage, as shown in Fig. 2. This virtual ground is an important feature of the push-pull driver, making it unnecessary to use a choke inductor and/or a large on-chip bypass capacitor at supply.

### B) Quad-Push-Pull Circular Geometry

The circular geometry comprises of four push-pull amplifiers, each forming one side of a square as shown in Fig. 3. This strategic positioning of the four push-pull amplifiers allow us to use a straight and wide metal line as the drain inductor. A slab inductor exhibits a higher quality factor,  $Q$  (~20 to 30) than a spiral inductor (5 to 10) and hence will lower the losses in the passive network. The slab inductors also provide natural low resistance paths for the dc current to flow from the supply to the drain of the transistors, as shown in Fig. 3.

By driving the two adjacent transistors of two different push-pull amplifiers in opposite phases, we can create a virtual ac ground in each corner of the square. This is an essential feature of the circular geometry, as the fundamental and odd harmonics of the signal will not leave the loop made of the four metal slabs as shown in Fig. 3. Thus, any connection from this square to the supply voltage or ground *will not* carry any ac signals at the fundamental frequency or its odd harmonics. This practically limits the loss in the supply connection to dc ohmic loss of the connecting line, which can be easily minimized using wider metal line. It is noteworthy that the topology of Fig. 3 does not form a virtual ground at the supply and ground nodes for the even harmonics. Thus, the transistors see relatively high impedance at the even harmonics compared to the fundamental and the odd harmonics.

### C) Harmonic Control

Controlling the harmonic content of the signal inside the amplifier plays a major role in the performance of a switching amplifier. This can be achieved by connecting four capacitors between the drains of the adjacent transistors in each corner of the square, as depicted in Fig. 4. The capacitors will only affect fundamental and odd harmonics since the even harmonic voltages are equal in magnitude and phase on both terminals of the capacitors. Thus, these capacitors are used to obtain the desired inductive impedance at the fundamental frequency, and provide very low impedances at odd harmonics, while maintaining high impedance for even harmonics. This selective impedance control allows each push-pull amplifier to be driven as a power efficient switching amplifier operating in class-E/ $F_3$  [9]. This topology can be used as a linear class-A amplifier by omitting the corner capacitors and adjusting the drain inductance to resonate the transistor drain-to-bulk capacitors.

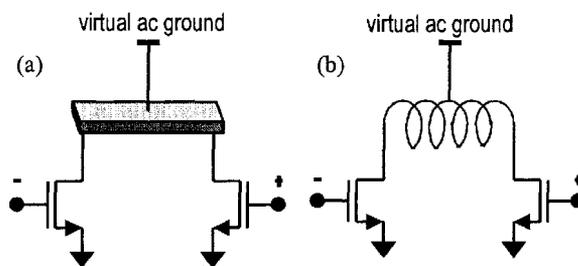


Figure 2- Push-pull amplifiers: (a) using a metal line as drain inductors; (b) equivalent circuit

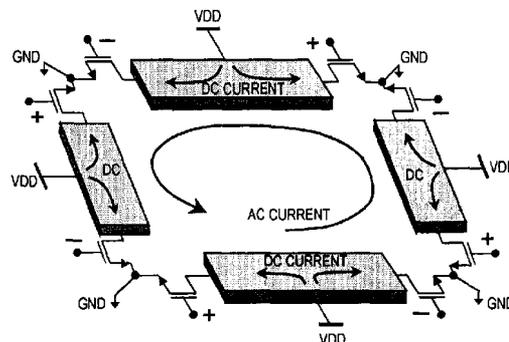


Figure 3- Four Push-pull amplifiers in circular geometry

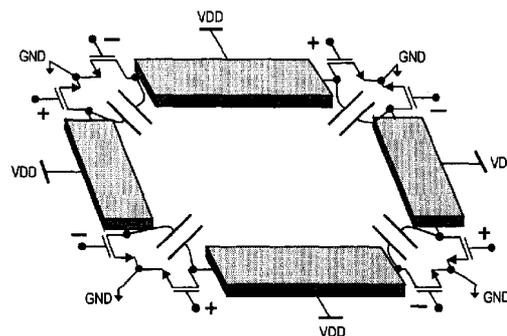


Figure 4- Four Push-pull amplifiers in circular geometry with four harmonic control capacitors

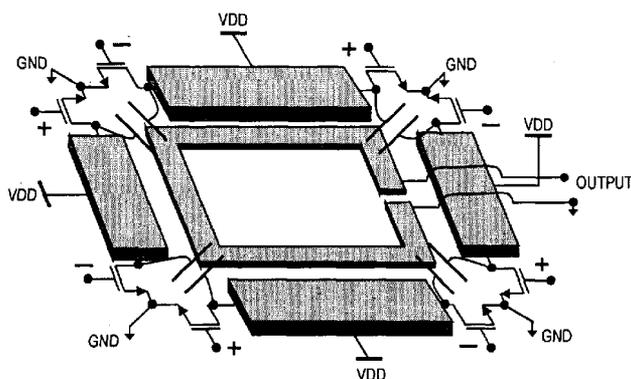


Figure 5- Four Push-pull amplifiers in circular geometry with secondary coil connected to output

#### D) Output Power Combining

The square geometry is used as the primary circuit of a magnetically coupled transformer to combine the output power of these four push-pull amplifiers and match their small drain impedance to a  $50\Omega$  unbalanced load. The ability to drive an unbalanced load is essential to avoid an external balun for driving commonly used single-ended antennas. These four push-pull amplifiers driven by alternating phases generate a uniform circular current at the fundamental frequency around the square resulting in a strong magnetic flux through the square. A one-turn metal coil inside the square can be used to harness this alternating magnetic flux and act as the transformer secondary loop, as shown in Fig. 5. It also provides an impedance transformation ratio of 8:1 to present impedance of  $6.25\Omega$  to the drain. Ignoring the losses, this transformation and combining process raises the potential output power of the amplifier from  $40\text{mW}$  to  $2.56\text{W}$  for a  $\pm 2\text{V}$  drain voltage swing in the linear mode of operation. As the transformer-coupling factor,  $k$ , is lower than 1 (typically around  $k=0.6-0.8$ ) a capacitor has to be connected in parallel to the output to compensate the leakage inductance of the transformer.

The even harmonics are not coupled to the secondary due to the symmetry of the push-pull topology, and thus are rejected significantly. Also the transistor drain to bulk capacitance and the corner capacitors will practically short-circuit all odd harmonics except the fundamental frequency signal, thus attenuating odd harmonics at the output.

Unlike other amplifier classes (e.g., class F) that require individual adjustments for each harmonic, this circular-geometry active-transformer topology only requires adjustment at the fundamental frequency during the design process. Once the fundamental frequency is set, all other harmonics will see the desired impedances automatically.

#### E) Input Power Splitting and Matching

A  $50\Omega$  unbalanced input has to be matched and transformed into four balanced drive signals at the gates, resulting in similar challenges as the output network. Four inductive loops are connected between the gates at each corner to resonate the gate capacitance at the fundamental frequency, as shown in Fig 6. The single loop inductor exhibits better  $Q$  (10-15) than normal spiral inductors. The middle point of these inductive loops form virtual ac grounds that make it unnecessary to use a large capacitor to block the dc voltage.

The input power splitting network consists of three parts, namely, the input spiral transformer balun, the connecting differential lines bringing the balanced signal to the center of the square, and the splitting network symmetrically connecting the center point to the gates of each transistors. The splitting network provides in-phase balanced input signals to the gates of each push-pull pair transistors. The splitting network metal lines are twisted in order to provide magnetic coupling from the output transformer to enhance

the gain of the amplifier. A parallel capacitor is necessary at the input to resonate the leakage inductance and provide matching to  $50\Omega$  at the input side of the spiral 1:1 on-chip balun. It is very important to notice that none of the bonding wires are used as inductors making it unnecessary to fine tune their value for optimum operation.

### Experimental Results

As a demonstration of the concept, a 2.2-W, 2.4-GHz single-stage fully-integrated circular-geometry switching power amplifier in class E/ $F_3$  was fabricated and measured using  $0.35\mu\text{m}$  CMOS transistors in a BiCMOS process technology. This process offers three metal layers, the top one being  $3\mu\text{m}$  thick with a distance of  $4.3\mu\text{m}$  from the substrate, the substrate has a resistivity of  $8\Omega\cdot\text{cm}$ . The chip area is  $1.3\text{mm} \times 2.0\text{mm}$  including pads. The complete electrical diagram of the designed circuit can be seen in Fig. 7. Quasi-3D simulation using SONNET and ADS is performed on the complete structure as a part of the design cycle to verify performance of the amplifier.

In our measurement, the chip is glued directly to a gold plated brass heat sink using conductive adhesive to allow enough thermal dissipation. The chip ground pads are wire bonded to the heat sink. The input and output are wire bonded to  $50\Omega$  microstrip lines on printed circuit board (PCB). Supply and gate bias pads are also wire bonded. The input is driven using a commercial power amplifier connected to the circuit input through a directional coupler

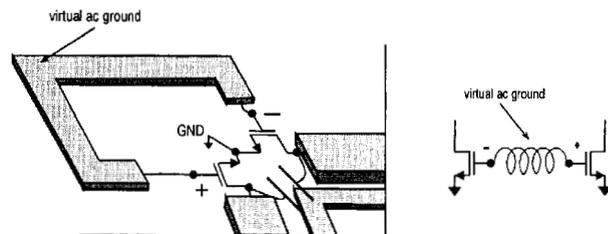


Figure 6- Gate matching "L" shape inductor (a) geometry, (b) equivalent circuit.

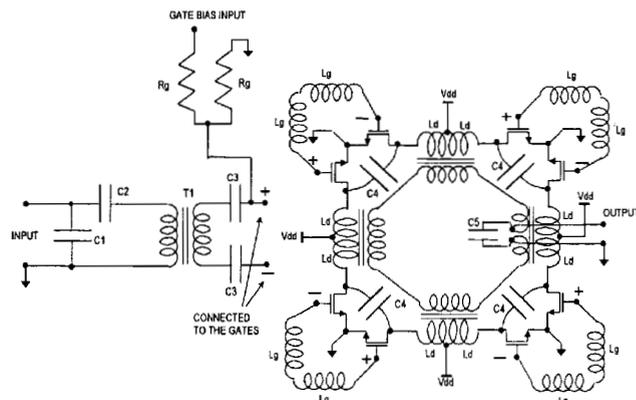


Figure 7- Electrical diagram of circular geometry power amplifier.

to measure the input return loss. The output is connected to a power meter through a 20dB attenuator and 2.9GHz low pass filter to avoid measuring harmonic signal powers. All system power losses are calibrated out, including the connector and Duroid board losses. The bond wire power loss is included in the amplifier's measured performance.

An output power of 2.2W at 2.4GHz is obtained with 8.5 dB gain using a 2V power supply. The corresponding power added efficiency (PAE) is 31% and drain efficiency is 36%. If the output is taken differentially, a PAE of 41% is achieved with  $P_{out}$  of 1.9W, gain of 8.7dB and drain efficiency of 48%. Figures 8 and 9 show the gain and PAE vs. output power for 2V and 1V supplies, respectively. Small signal gain is 14dB and input reflection coefficient is  $-9$ dB. The 3dB bandwidth is 510MHz centered at 2.44GHz. All harmonics up to 20GHz were more than 64dB below the fundamental.

### Conclusion

A new method for implementation of a power amplifier in a low voltage CMOS process was presented. A novel *fully-integrated single-stage circular geometry active transformer power amplifier* implemented in a low voltage CMOS process achieves 2.2W output power with 31% PAE at 2.4GHz. It can also be used as a 450mW, 1V, 2.4GHz amplifier with 27% PAE. The circuit includes input and output matching to 50Ω, requiring no external components. This new concept combines several push-pull amplifiers efficiently with an extensive use of virtual ac grounds and magnetic couplings. None of the bonding wires are used as signal path inductors making the circuit insensitive to their exact value. This is the first reported *true* fully-integrated power amplifier using a low voltage CMOS process achieving 2.2W at 2.4GHz, as can be seen in the following Table, summarizing the previous work.

Freq GHz	$P_{out}$ W	Sup V	PAE %	Wirebond Inductor	External Comp.	Active Device	Ref.
1.9	1.0	2	41	YES	YES	CMOS	[1]
0.9	1.0	1.9	41	YES	YES	CMOS	[2]
0.9	5.0	4.5	59	NO	YES	Si Bipolar	[3]
1.9	1.4	2.5	55	NO	YES	Si Bipolar	[4]
0.9	0.2	5	49	NO	NO	SOI LDMOS	[5]
2.4	0.25	7	79	NO	NO	MESFET	[6]
2.4	0.45	1	27 (36 Diff.)	NO	NO	CMOS	this
2.4	2.2	2	31 (41 Diff.)	NO	NO	CMOS	PA

### Acknowledgments

The authors thank Conexant Systems for chip fabrication, particularly R. Magoon, F. In'tveld, J. Powell, A. Vo, and K. Moye. We also acknowledge Intel corp., Army research office, JPL, Infineon, and NSF for support of this project. K. Potter, D. Ham, and H. Wu of Caltech, deserve special thanks for their assistance. The technical support for CAD tools from Agilent Technologies and SONNET Software, Inc. are also appreciated.

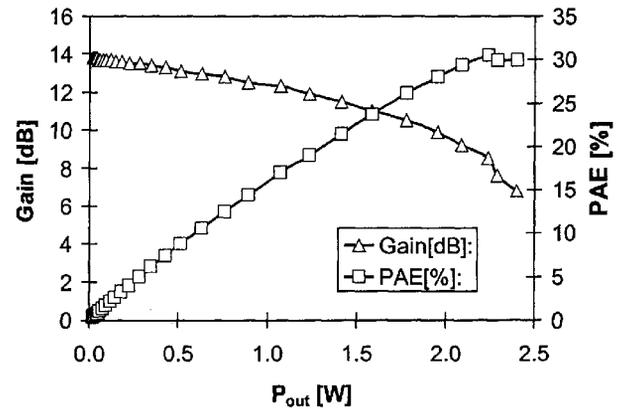


Figure 8- Output Power vs. Gain and PAE with 2V Supply

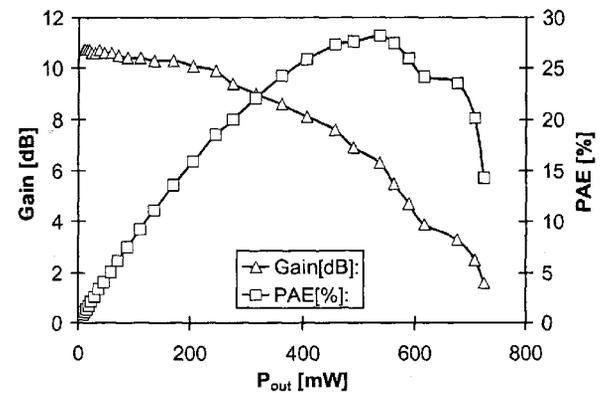


Figure 9- Output Power vs. Gain and PAE with 1V Supply

### References

- [1] K. C. Tsai and P. R. Gray, "A 1.9 GHz, 1-W CMOS Class-E Power Amplifier for Wireless Communications," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 7, pp. 962-969, July 1999.
- [2] C. Yoo and Q. Huang, "A Common-Gate Switched, 0.9W Class-E Power Amplifier with 41% PAE in 0.25μm CMOS," *Symposium on VLSI Circuits Digest*, pp. 56-57, Honolulu, June 2000.
- [3] W. Simbürger, *et al*, "A Monolithic Transformer Coupled 5-W Silicon Power Amplifier with 59% PAE at 0.9 GHz," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 12, pp. 1881-1892, Dec. 1999.
- [4] W. Simbürger, *et al*, "A Monolithic 2.5V, 1W Silicon Bipolar Power Amplifier with 55% PAE at 1.9GHz," *IEEE MTT-S Digest*, vol. 2, pp. 853-856, Boston, June 2000.
- [5] Y. Tan, *et al*, "A 900-MHz Fully Integrated SOI Power Amplifier for Single-Chip Wireless Transceiver Applications," *IEEE Solid-State Circ.*, vol. 35, no. 10, pp. 1481-1485, Oct. 2000.
- [6] J. Portilla, H. Garcia, and E. Artal, "High Power-Added Efficiency MMIC Amplifier for 2.4 GHz Wireless Communications," *IEEE Journal of Solid State Circuits*, vol. 34, no. 1, pp. 120-123, Jan. 1999.
- [7] J. R. Long and M. A. Copeland, "The Modeling, Characterization, and Design of Monolithic Inductors for Silicon RF IC's," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 3, pp. 357-369, March 1997.
- [8] J. R. Long, "Monolithic Transformers for Silicon RF IC Design," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 9, pp. 1368-1382, Sept. 2000.
- [9] S. D. Kee, I. Aoki, and D. Rutledge "7-MHz, 1.1-kW Demonstration of the New E/F<sub>odd</sub> Switching Amplifier Class," submitted to *IEEE MTT-S*, Phoenix, June 2001.