17.2 A CMOS Differential Noise-Shifting Colpitts VCO

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Demand for higher numbers of communication channels imposes tighter phase noise performance for the local oscillators. Cross-coupled oscillators are widely used due to ease of implementation and differential operation (Figure 17.2.1a) [1,2,3]. Unfortunately, in cross-coupled VCOs the maximum noise generation instant coincides with maximum phase noise sensitivity and hence the cross-coupled VCOs do not use the full potential of the resonator [3]. This oscillator topology achieves improved phase noise for a given quality factor and bias current by alternating the bias current and aligning the maximum noise with the least sensitive time in the cycle.

The phase noise of an oscillator is given by [4]:

$$L\{f_{off}\} = \frac{\bar{i}_n^2/\Delta f}{8\pi^2 f_{off}^2} \cdot \frac{\Gamma_{rms}^2}{q_{max}^2} \quad (1)$$

where f_{off} is the offset frequency from the carrier, q_{max} is the maximum signal charge swing, $i_n^2/\Delta f$ is the power spectral density of the parallel current noise, and Γ_{rms}^2 is the rms value of the *effective* impulse sensitivity function (ISF) [4]. ISF is defined as:

$$\Gamma_{eff}(wt) = \Gamma(wt) \bullet \alpha(wt) \quad (2)$$

where Γ is the impulse sensitivity function (ISF) representing the time varying sensitivity of the oscillator phase to perturbations and α is the noise modulating function (NMF) that is a deterministic periodic function representing the modulation of the noise [4].

Figure 17.2.1. shows a standard cross-coupled oscillator together with the ISF, NMF and the effective ISF of its pMOS transistors. The waveforms for the nMOS transistors are similar. The noise generated from the pMOS (and nMOS) transistors reaches its maximum when the oscillator is sensitive to perturbations and hence results in a lower phase noise for a given resonator Q and bias current.

Alternatively, the Colpitts oscillator of Figure 17.2.2 has good cyclostationary noise properties [4]. Figure 17.2.2 shows the ISF, NMF and effective ISF of the active device noise, confirming this effect. For this topology, the noise generated by the core transistor is maximum when the oscillator is least sensitive to perturbations and can potentially achieve lower phase noise.

In addition to better cyclostationary noise properties, the Colpitts topology achieves a higher voltage swing for a given bias current and resonator Q compared to the cross-coupled oscillators. For tail bias current, I_{bias}, and an effective parallel tank resistance, R_P, the nMOS-only (or pMOS-only) and the complimentary cross-couple oscillator topologies have tank amplitudes of approximately, $2I_{bias}R_P/\pi$ and $4I_{bias}R_P/\pi$, respectively, while the Colpitts oscillator achieves a tank amplitude of $2I_{bias}R_P$ [2,4].

Despite these advantages, CMOS Colpitts oscillators are rarely used in integrated circuits mainly due to their higher required gain for reliable start-up and single-ended nature that makes them more sensitive to common-mode noise sources such as substrate and supply noise.

The design evolution leads to a topology that overcomes the start-up issues while providing a low-noise fully-differential output. A differential output can be provided by coupling two Colpitts oscillators by sharing the source-to-ground capacitors, C_2, between two independent Colpitts oscillators, as shown in Figure 17.2.3a. Since the center node where both C_2 are connected together is a differential virtual ground, the original behavior of operation of the Colpitts oscillators remains unchanged when the two sides oscillate 180° out of phase.

While providing differential operation, the topology of Figure 17.2.3a increases the current consumption by a factor of two. Noting that the current through the transistor of Figure 17.2.2a flows through the core transistor for less than half of the period (Figure 17.2.2b), it is possible to reuse the same current source by switching it between the two sides of the oscillator, as in Figure 17.2.3b. This switching must occur in a synchronized manner and can be achieved by using a pair of nMOS transistors to switch the current from one side to the other, as in Figure 17.2.4a. This switching action will cut down the current consumption by almost a factor of two for differential operation, which allows the oscillator to use less dc power. The oscillator takes full advantage of the cyclostationary noise shaping of the core transistors. Moreover, the negative resistance of the tail cross-coupled pair provides an effective means of guaranteeing reliable start-up.

Simulated voltage waveforms of this new topology shown in Figure 17.2.4a are presented in Figure 17.2.4b. The ISF, NMF, and effective ISF for the core transistors are shown in Figure 17.2.4c. In this configuration, the transistor channel noise is maximum when the oscillator is the least sensitive to perturbations, reducing the effective ISF considerably.

A test VCO using 0.35μm CMOS transistors is optimized using linear programming [3]. The inductance is chosen for a center frequency of 2.1GHz. The inductors have quality factors of 6. nMOS transistors operating in inversion mode are used as varactors. The channel length of the nMOS varactors is optimized to maximize the quality factor while maintaining a good tuning range. The oscillator operates from 1.8 to 2.45GHz, which corresponds to a center frequency of 2.12GHz and a tuning range of 30.5%. Figure 17.2.5 shows the tuning range and phase noise of this VCO. The oscillator shows a phase noise of -139dBc/Hz at 3MHz offset from the carrier using low Q inductors of 6, while drawing 4mA from a 2.5V supply.

To verify the effect of capacitive and LC tail current noise filtering, they have been added to the oscillator with the option to remove the inductor or capacitor through a laser trim [2,5]. The LC network resonates at twice the frequency of oscillation. Measured oscillator phase noise at 3MHz is -138.2dBc/Hz with the LC filter and -139.2dBc/Hz with the capacitor alone (inductor shorted). The LC filtering method does not have a significant effect on phase noise in this topology and actually degrades it by <1dB. Figure 17.2.6 is a chip micrograph.

References:

[1] L. Dauphinee et al., "A Balanced 1.5GHz Voltage-Controlled Oscillator with an Integrated LC Resonator", ISSCC Digest of Technical Papers, pp. 390-391, Feb. 1997.

[2] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential LC oscillators", IEEE J. of Solid State Circuits, vol. 34, pp. 717-724, May 1999.

[3] D. Ham, A. Hajimiri, "Concepts and methods in optimization of integrated LC VCOs", IEEE J. of Solid State Circuits, vol. 36, pp. 896-909, June 2001.

[4] A. Hajimiri and T. H. Lee, "The design of low noise oscillators," Norwell, MA: Kluwer, 1999.

[5] E. Hegazi et al., "A Filtering Technique to Lower Oscillator Phase Noise", ISSCC Digest of Technical Papers, pp. 364-365, Feb. 2001.

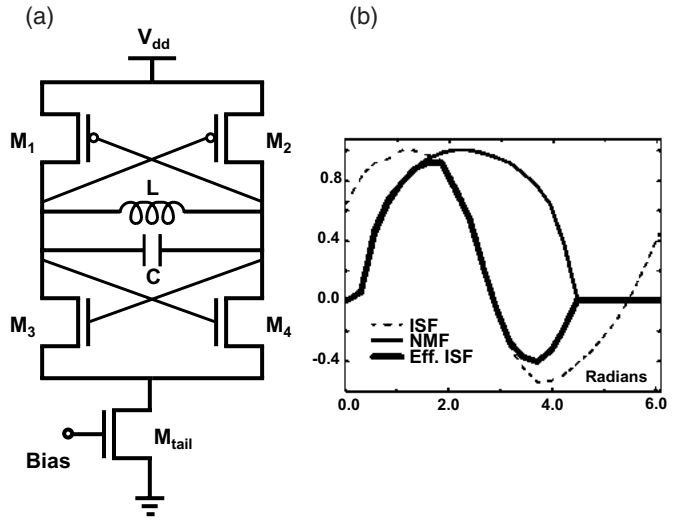

Figure 17.2.1: Cross-coupled oscillator (a) topology and (b) its ISF, NMF, and effective ISF waveforms.

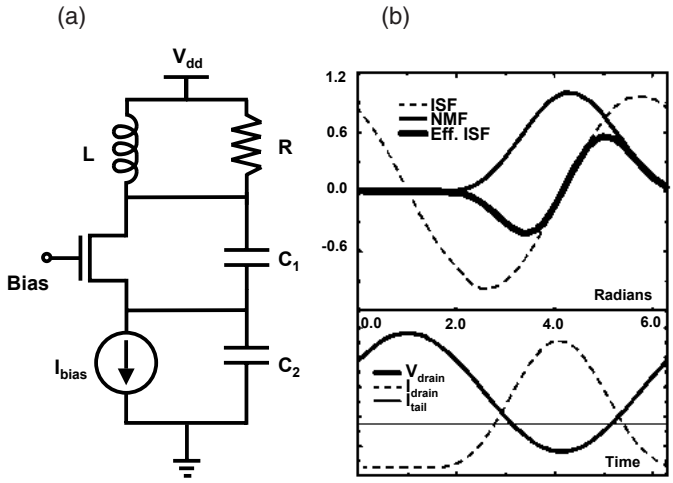

Figure 17.2.2: Single-ended Colpitts oscillator (a) topology and (b) its ISF, NFM, and effective ISF waveforms.

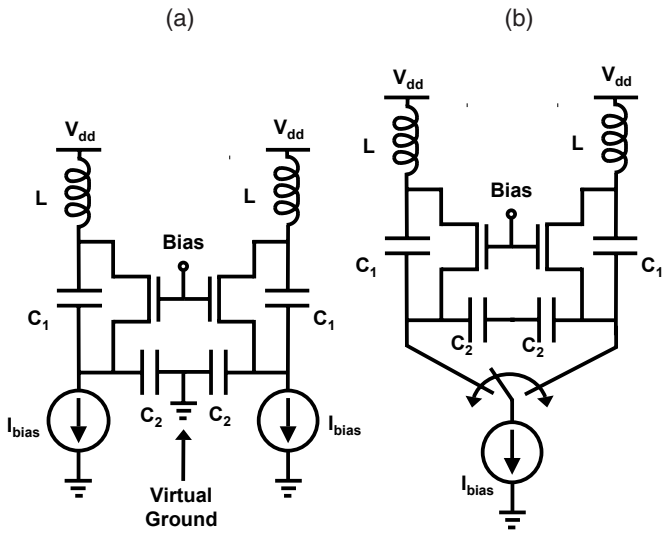

Figure 17.2.3: Differential Colpitts oscillator (a) initial topology (b) with switching current source.

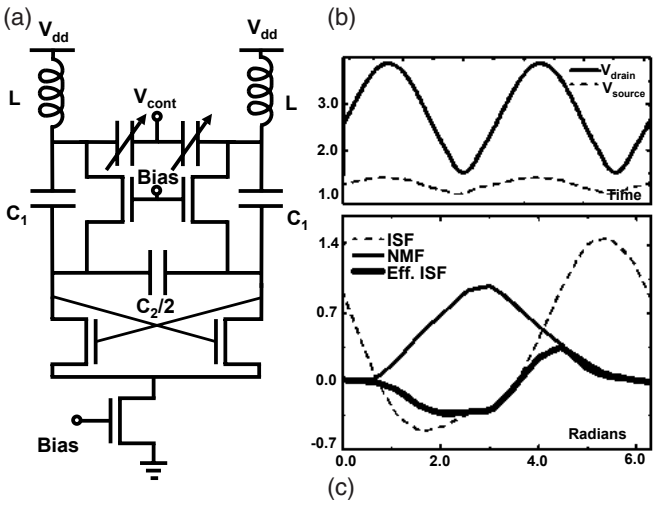

Figure 17.2.4: (a) Differential Colpitts oscillator with tail cross-coupled switch implementation (b) Voltage waveforms of the VCO with current reusing (c) ISF, NMF and effective ISF.

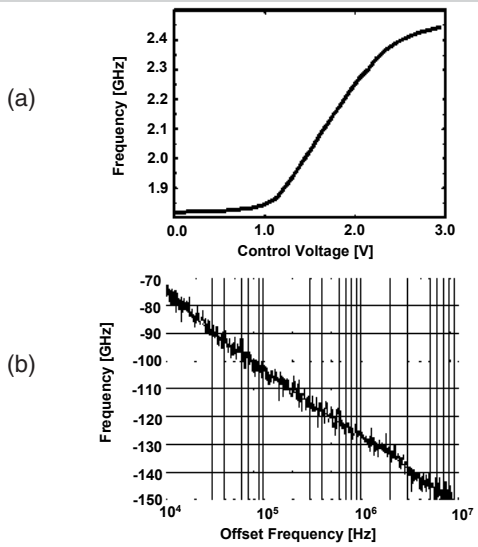

Figure 17.2.5: Measured frequency tuning range of the VCO (b) measured phase noise plot at f_{osc} = 1.8GHz.

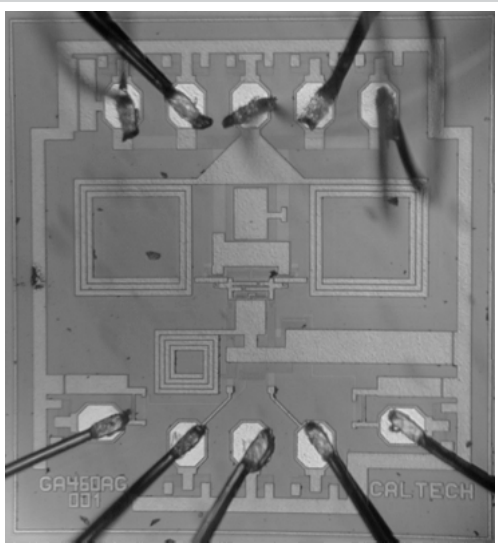

Figure 17.2.6: Die micrograph.

