21.1 Circular-Geometry Oscillators

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Demand for faster data rates in wireline and wireless markets has resulted in tighter jitter and phase noise requirements for oscillators. Although active device noise (and not the resonator noise) dominates the phase noise of most CMOS oscillators [1], in a properly designed oscillator, the quality factor, Q, of the resonant tank indirectly plays a central role in the phase noise. The best phase-noise/power trade-off is usually achieved at the borderline between the current- and voltage-limited regimes. At this operating point, the tank amplitude is proportional to $I_{bias} \cdot R_{tank}$, where I_{bias} is the oscillator dc bias current and R_{tank} is the equivalent tank parallel resistance [2]. A higher tank Q translates to a larger effective tank parallel resistance, R_{tank}. This, in turn, allows the designer to lower the oscillator's bias current, I_{bias}, while maintaining the full voltage swing necessary for operation at the edge of the voltage-limited regime. The lower bias current decreases the noise from the active devices, which is often the dominant contributor to phase noise. This explains the well-established fact that higher tank quality factor can be used to improve oscillator phase noise.

In typical integrated circuit applications, the inductor quality factor, Q_{ind}, often limits the quality factor of the resonator. Q_{ind} is mostly limited by ohmic and substrate losses. For a given oscillation frequency in a parallel LC tank, it is desirable to use the smallest L possible to minimize the noise of the resonator [1]. This smaller L also helps with the smaller LC product needed in a higher frequency oscillator.

There are two ways to implement these small on-chip inductors, namely single turn spiral and slab inductors. For a given L and metal width w, the slab inductor length is shorter than the perimeter of the single turn spiral loop of the same inductance. This is due to the negative mutual inductance between the segments on the opposite sides of the single turn spiral. Moreover, the shunt resistance through the substrate between the two terminals of the slab inductor is higher when compared to that of the single turn spiral due to the larger distance between them. Therefore slab inductors have smaller series and substrate losses, and present a higher Q, when compared to the single turn spiral. In addition, the slab inductor is easier to model and optimize due to its inherently simpler geometry. Despite these advantages, slab inductors are not commonly used in an integrated oscillator because of the intrinsic topological constraints for the interconnection of their terminals in the layout. The slab inductor terminals must be connected to the resonating capacitor C and to the oscillator core (Fig. 21.1.1). These interconnections add additional inductance and loss that can defeat the purpose.

To overcome these issues, individual oscillator cores using slab inductors are laid out adjacent to one another and in a circular configuration similar to that used to implement a power amplifier in [3] (Fig. 21.1.2). In this implementation, the individual oscillators share two slab inductors with the neighboring oscillator cores. In the desired mode of operation, the slab inductor terminals oscillate at opposite phases. Therefore, an ideal connection of the active oscillator core across the slab inductor can be imitated by connecting the active cores to two adjacent terminals of neighboring slabs. This will work when the slabs are placed in a circular geometry, as in Fig. 21.1.2.

While very effective in principle, this approach can suffer from parasitic modes of oscillation and self-induced dc latching problems in the absence of safeguards against these phenomena. For instance, Fig. 21.1.3 shows a possible stable dc solution of the topology. From a dc standpoint, it is nothing but four latches connected in a loop.

Interestingly, at the desired oscillation mode, the slab inductor middle points are at virtual ground. Thus, connecting them at dc would suppress the undesired dc and parasitic modes of oscillation, while it will not affect the desired mode of operation. This can be done in a symmetric fashion by introducing a cross, connecting the mid-points of the slab inductors at the center of the oscillator, as in Fig. 21.1.2. This connection will short the outputs of the oscillator cores at low frequencies and even harmonics avoiding any possible dc latching. In addition to eliminating the dc latch issue, the cross loads the outputs of the oscillators with a small impedance decreasing the start up gain of the parasitic oscillation modes. The oscillator output is taken by buffering the output of a circular pick-up loop in the middle of the oscillator.

This topology can be implemented using any number of corners and with a variety of active cores, such as the PMOS- or NMOS-only cross-coupled oscillators or the noise shifting differential Colpitts oscillator [4]. It can also be used to implement oscillators with differential tanks, such as the complementary cross-coupled oscillator.

Single frequency and voltage controlled Circular-Geometry oscillators with four corners were implemented using 0.18μm CMOS transistors. Full electromagnetic simulations were carried out to model the high frequency behavior of the slab inductors and the coupling between them. For these prototypes, we used the complementary cross-coupled oscillator core due to its higher oscillation amplitude and low voltage of operation. The single frequency Circular-Geometry oscillator operates at 5.33GHz and shows a phase noise of –147.3dBc/Hz at 10MHz offset from the carrier while drawing 10mA from a 1.4V supply. Fig. 21.1.4 shows the phase noise plot for this oscillator, and Fig. 21.1.5 is the die photo. The voltage controlled Circular-Geometry oscillator has a center frequency of 5.36GHz and 8% of continuous frequency tuning with a phase noise of –142.2dBc/Hz at 10MHz offset from the carrier when drawing 12mA from a 1.8V supply. The lower phase noise of the fixed frequency oscillator compared to the VCO is primarily due to the low quality factor of the varactors at higher frequencies.

The summary of the measurements for these oscillators is reported in Fig. 21.1.6. To evaluate their performance, the unitless power-frequency-normalized and power-frequency-tuning-normalized figures of merit [1]

$$PFN = 10\log\left[\frac{kT}{P_{\sup}} \cdot \left(\frac{f_0}{f_{off}}\right)^2\right] - L\{f_{off}\} \quad (1)$$

$$PFTN = 10\log\left[\frac{kT}{P_{\sup}} \cdot \left(\frac{f_{tune}}{f_{off}}\right)^2\right] - L\{f_{off}\} \quad (2)$$

were calculated for recently published CMOS LC oscillators above 4GHz and are shown in Fig. 21.1.7.

References:

[1] D. Ham and A. Hajimiri, "Concepts and Methods in Optimization of Integrated LC VCOs," *IEEE J. Solid-State Circuits*, vol. 36, no. 6, pp. 896-909, June 2001.

[2] A. Hajimiri and T. Lee, "Design Issues in CMOS Differential LC Oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 717-24, May 1999.

[3] I. Aoki, S. Kee, D. Rutledge, and A. Hajimiri, "Fully Integrated CMOS Power Amplifier Design Using the Distributed Active-Transformer Architecture," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 371-83, March 2002.

[4] R. Aparicio and A. Hajimiri, "A Noise-Shifting Differential Colpitts VCO," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1728-36, Dec. 2002.

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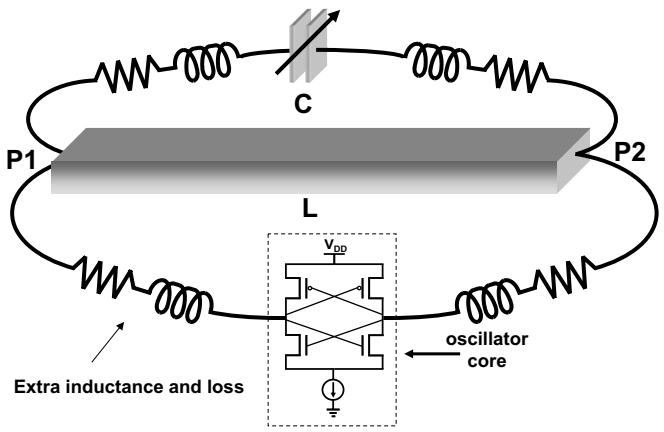

Figure 21.1.1: Slab inductor terminal connection issues.

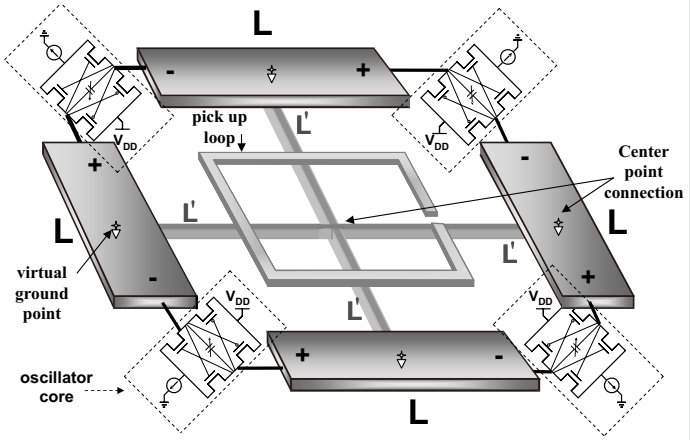

Figure 21.1.2: Proposed oscillator topology.

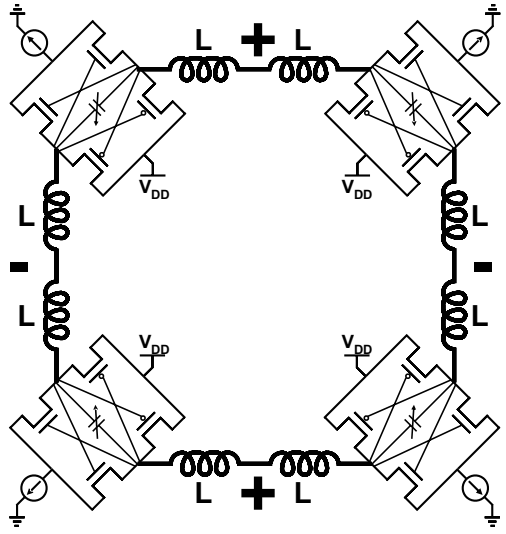

Figure 21.1.3: dc latching issues.

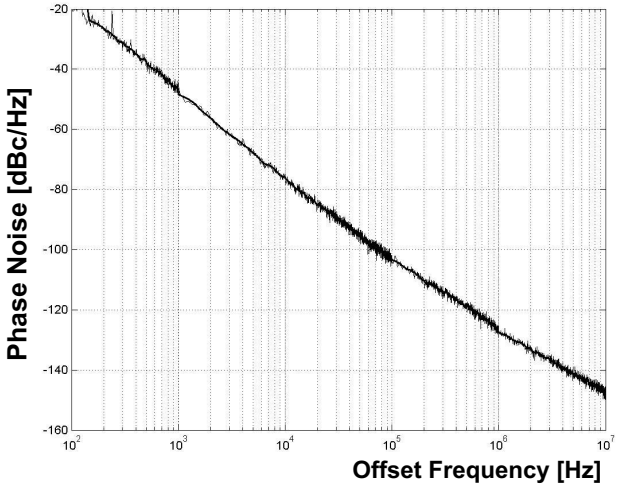

Figure 21.1.4: Single frequency Circular-Geometry oscillator phase noise plot at f_{osc}=5.35GHz.

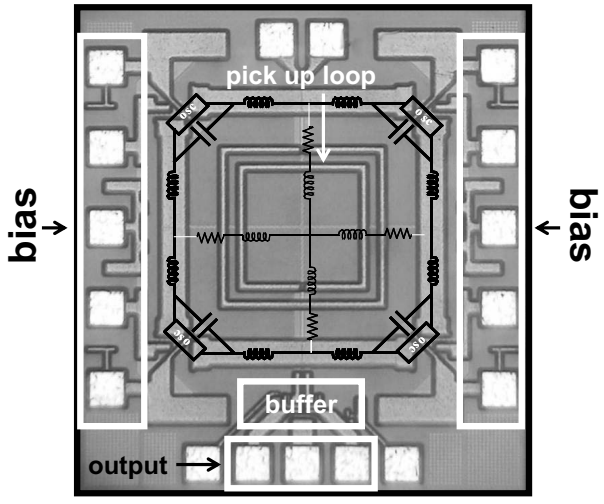

Figure 21.1.5: Die micrograph.

Circular-Geometry Oscillator	Single Frequency	VCO
Technology	IBM 7HP SiGe (CMOS transistors only)	
Channel Length	0.18μm	
Center Frequency	5.33GHz	5.36GHz
Frequency Tuning	NA	8.3%
Output Power	1dBm	
V_{dd}	1.4V	1.8V
I_{bias}	10mA	12mA
Phase Noise @ 10MHz offset	-147.3 dBc/Hz	-142.2 dBc/Hz

Figure 21.1.6: Performance summary.

Author	Reference	Technology	Frequency	Power	PFN	PTFN
Circular-Geometry Single Frequency	**This work**	**SiGe 0.18 µm**	**5.33GHz**	**14mW**	**16.5**	**NA**
Ainspan *et al*	ESSCIRC 2000	CMOS 0.24 µm	7.3 GHz	2.4mW	16.3	4.2
Andress *et al*	ISSCC 2004		10GHz	2.93mW	11.5	NA
Tsang *et al*	RFIC 2003	CMOS 0.18 µm	12GHz	1.4mW	11.03	-18.4
Chang *et al*	RFIC 2003	CMOS 0.18 µm	5.5GHz	3.6mW	10.4	-2.8
Circular-Geometry VCO	**This work**	**SiGe 0.18 µm**	**5.15GHz**	**25.2mW**	**9.6**	**-12.0**
De Anter *et al*	ISSCC2001	CMOS 0.25µm	17 GHz	10.5mW	8.75	-12.7
H-M Wang	ISSCC 2001	CMOS 0.25µm	50 GHz	13mW	8.0	-25.1
Tiebout *et al*	ISSCC 2002	CMOS 0.12µm	50 GHz	1mW	5.4	-27.2
Wu *et al*	CICC 2000	BiCMOS 0.35µm	10 GHz	35mW	4.9	-13.7

Figure 21.1.7: Comparison of oscillators above 4GHz.

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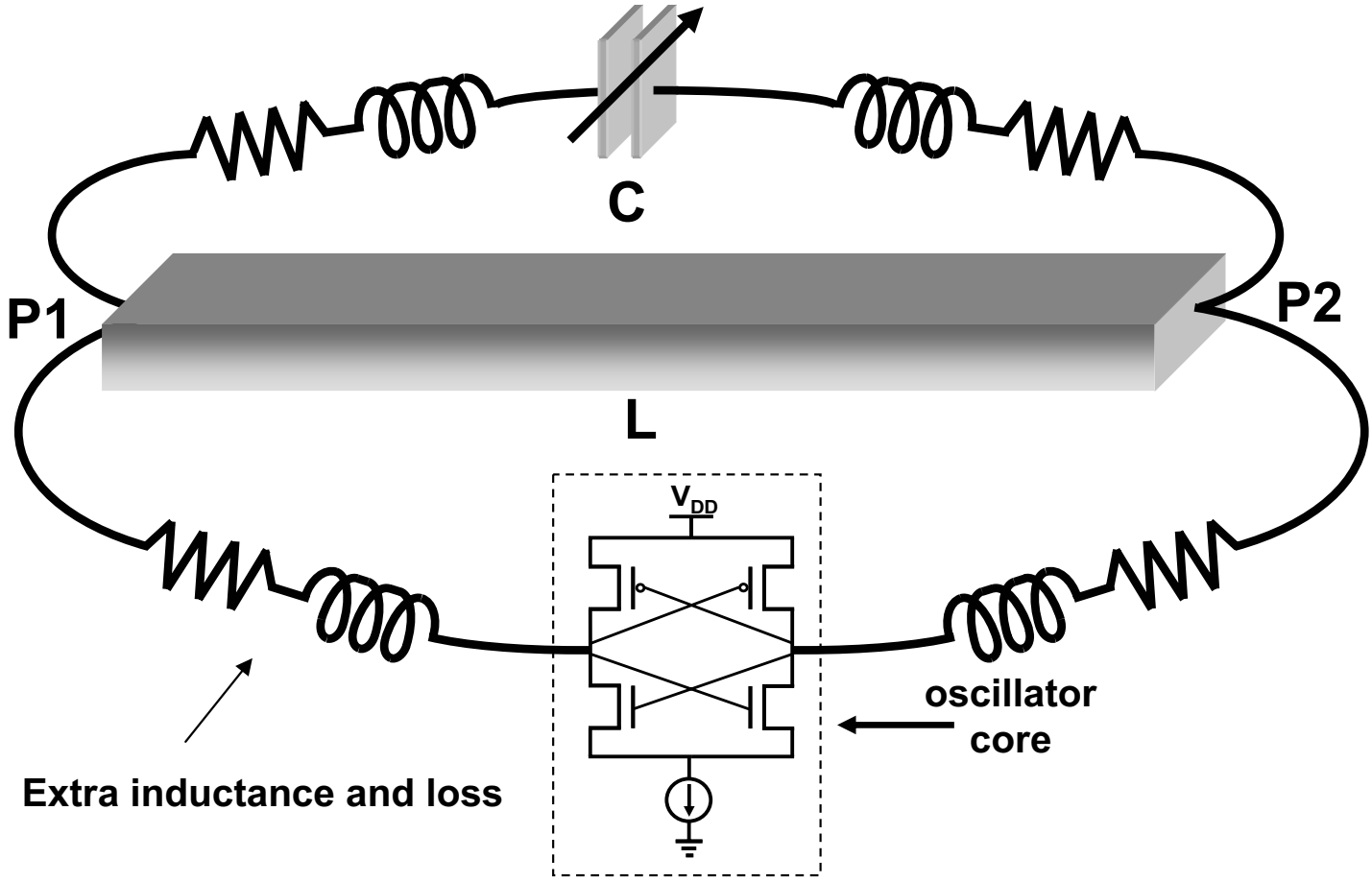

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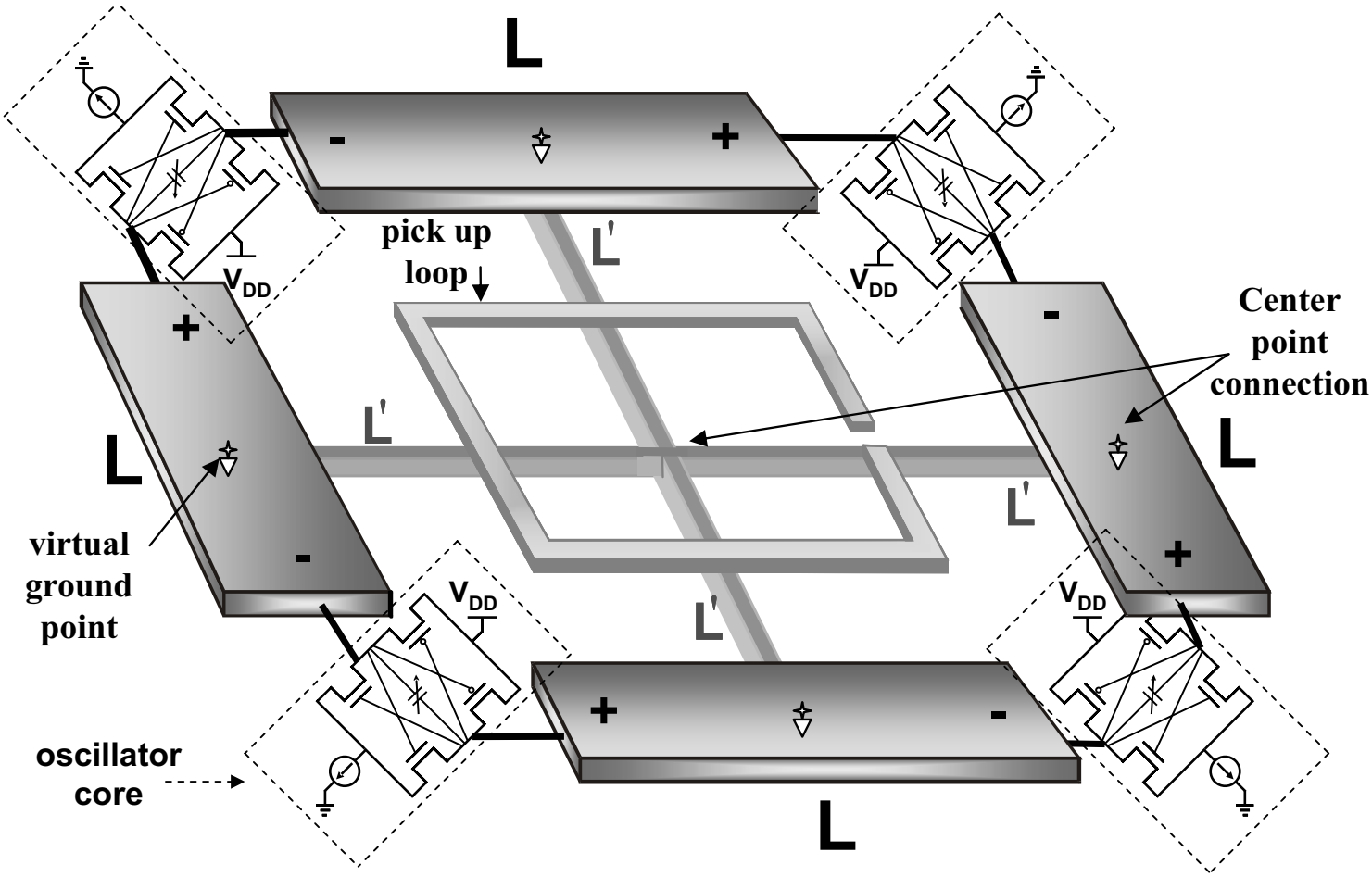

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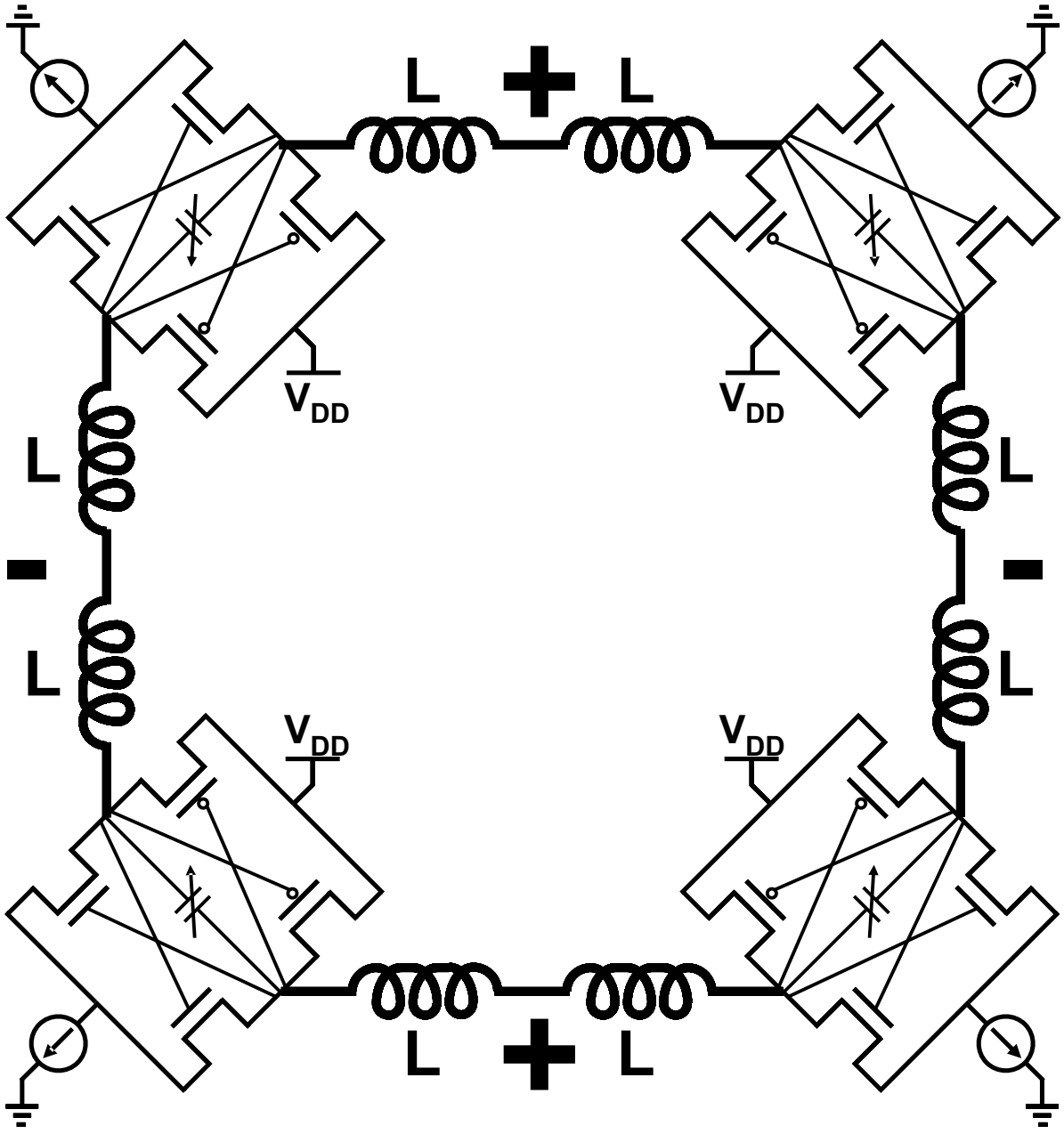
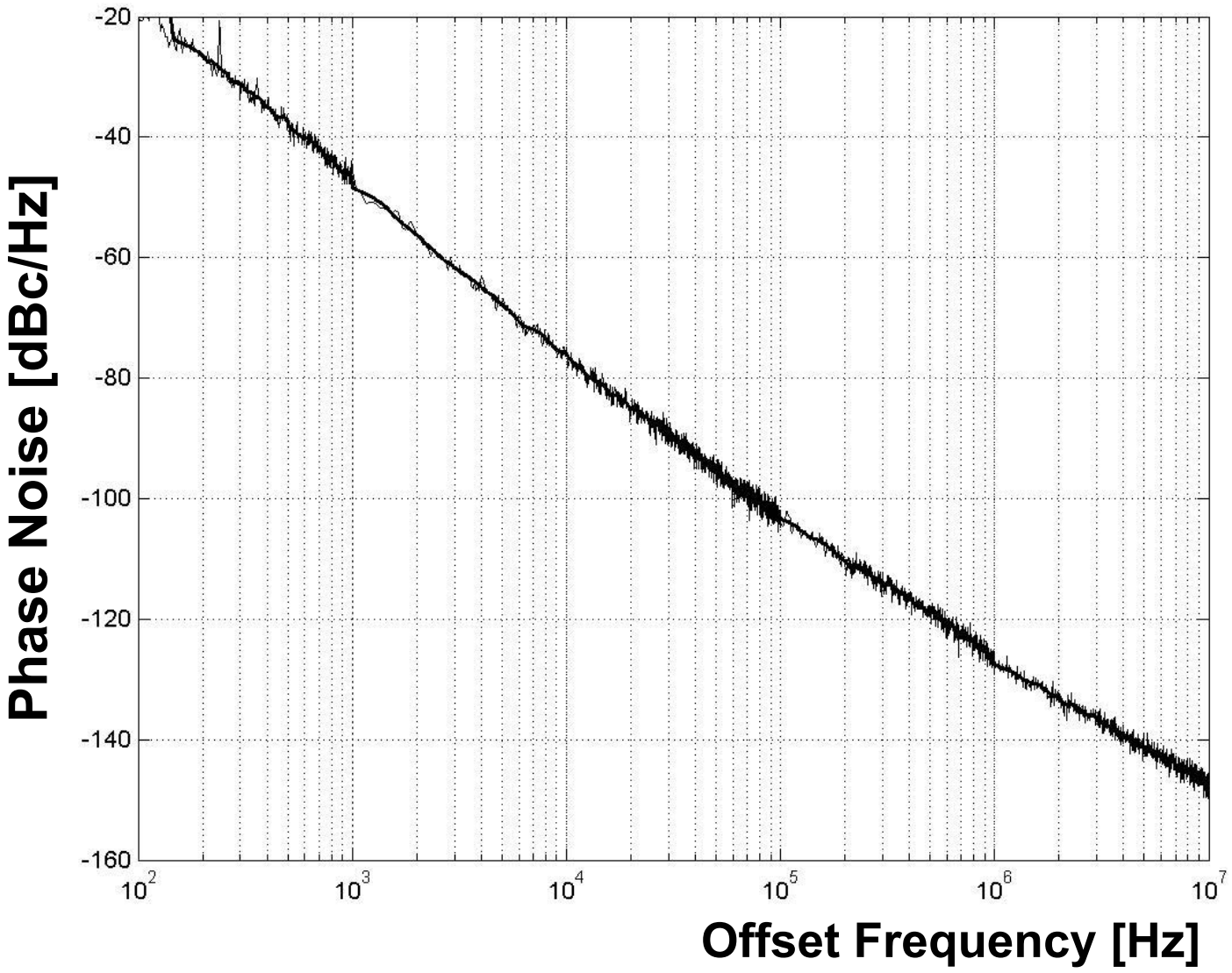


Figure 21.1.3: dc latching issues.



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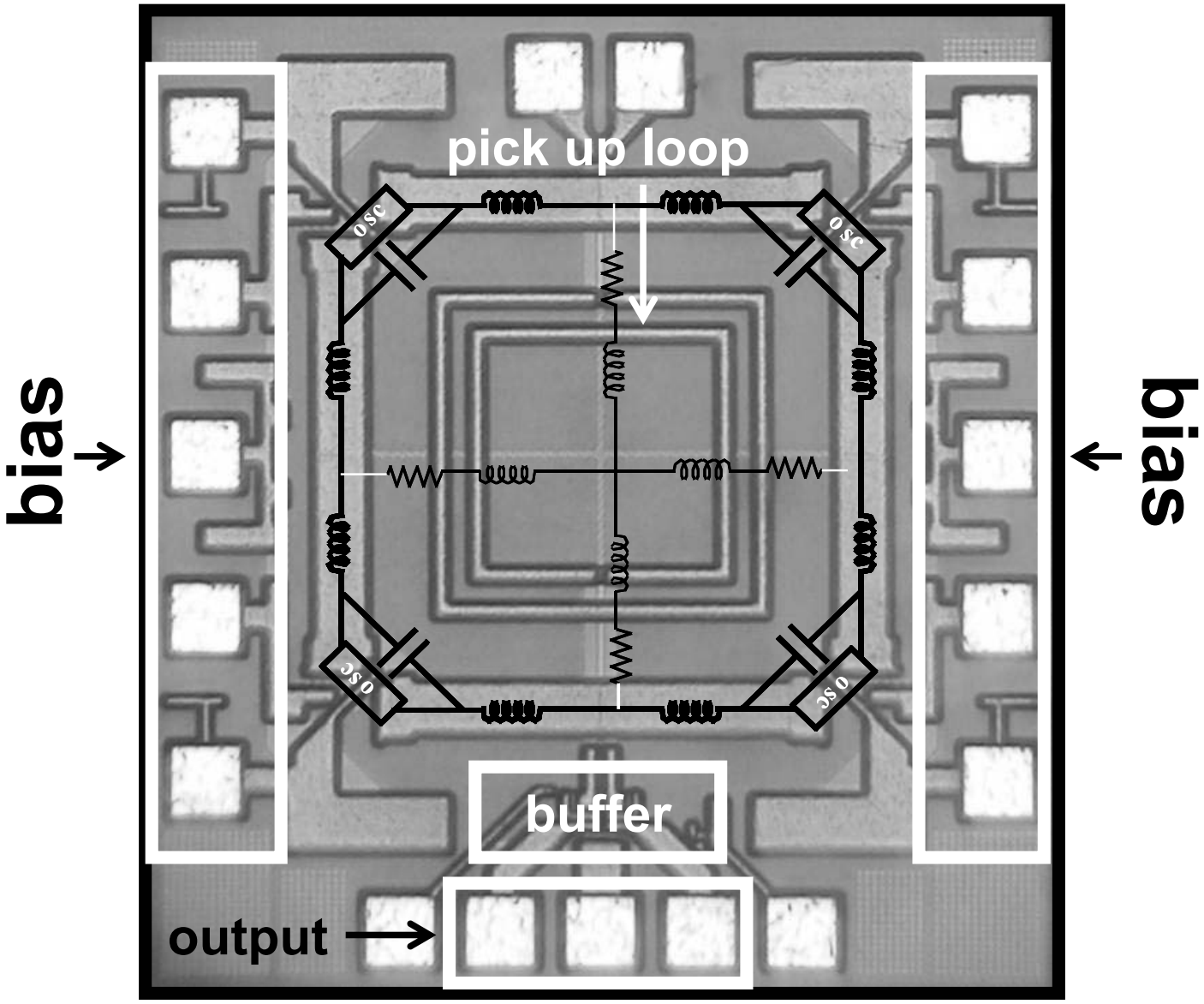

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