Circular-Geometry Oscillators

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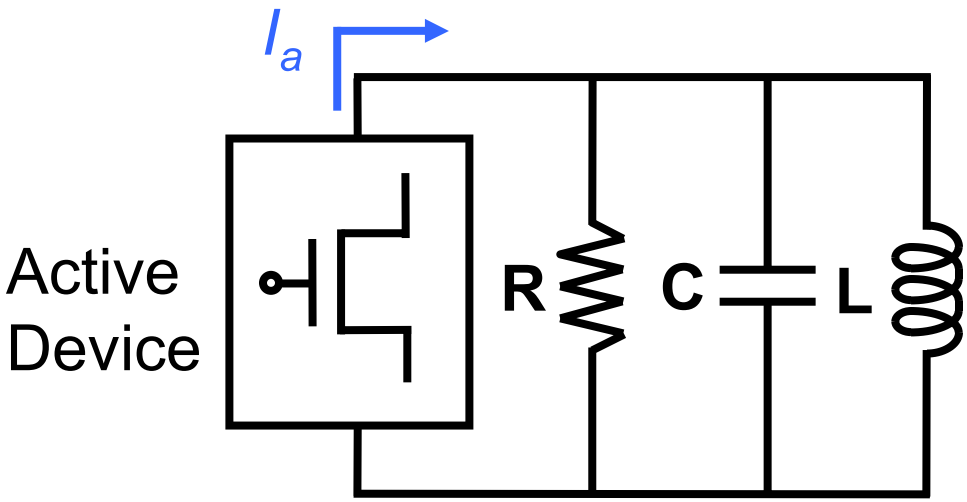
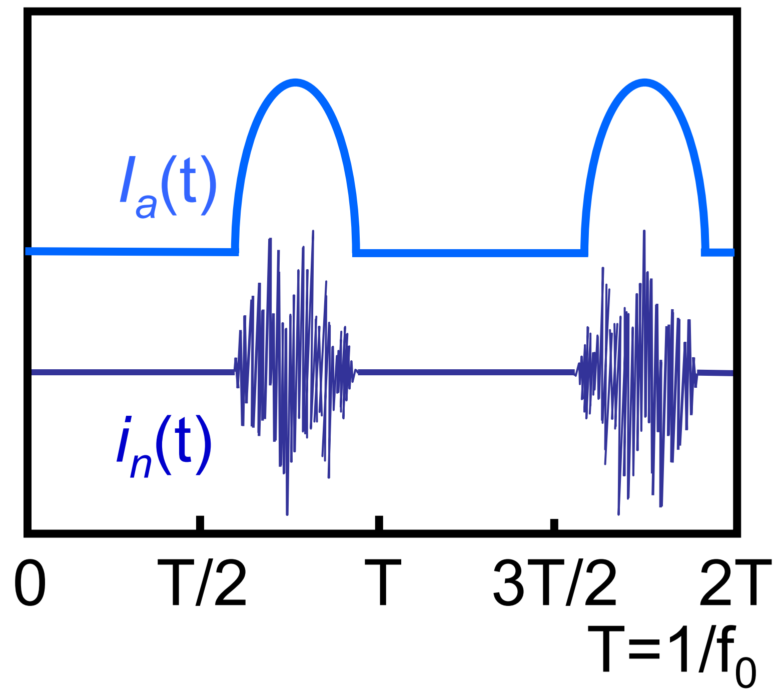
Outline

- The effect of tank *Q*
- Inductor selection and comparison
- Circular-geometry oscillators
- Experimental results
- Conclusions

Active Device Noise

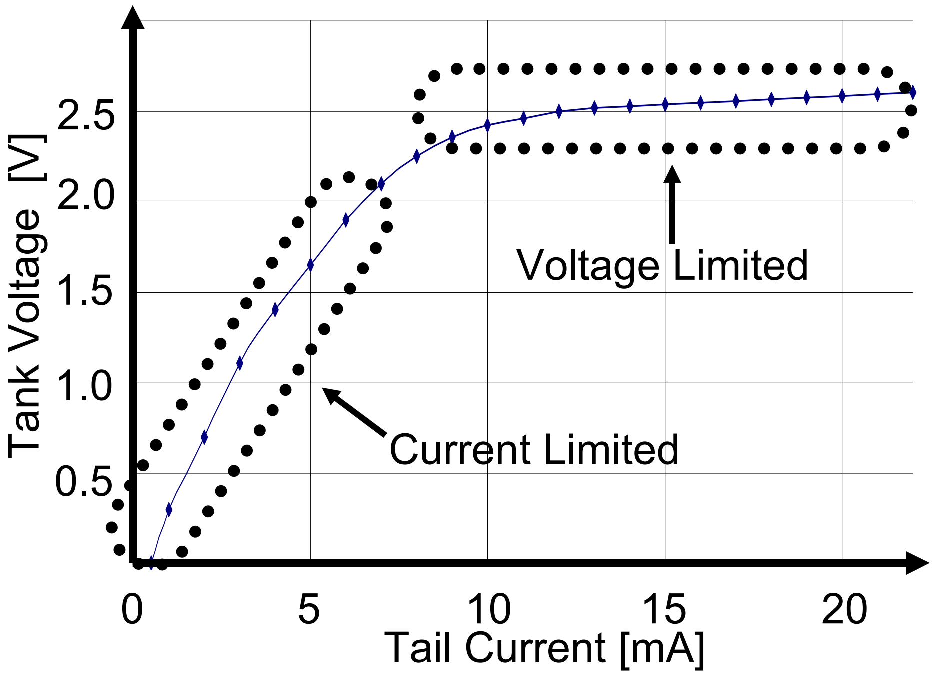




- Active device noise dominates the phase noise of most CMOS oscillators[1].

[1] D. Ham and A. Hajimiri, "Concepts and methods in optimization of integrated LC VCOs", IEEE JSSC, June 2001.

Importance of Tank Q



- Q_{tank} plays a central role in the phase noise *indirectly*.

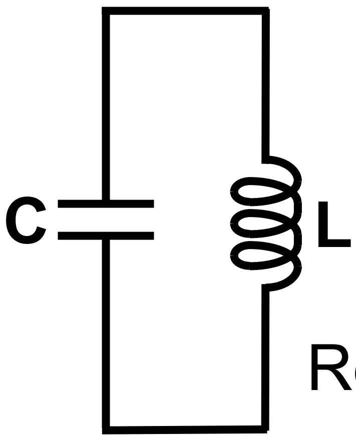
$$V_{\text{tank}} \approx R_{\text{tank}} \cdot I_{bias}$$

$$Q_{\text{tank}} = \frac{R_{\text{tank}}}{\omega L}$$

For V_{tank}=constant, if Q_{tank} ⇧ then I_{bias} ⇩

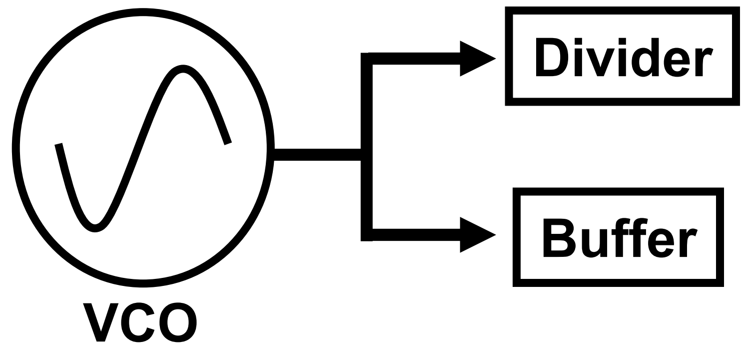
- The lower bias current decreases the noise from the active devices.

High Frequency Oscillator Constraints



$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

$$\text{Resonator Noise} = \frac{kT}{C}$$

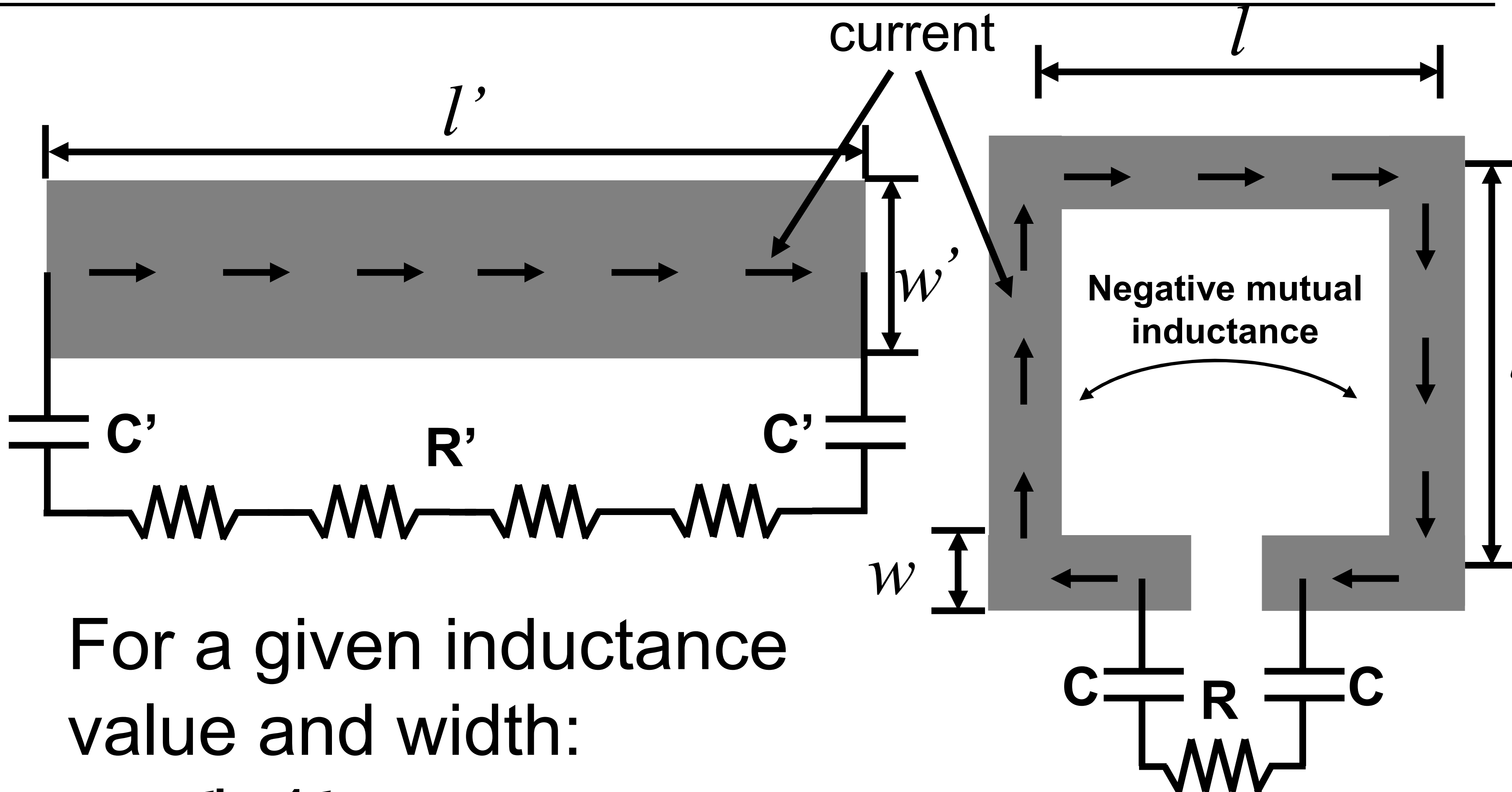


Lower Resonator Noise ⇒ L ↓ and C ↑

Higher f_0 ⇒ L ↓ and/or C ↓

- Q_{ind} often limits Q_{tank},
- Higher frequencies requires a smaller inductance, L.

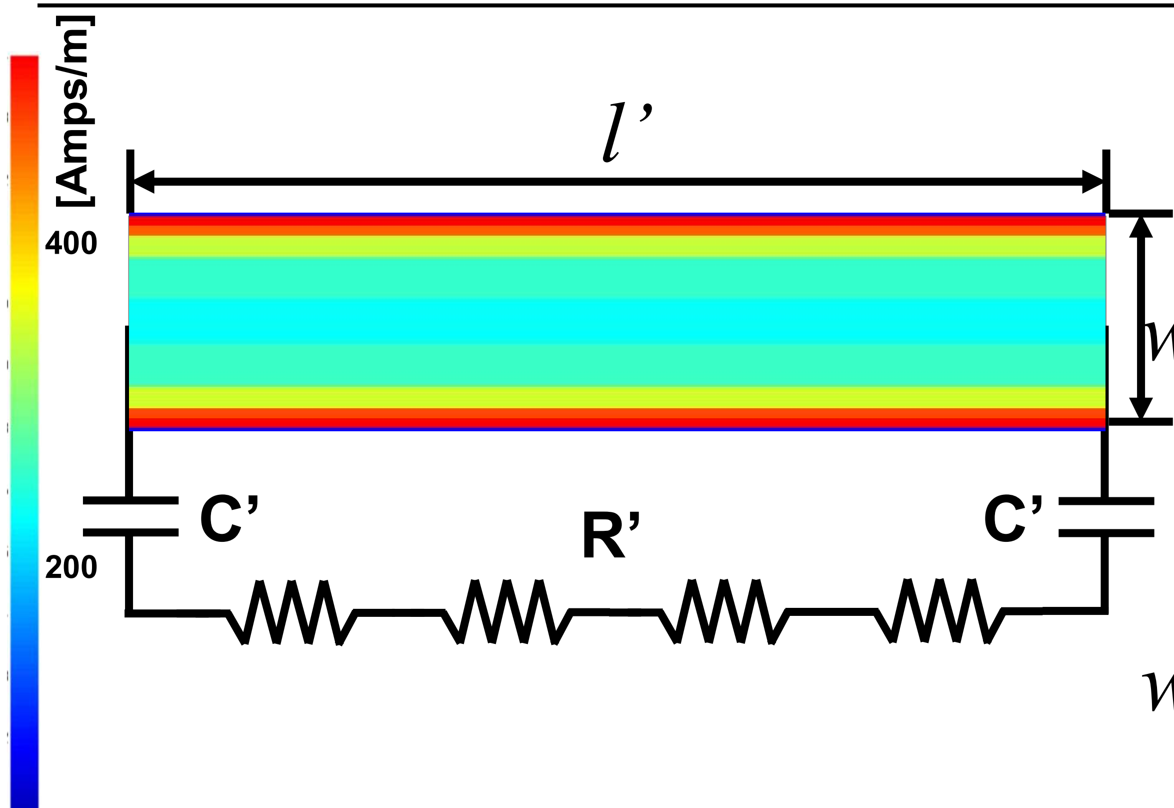
Low Impedance Inductor Comparison

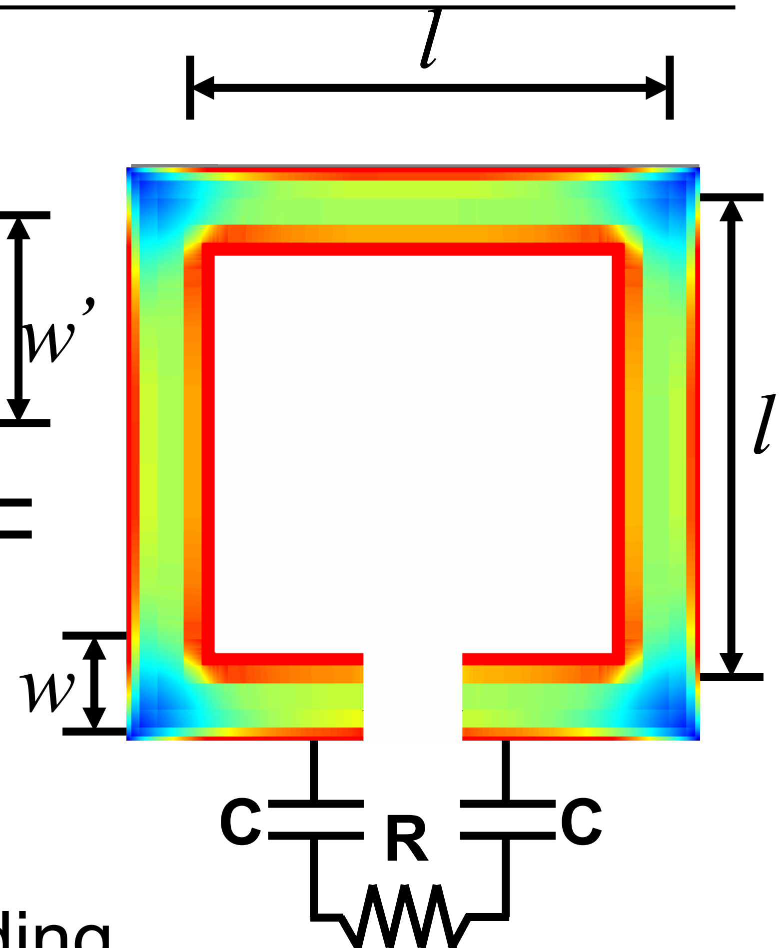


For a given inductance value and width:

- $l' < 4l$
- $R' > R$

Low Impedance Inductor Comparison

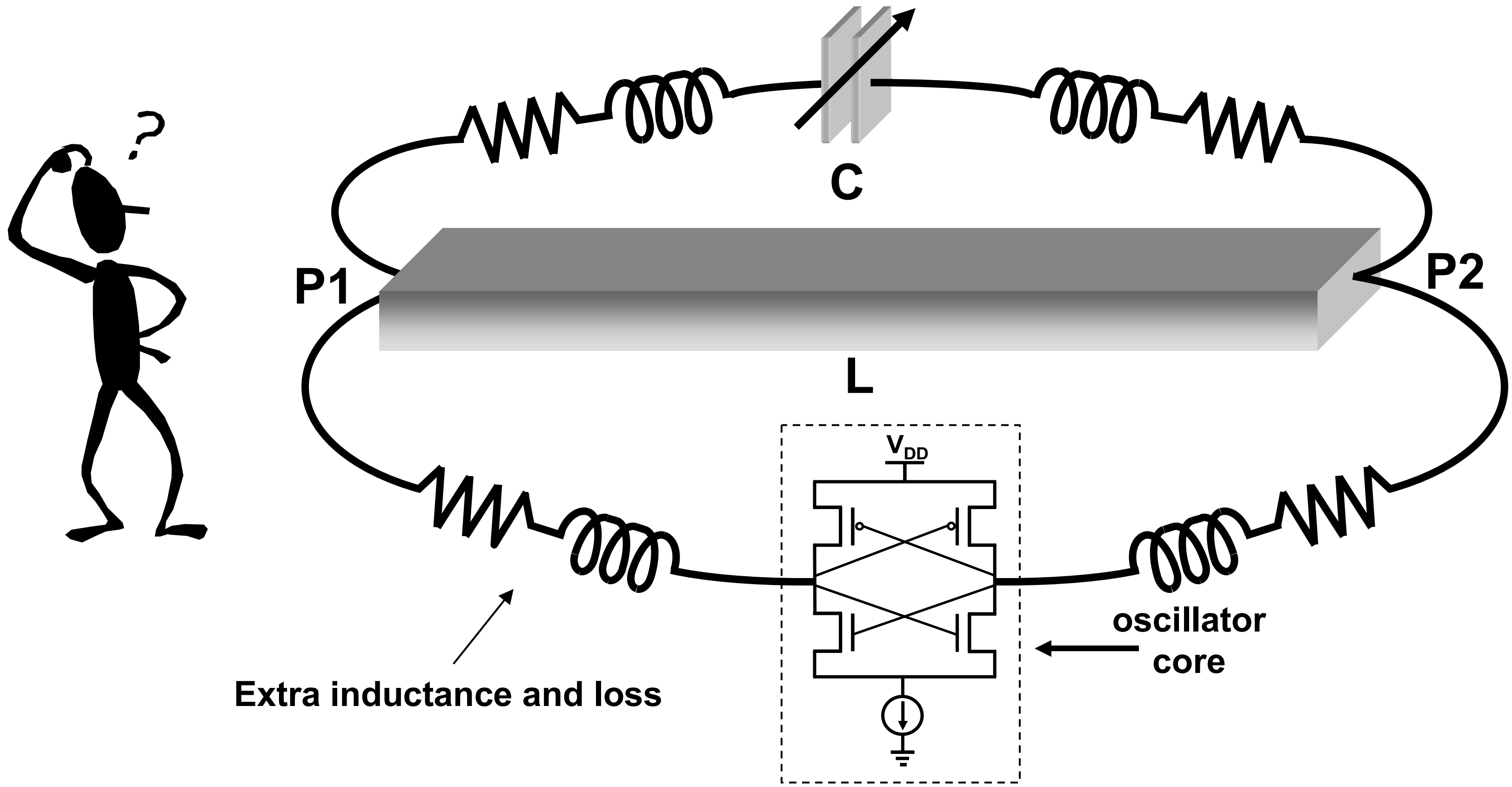




Slab inductors:

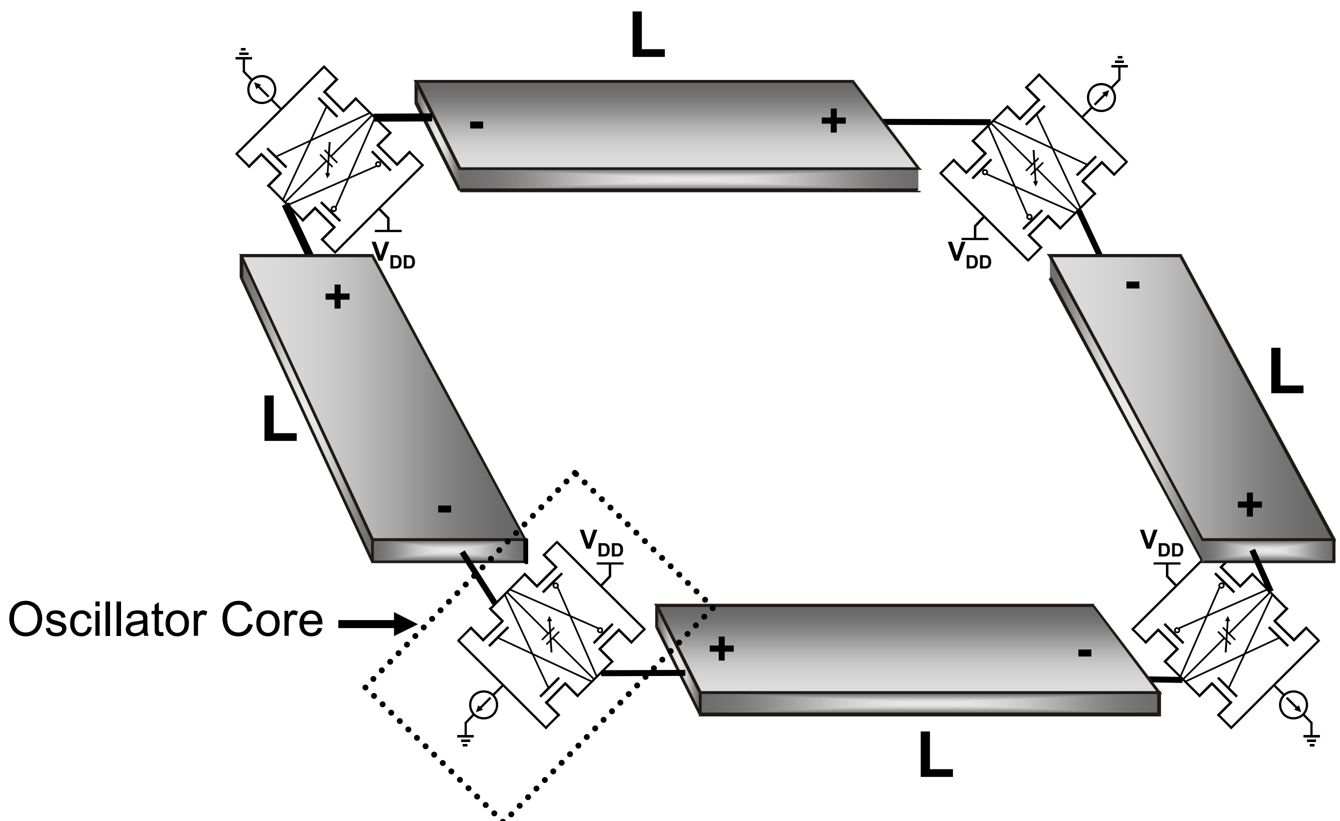
- Present less current crowding,
- Have smaller series and substrate losses,
- Are easier to optimize due to simpler geometry.

Slab Inductor Issues



Interconnects add inductance and loss!

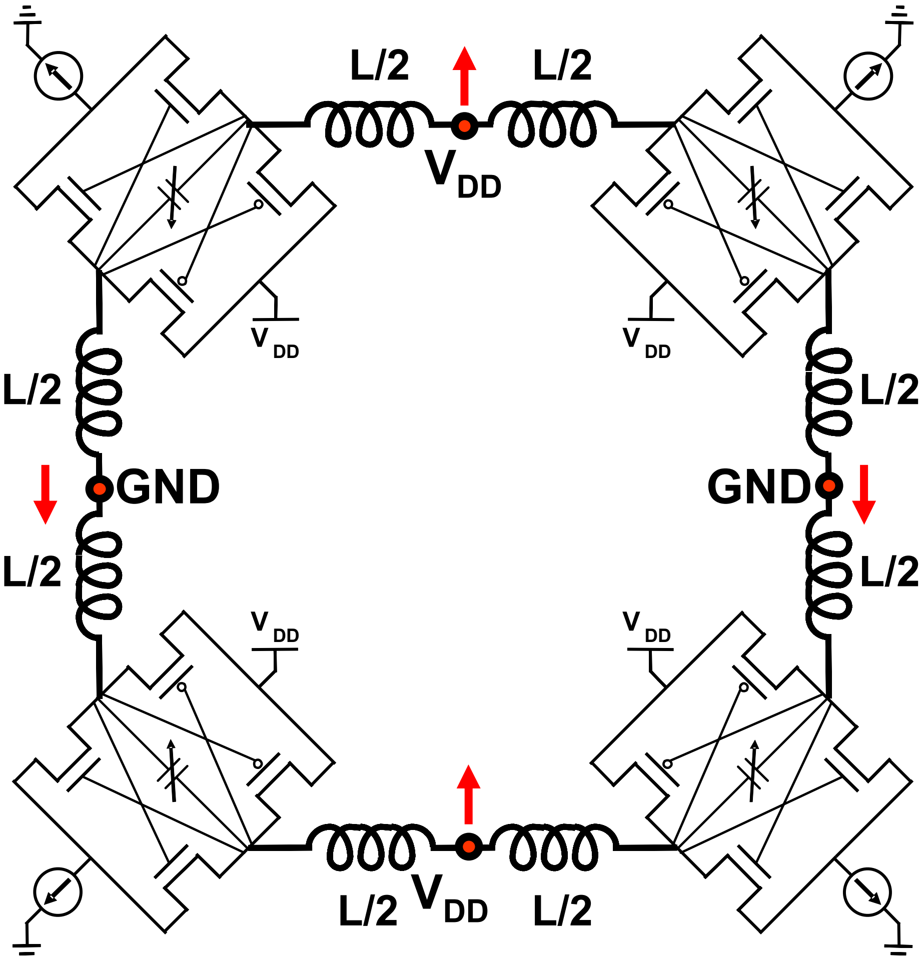
Circular-Geometry Oscillators



•Direct oscillator implementation with slab inductors using a circular-geometry structure. [1]

[1] I. Aoki, S. Kee, D. Rutledge, and A. Hajimiri, “Fully integrated CMOS power amplifier design using the distributed active-transformer architecture”, IEEE CICC, May 2001.

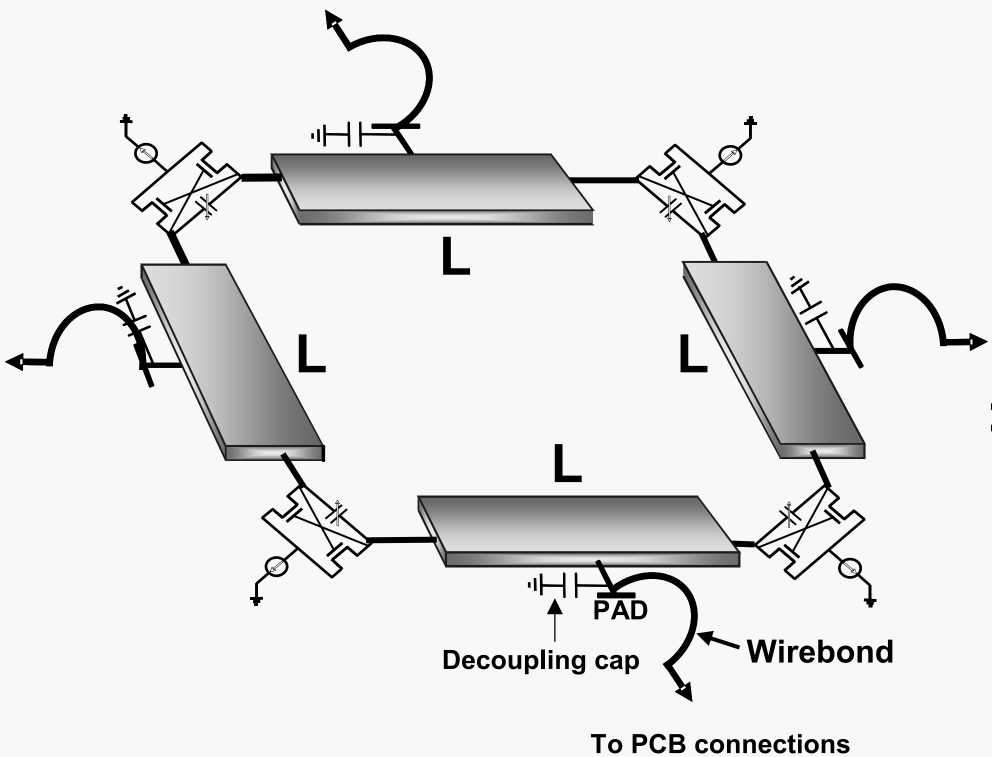
Direct Implementation Issues

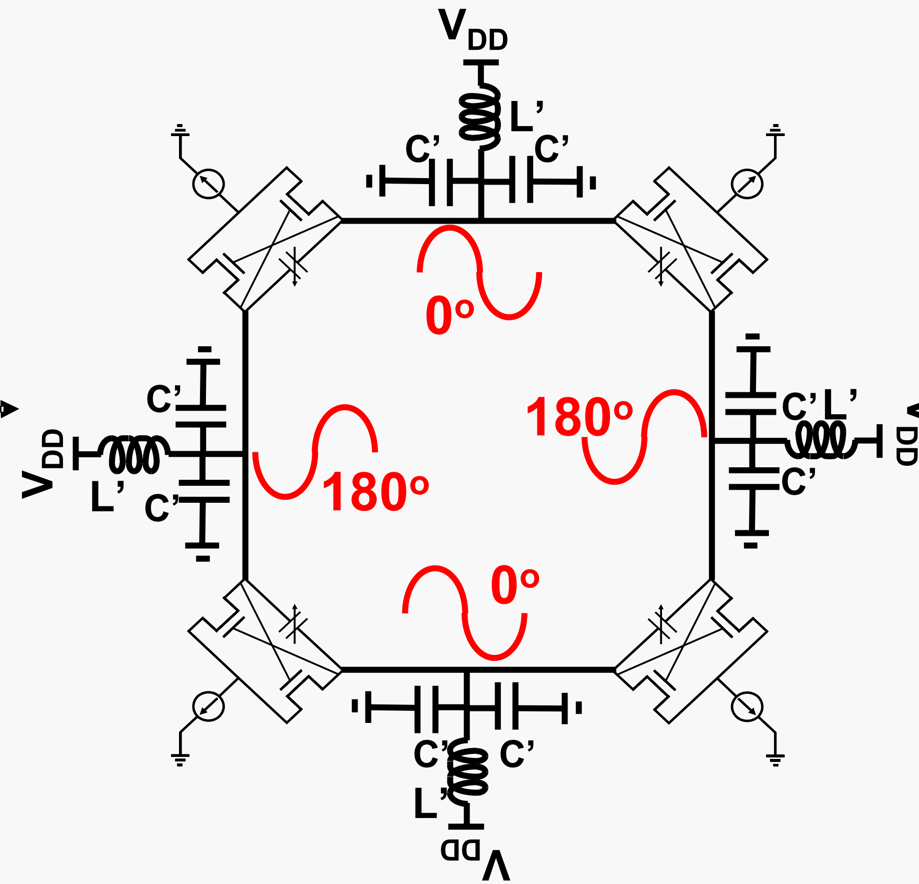


***dc* latching**

•Possible stable dc solution of a topology using 4 corners and complementary cross-coupled oscillator as a core.

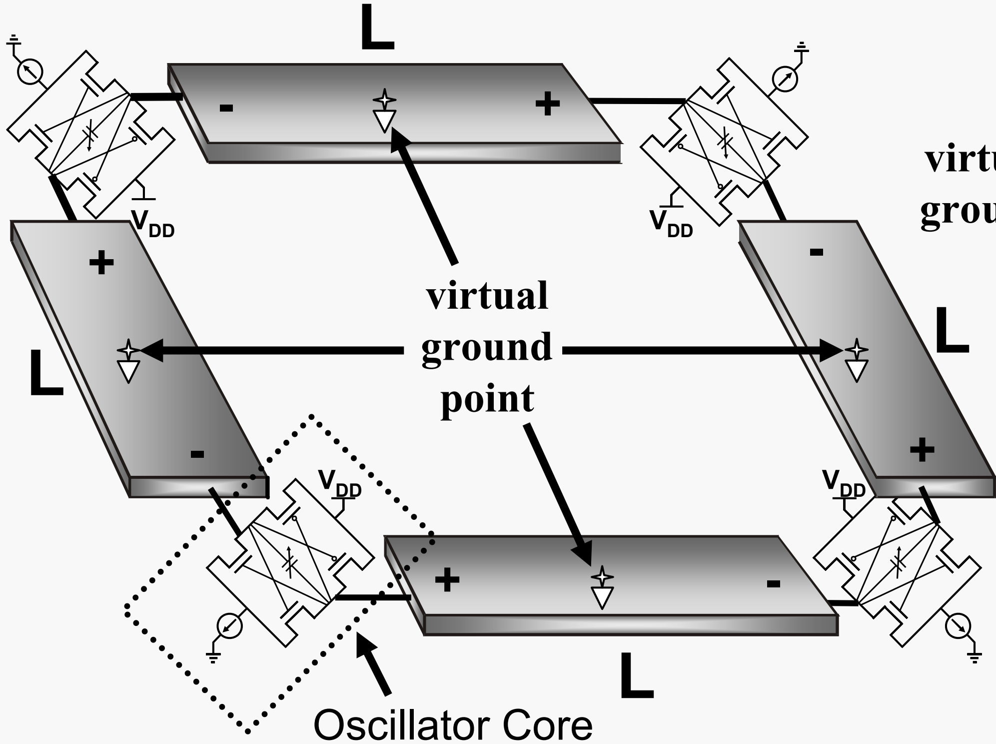
Multiple Oscillation Modes

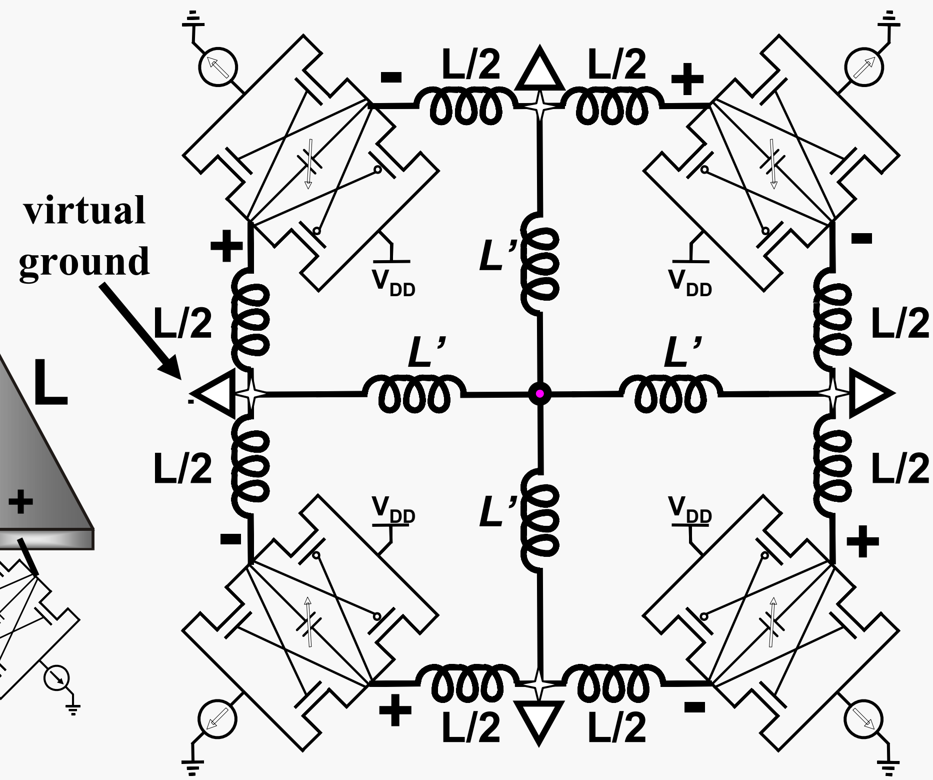




•Parasitic modes of oscillation in the absence of safeguards against this phenomena.

Middle Point Cross-Connection

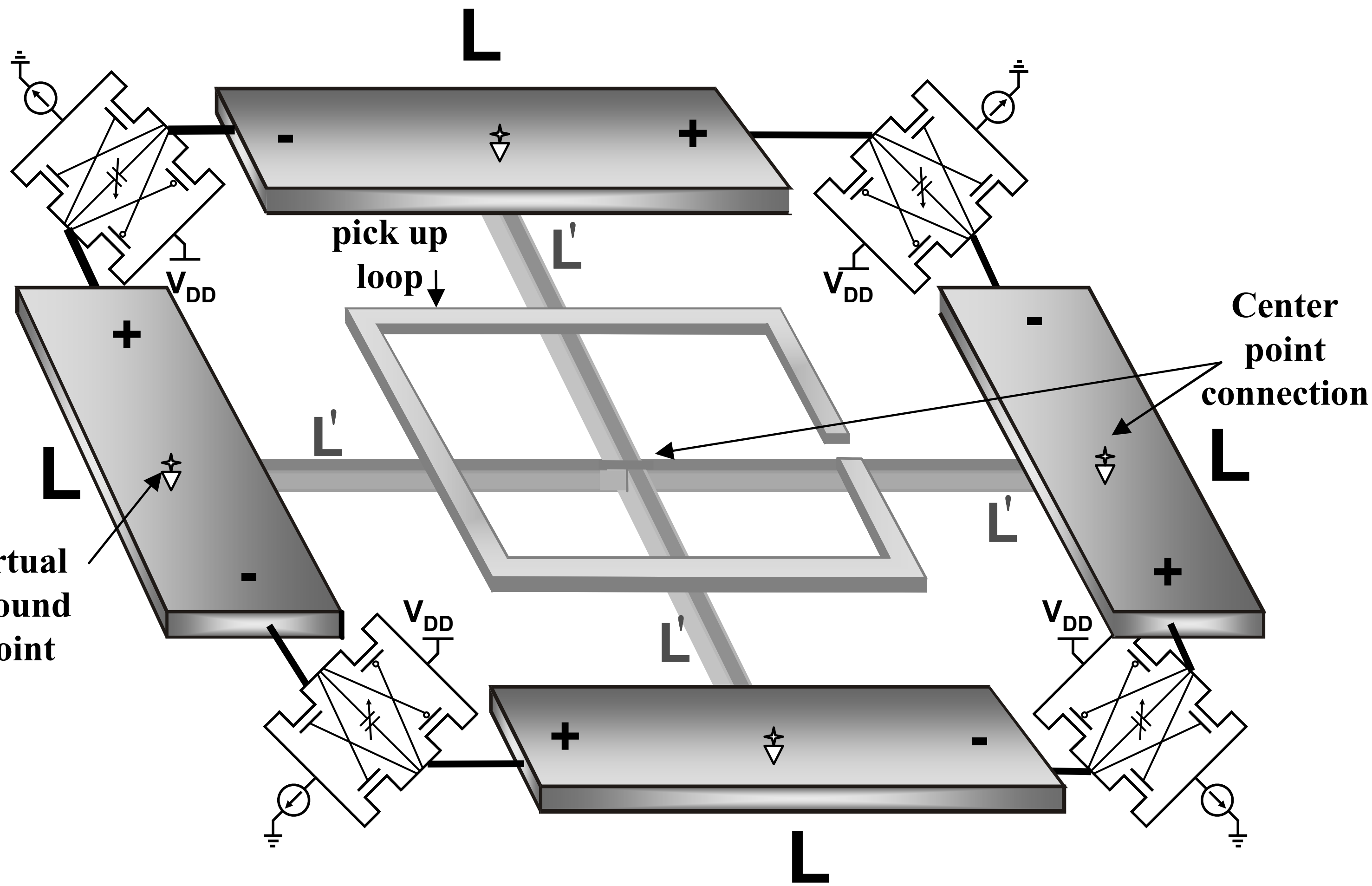




•Shorts the outputs of the oscillator cores at low frequencies and even harmonics,

•Loads the cores with a small impedance decreasing the start up gain of the undesired oscillation modes.

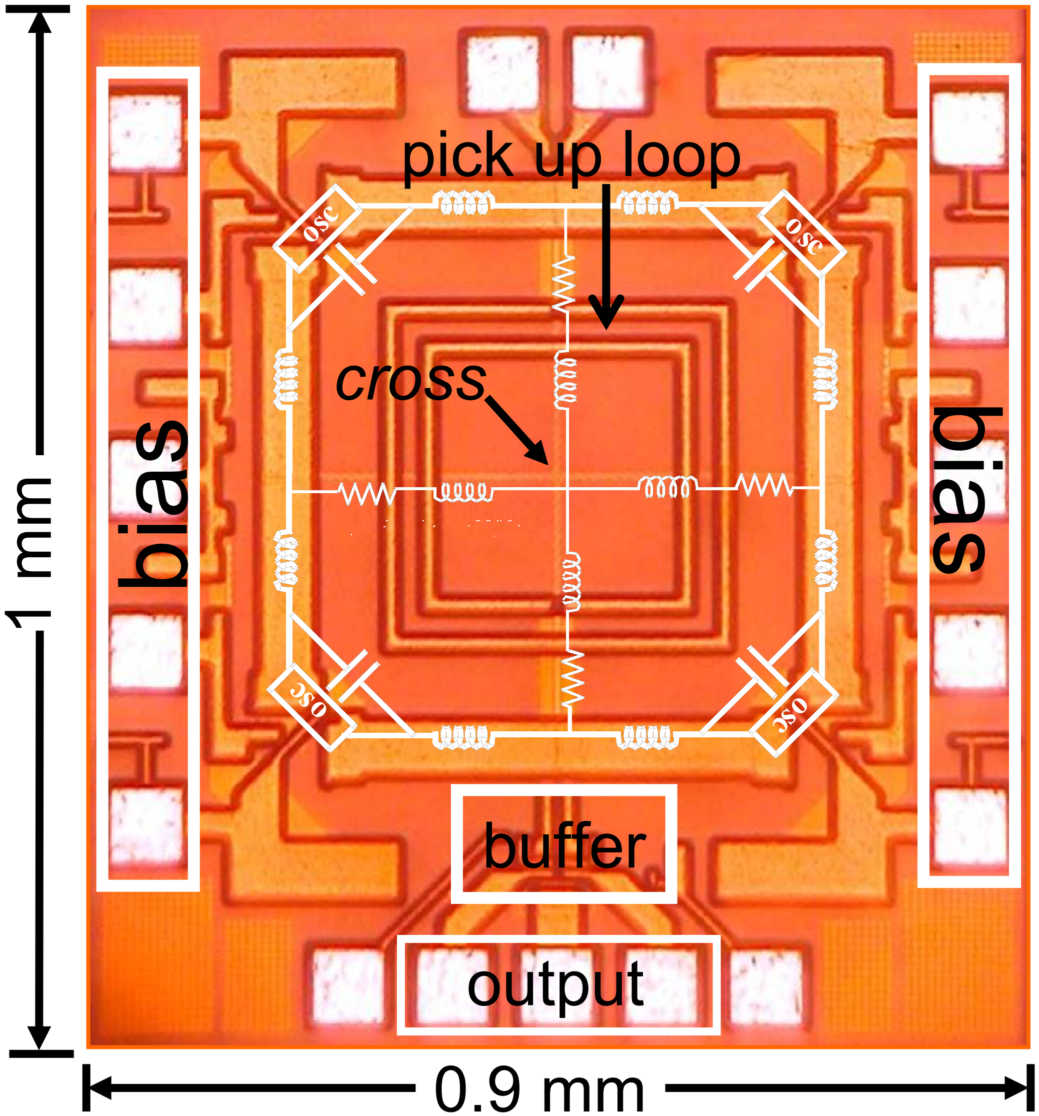
Proposed Oscillator Topology



•Output extracted by a pick-up loop in the center,

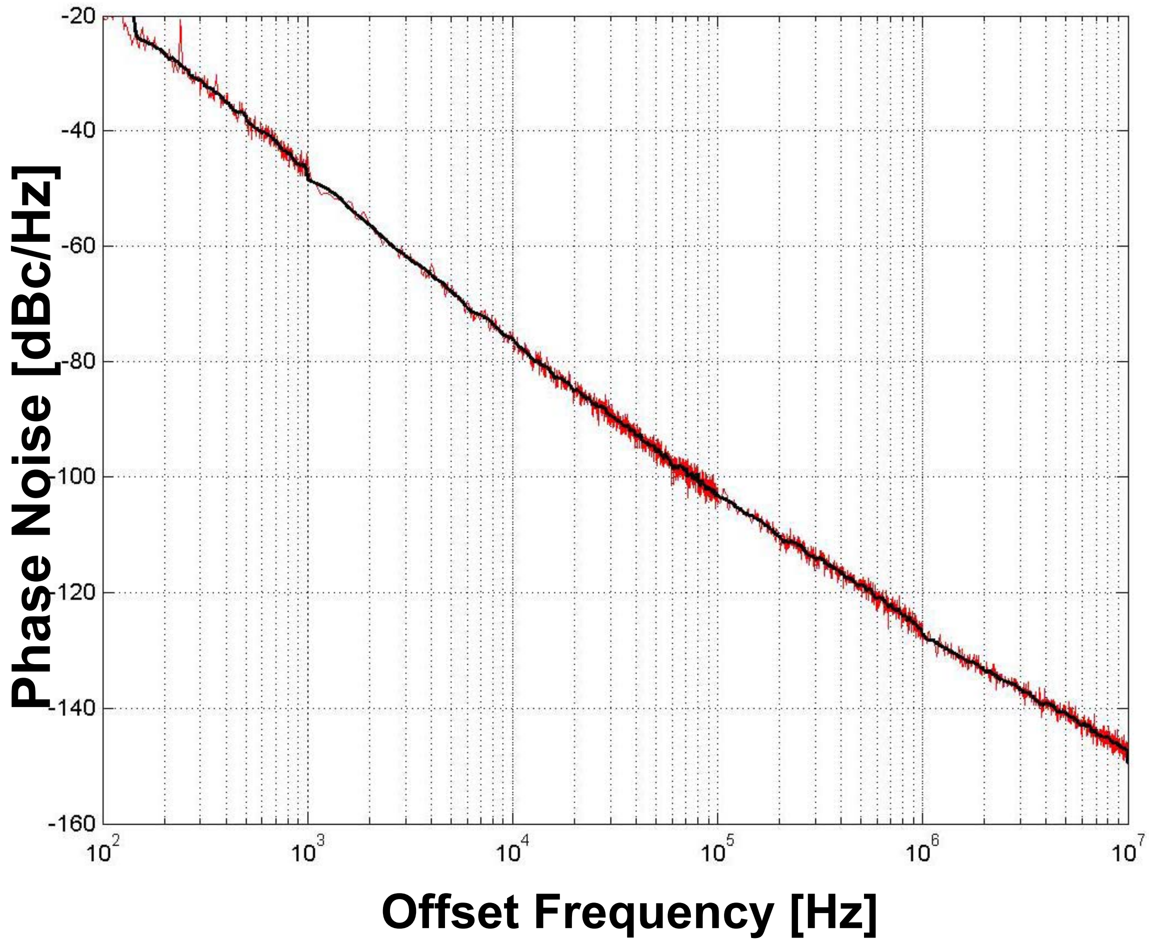
•This topology can be implemented using any number of corners and with a variety of active cores.

Implemented Oscillator



Circular-Geometry Oscillator	Single Frequency	VCO
Technology	SiGe 7HP (CMOS transistors only)	
Channel Length	0.18μm	
Center Frequency	5.35GHz	5.36GHz
Tuning Range	--	8.3%
Output Power	1dBm	
V_{dd}	1.4V	1.8V
I_{bias}	10mA	12mA

Phase Noise



Single frequency Circular-Geometry oscillator phase noise plot at f_{osc}=5.35GHz

Circular-Geometry Oscillator	Single Frequency	VCO
Phase Noise @10MHz offset	-147.3 dBc/Hz	-142.2 dBc/Hz
Frequency	5.35GHz	5.36GHz
V_{dd}	1.4V	1.8V
I_{bias}	10mA	12mA
Tuning Range	--	8.3%
Output Power	1dBm	

Oscillators Above 4GHz Comparison

$$PFN = 10\log\left[\frac{kT}{P_{sup}} \cdot \left(\frac{f_0}{f_{off}}\right)^2\right] - L\{f_{off}\}$$

$$PFTN = 10\log\left[\frac{kT}{P_{sup}} \cdot \left(\frac{f_{tune}}{f_{off}}\right)^2\right] - L\{f_{off}\}$$

Reference	Technology	Frequency	Power	PFN[1]	PTFN[2]
This work	**SiGe 0.18 μm**	**5.35GHz**	**14mW**	**16.5**	**NA**
This work	**SiGe 0.18 μm**	**5.36GHz**	**25.2mW**	**9.6**	**-12.0**
ESSCIRC 2000	CMOS 0.24 μm	7.3 GHz	2.4mW	16.3	4.2
RFIC 2003	CMOS 0.18 μm	12GHz	1.4mW	11.03	-18.4
RFIC 2003	CMOS 0.18 μm	5.5GHz	3.6mW	10.4	-2.8
ISSCC2001	CMOS 0.25μm	17 GHz	10.5mW	8.75	-12.7
ISSCC 2001	CMOS 0.25μm	50 GHz	13mW	8.0	-25.1
ISSCC 2002	CMOS 0.12μm	50 GHz	1mW	5.4	-27.2
CICC 2000	BiCMOS 0.35μm	10 GHz	35mW	4.9	-13.7

Conclusions

- A new circular-geometry oscillator topology is presented that allows the use of slab inductors,
- Can be implemented using any number of corners and with a variety of active cores,
- A general methodology to suppress the undesired oscillation modes and dc latching has been devised,
- Two circular-geometry oscillators are fabricated achieving some of the largest figures of merit.