

Demonstration of a Switchless Class E/F_{odd} Dual-Band Power Amplifier

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Abstract — A 250 W dual-band power amplifier belonging to the Class E/F switching amplifier family is presented. The amplifier operates in the 7 MHz and 10 MHz HAM bands, achieving 16 dB and 15 dB gain with power added efficiencies (PAE) of 92 % and 87 % in those bands, respectively. It utilizes dual-resonant passive input and output networks to achieve high-efficiency Class E/F_{odd} operation at both frequencies of operation, allowing the same passive networks to be used for both frequency bands without the use of band-select switches.

I. INTRODUCTION

Dual-band transceiver systems have been proposed to address the increasing demand for system flexibility [1] and capacity [2] created by the continuing growth of wireless communication applications. Such systems need a means of amplifying signals at the two frequencies of operation. In particular, they require power amplifiers on the transmitter side capable of operation in both bands.

Various dual-band power amplifier design strategies have been employed in the past [2], each differing in the amount of circuitry used for operation in both bands. To date, all reported dual-band power amplifiers utilize semiconductor switches to re-route the signal depending on the band of operation, employ diplexers, or employ electronically tunable components [2,3].

The implicit assumption for using active signal-routing switches seems to be that active switches outperform dual-band tuned passive networks. However, because each active device in the signal path itself introduces significant losses, we propose a design strategy avoiding the use of such signal-routing devices. Furthermore, using networks tuned at both frequencies of operation allows a reduced component count compared to strategies using diplexers.

In this paper, we present a design using dual-band passive input and load networks providing transformation and harmonic-tuning for both bands of operation. Our approach avoids active band-switching components in favor of shared passive networks. Similar networks have been used in concurrent multi-band low noise amplifiers (LNA) recently reported [4].

To demonstrate this approach, and to allow comparison with similar single-band designs, a first dual-band harmonic-tuned power amplifier has been implemented.

This amplifier does not require a band-select signal and exhibits performance comparable to a single-band design.

II. THEORY OF OPERATION

A. Class E/F_x Power Amplifiers

The amplifier described in this paper is based on the Class-E/F_{odd} mode of operation, formerly described as a single-band design in [5,6]. The Class-E/F family of power amplifiers operates the active device as a switch. Their tuning network incorporates the switch output capacitance into the load network as in Class-E power amplifiers, but allows improved waveforms by tuning some of the harmonics as in inverse Class-F [7]. Subscripts in the name indicate these tuned harmonics, and the switch is presented with a capacitance at the remaining harmonics. By tuning the fundamental frequency load sufficiently inductive, the E/F amplifier is made to operate in zero voltage switching (ZVS) mode, eliminating losses due to discharge of the output capacitance.

The Class E/F_{odd} tuning produces half-sine voltage waveforms at the switch output. Current waveforms are square-waves with half-cosine waveforms superimposed, with the amplitude of the half-cosine determined by the capacitance parallel to the switch [5]. The Class E/F_{odd} mode was chosen because, unlike Class-E, the impedance of the switch output capacitance and the load conductance are independent parameters, allowing output power at both frequencies to be independent of this capacitance.

B. A Harmonic-Tuned Dual-Band Power Amplifier

Fig. 1 shows the harmonic-tuned dual-band power amplifier topology used for the amplifier reported in this paper. Input and output port impedance is 50Ω . The input network consists of L_{pin} , C_{pin} , T_{in} and L_{sin} . Together, these components convert a 50Ω unbalanced signal source to a balanced signal conjugate matched to the transistor input.

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The output network consists of C_{pout} , L_{sout} , C_{sout} and T_{out} . T_{out} is a 1:1 balun, the magnetizing inductance of which is utilized in the output network tuning. T_{out} , L_{sout} and C_{sout} provide inductive, capacitive and again inductive susceptance as frequency is increased. These three components provide inductive susceptance needed for ZVS operation at each frequency band.

At all odd harmonics of each frequency of operation the network including C_{pout} provides capacitive susceptance that – along with the transistor output capacitance – provides a low impedance path to ground compared to the load resistance[8]. Due to the differential topology, each transistor is presented only its own output capacitance at even harmonics. Thus, this amplifier operates in Class E/ F_{odd} mode at both bands.

Because of the dual-band harmonic-tuning scheme employed in this amplifier, no additional switches or electronically tunable components are needed for correct operation in either band. This promises to reduce the complexity of dual-band power amplifiers, thereby increasing reliability and decreasing cost.

III. CIRCUIT DESIGN

To demonstrate the dual-band harmonic-tuned power amplifier concept, a Class-E/ F_{odd} amplifier using the topology shown in Fig. 1 has been constructed. This amplifier uses two IRFP250N 200, 30 A MOSFETs.

To determine the susceptance needed for ZVS operation at each frequency, two single-band Class E/ F amplifiers are simulated that use an LC parallel tank at the output. The simulated single-band designs and the final dual-band amplifier have a sufficiently large value for C_{pout} in common that presents a low impedance at the first odd harmonic. This is important to allow the inductive susceptance determined from these single-band

simulations to be used in the design of the dual-band load network.

The transistor model used in the simulation consists of an ideal switch with a nonlinear output capacitance fitted to measured data. Component values for the dual-band load network were calculated that provide a good trade-off between losses and bandwidth besides the susceptance needed for ZVS operation at both frequencies. A simulation of the amplifier – assuming quality factors of 120 and 160 for inductors and capacitors respectively – is performed to assure ZVS operation at both design frequencies and reasonable losses. Transistor lead inductances are also included to estimate the ringing waveforms. The simulation predicts an output power of approximately 400W in both bands according to:

$$P_{out} = V_{pk}^2 / (2 \cdot R_{load}) \quad (1)$$

with load resistance $R_{load} = 50 \Omega$ and peak drain voltage $V_{pk} \approx \pi \cdot V_{supply} = 200 \text{ V}$.

The amplifier is constructed on a patterned FR4 board. The output network is implemented using ATC100E and ATC180R series capacitors from American Technical Ceramics. Inductor L_{sout} and transformer T_{out} are both air-core and are wound from magnet ribbon wire and 50 Ω semi-rigid coaxial cable respectively. Holes in the circuit board allow the transistors to be mounted directly to a backside heat sink.

With a load connected, the conductance presented to the transistor drains as measured with an HP4149A impedance analyzer is lower than the expected 2mS.

The reason for this decrease is likely to be the distributed inductance on the circuit board and the non-ideal coupling factor of T_{out} . This decreased load conductance causes the output power to be less than the design goal.

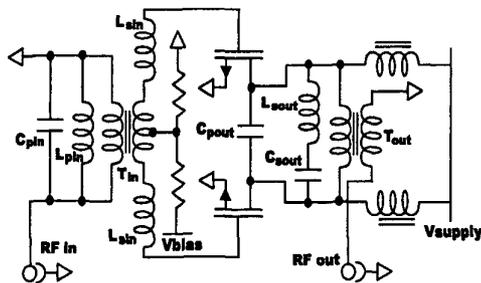


Fig. 1. Topology of the dual-band harmonic-tuned power amplifier reported in this paper.

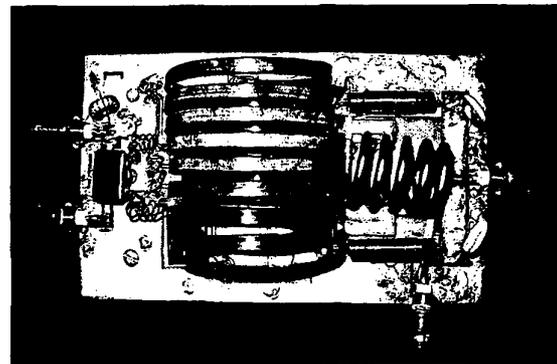


Fig. 2. Photograph of assembled amplifier. Width x length x height approximately 10cm x 18cm x 14cm

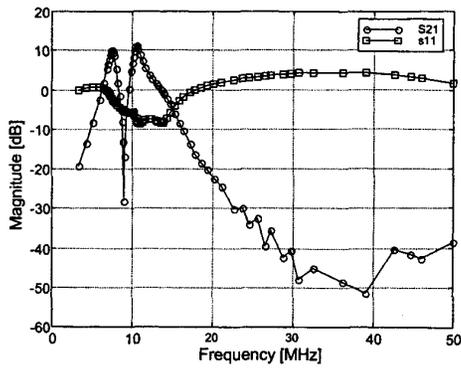


Fig. 3. S-parameters S21 and S11 as a function of frequency for the dual-band power amplifier under Class-A bias with 40mA total supply current, 30V supply voltage and small signal input. The plot shows two gain peaks close to the desired bands of operation.

An ad hoc input network consisting of T_{in} and L_{sin} is used to determine the proper input-matching network. By tuning this network once for each frequency of operation, appropriate characteristics for the matching network in each band may be determined. Component values for a dual-band input network achieving similar transformations at both frequencies simultaneously may then be calculated. A photograph of the prototype amplifier is shown in Fig.2.

IV. PERFORMANCE

The small-signal transfer characteristics of the amplifier are determined first to assure that it displays dual-band gain behavior. Despite the positive value of S11 between 20MHz and 50MHz, the amplifier does not oscillate and is stable at large-signal Class E/F operation.

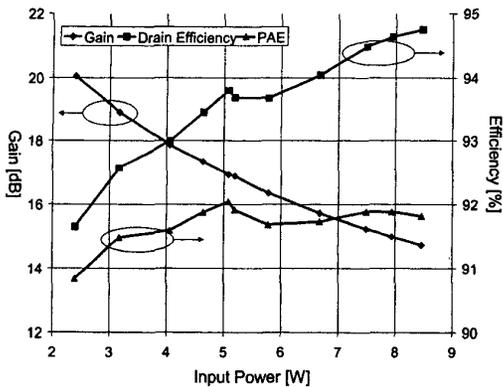


Fig. 4. Gain, Drain Efficiency and PAE versus input power at 7.15MHz running at 58V supply voltage. As expected, gain drops while efficiency improves as the input power is increased

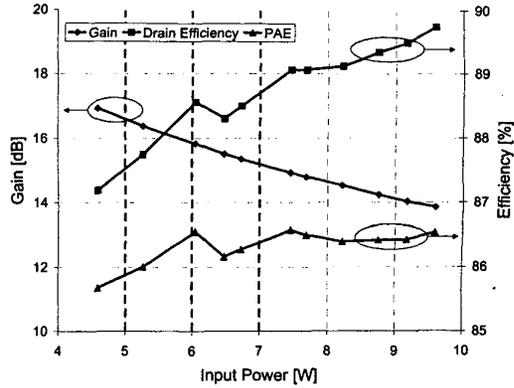


Fig. 5. Gain, Drain Efficiency and PAE versus input power at 10.1MHz running at 58V supply voltage

Figs. 4 and 5 show the measured gain, drain efficiency and PAE versus input power while operating from a 58V supply at 7.15 MHz and 10.1 MHz respectively. As noted earlier, the measured output power is lower than simulated due to parasitic impedance transformation. The bandwidth in both bands was sufficient to allow operation over the 7.0MHz-7.3MHz and the 10.0MHz-10.18MHz bands.

Like any saturated amplifier, the output power may be adjusted by changing the supply voltage. Fig. 6 shows measured power-added efficiency (PAE) at both frequencies as the output power is backed off by up to 6dB.

Figs. 7 and 8 show measured drain voltage waveforms at 7.15MHz and 10.1MHz under full output power.

The amplifier reported here compares well to a similar single-band design. The amplifier exhibits lower gain and higher efficiency than the single-band design reported in

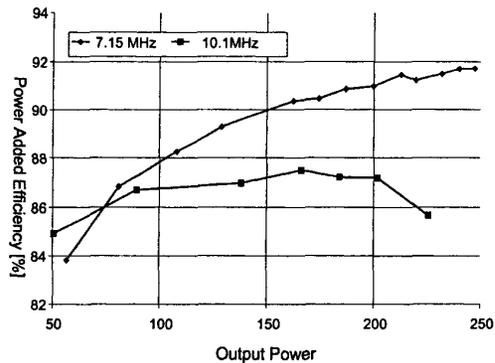


Fig. 6. Power Added Efficiency (PAE) as a function of input power at 7.15MHz and 10.1MHz. The amplifier operates with good efficiency over a 6dB range of output powers

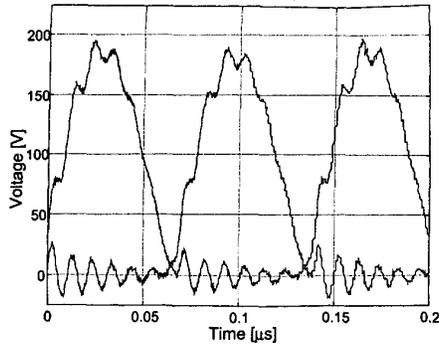


Fig. 7. Measured drain voltage waveforms at 7.15MHz. The ringing is due to transistor package inductance and possibly slight harmonic mistuning.

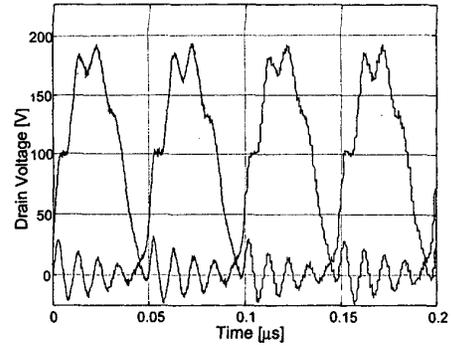


Fig. 8. Measured Drain Voltage Waveforms at 10.1MHz. The waveforms exhibit similar ringing as in operation at 7.15MHz

[5] presumably due to the use of a lower-voltage transistor and larger, higher-Q passives. During operation an external fan has been used to cool the heat sink. This fan may not be necessary as the amplifier remains relatively cool. Table 1 shows a performance summary.

V. CONCLUSION

The first dual-band harmonic-tuned power amplifier is reported that avoids the use of band-selecting active devices or diplexers. The amplifier exhibits performance in each band comparable to a single-band design, in good agreement to simulations in this configuration. The use of dual-band tuned harmonic networks could thus be an alternative to the use of band-switching active signal routing devices.

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	Frequency	
	7.15 MHz	10.1 MHz
Output Power	250 W	225 W
Gain	16 dB	15 dB
PAE	92 %	87 %
Drain Efficiency	94%	90%
Input VSWR	1.7	1.4
Input Power	5.6 W	6.8 W
V_{bias}	2 V	

Table 1. Mid-band performance summary.

REFERENCES

- [1] B. Razavi, "A 900MHz/1.8GHz CMOS Transmitter for Dual-Band Applications," *1998 Symp. VLSI Circuits Dig.*, IEEE 1998, pp. 128-131
- [2] A. Adar, J. DeMoura, H. Balshem, and J. Lott: "A High Efficiency Single Chain GaAs MESFET MMIC Dual Band Power Amplifier for GSM/DCS Handsets," *IEEE Gallium Arsenide Integrated Circuit Symposium, Technical Digest 1998*, Atlanta, Georgia, Nov. 1-4, pp. 69-72
- [3] K. Yamamoto, S. Suzuki, K. Mori, T. Asada, T. Okuda, A. Inoue, T. Miura, K. Chomei, R. Hattori, M. Yamanouchi, S. Teruyuki, "A 3.2-V Operation Single-Chip Dual-Band AlGaAs/GaAs HBT MMIC Power Amplifier with Active Feedback Circuit Technique," *IEEE Journal of Solid-State Circuits*, Vol. 35, No. 8, pp. 1109-1120, Aug 2000
- [4] H. Hashemi, A. Hajimiri, "Concurrent Dual-Band CMOS Low-Noise Amplifiers and Receiver Architectures," *2001 Symp. VLSI Circuits Dig.*, IEEE 2001, pp. 247-250
- [5] S.D. Kee, I. Aoki, D. Rutledge, "7-MHz, 1.1-kW Demonstration of the New E/F(2,odd) Switching Amplifier Class," *IEEE MTT-S Int. Microwave Symp. Dig.*, Vol. 3, Phoenix Arizona, May 20-25 2001, pp. 1505-1508
- [6] I. Aoki, S.D. Kee, D. Rutledge, A. Hajimiri, "A 2.4-GHz, 1.5-W, 2-V fully-integrated CMOS Circular Geometry Active Transformer Power Amplifier," *IEEE Custom Integr. Circ. Conf. Proceedings*, San Diego California, May 6-9 2001, pp. 57-60
- [7] A. Inoue, T. Heima, A. Ohta, R. Hattori, Y. Mitsui, "Analysis of Class-F and inverse Class-F Amplifiers," *IEEE MTT-S Int. Microwave Symp. Dig.*, Boston, MA 2000, pp. 775-777.
- [8] Raab, F.H., "Class-E, Class-C, and Class-F Power Amplifiers Based Upon a Finite Number of Harmonics," *IEEE Trans. Microwave Theory Tech.*, vol. 49, no. 8, pp.1462-1468, Aug. 2001