Stochastic Switching Circuit Synthesis

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***Abstract*—Shannon in his 1938 Master's Thesis demonstrated that any Boolean function can be realized by a switching relay circuit, leading to the development of deterministic digital logic. Here, we replace each classical switch with a probabilistic switch (pswitch). We present algorithms for synthesizing circuits closed with a desired probability, including an algorithm that generates optimal size circuits for any binary fraction. We also introduce a new duality property for series-parallel stochastic switching circuits. Finally, we construct a universal probability generator which maps deterministic inputs to arbitrary probabilistic outputs. Potential applications exist in the analysis and design of stochastic networks in biology and engineering.**

I. Introduction.

In his 1938 Master's Thesis, Claude Shannon discovered a systematic synthesis procedure to generate a switching circuit realizing any given Boolean function [1]. This classical contribution led to the development of modern digital logic design and is at the foundation of our ability to design and manufacture digital circuits with millions of transistors.

Most importantly, Shannon showed how logic (Boolean algebra) can be mapped to physics (relay-based switching circuits). Shannon focused on deterministic variables and functions; by closing a subset of switches, a switching circuit and its associated Boolean function yield a deterministic output.

The natural question is: can we create a similar theory for stochastic variables and functions? Namely, given a desired probability distribution and a set of probabilistic switches (that we call *pswitches*) as building blocks, can we systematically design a switching circuit that realizes a desired probability distribution? Our main contribution is a positive answer to this question for the case where the probability distributions involved are Bernoulli.

Shannon's work focused on the so-called *series-parallel* circuits. A t-terminal circuit is an undirected graph where t nodes are labeled as terminals and where each node is visited by at least one path between each pair of terminals. A circuit is closed if its terminals are connected; otherwise, it is open. A circuit is series-parallel iff each pair of its terminals is: (1) a single edge or (2) a series or parallel combination of two series-parallel circuits.

Shannon's work also focused on deterministic switching circuits, circuits where each switch is associated with a Boolean variable defining whether the switch is closed. We focus on *stochastic switching circuits*, circuits where each pswitch is associated with a Bernoulli random variable defining the (independent) probability that the pswitch is closed.

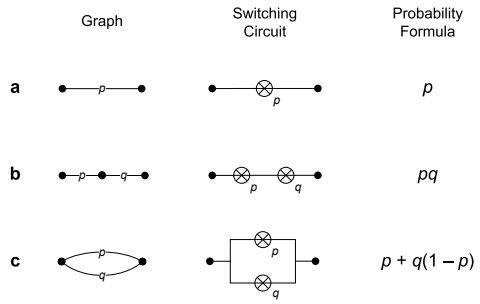

Fig. 1. **Series and Parallel Constructions.** The relationship between a graph and switching circuit is shown. There are only two ways to combine two single-pswitch circuits, both shown here. *(a)* Any circuit can be represented as a single pswitch. *(b)* Series. Only when both switches are closed is a series circuit closed. *(c)* Parallel. Only when both switches are open is a parallel circuit open.

Let $Pr(C)$ represent the probability that a switching ciruit C is closed. Some probability x is realized by C iff $x = Pr(C)$. Connecting the terminals of two switching circuits A and B places them in parallel, such that the new circuit is closed only when at least one of A and B are closed. Connecting one terminal of A with one terminal of B places them in series such that the new circuit is closed only when both A and B are closed.

Now, we will add a single pswitch closed with probability x to an established circuit C. Let $F = Pr(C)$. First, note that only one switching circuit exists with a single pswitch (see Figure 1a). If the pswitch is added in series, then the pswitch and C must both be closed; hence, the new circuit is closed with probability $F' = Fx$ (see Figure 1b). If the pswitch is added in parallel, then the circuit is only open if both the pswitch and C are open; hence, the new circuit is closed with probability $F' = 1 - (1 - x)(1 - F) = (1 - x)F + x$ (see Figure 1c).

In this paper, we shall construct two-terminal stochastic switching circuits where each pswitch is closed with some rational probability. The set of possible pswitch closure probabilities from which a circuit is constructed will be referred to as the *pswitch set* $\mathbf{S}$. We will call a circuit which realizes a Bernoulli distribution using the fewest possible pswitches an *optimal size circuit*. For example, given a pswitch set $\mathbf{S} = \{\frac{1}{2}\}$,

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we can use four pswitches to construct a stochastic switching circuit with probability $P = \frac{11}{16}$ (see Figure 2). No other circuit can be constructed which realizes it with fewer pswitches (proven in Section II), and so it is also an optimal size circuit.

We are now ready to state the main results in the paper:

1) *Synthesizing optimal size switching circuits* which realize Bernoulli distributions. (Sections II, III)
2) *A duality property* allowing for optimality and existence proofs. (Section III)
3) A *universal probability generator* (UPG) which maps n deterministic input bits to all n-bit binary fractions (in increasing order) using only $4n-2$ switches. The UPG can be used to synthesize a circuit realizing any arbitrary deterministic to probabilistic mapping. (Section IV)

Before we continue with the details of our results, we describe some of the related literature. Series-parallel circuits, a subset of switching circuits, have been rigorously analyzed, including their enumeration [2], duality properties [3], and other interesting topological properties [4]. For instance, Duffin found that the absence of a Wheatstone bridge is necessary and sufficient to make a circuit series-parallel [4].

Many duality properties for series-parallel circuits have been studied which are often dependent on the network under study. In resistor networks, the dual yields the inverse equivalent resistance [3]. In logic gate networks, the dual yields a new circuit with an equivalent Boolean formula (De Morgan). In electrical networks, duals are circuits having the same current and voltage formulas [5].

Circuit elements have been traditionally modeled stochastically to assess reliability of components [6]. To produce a system failure, a series connection of components only requires a single failure, whereas a parallel connection of components requires all components to fail. Several physical circuits have also been proposed for designing stochastic systems. For example, Gill suggested how to generate a probability transformation element using sequential memory logic [7].

II. Realizing Binary Fractions.

We first present a simple algorithm that constructs an optimal size circuit for any probability F expressable as an n-bit binary fraction. Specifically, assume without loss of generality that the least significant bit of F is '1'. Then, our algorithm produces an n-pswitch switching circuit that realizes F. We will prove that the resulting circuit is optimal in size.

The B-algorithm: an algorithm for generating circuits that realize binary fractions with pswitch set $\mathbf{S} = \{\frac{1}{2}\}$.

Let F_i be the ith least significant bit of F.

1) Let circuit C_1 be the single-pswitch circuit.
2) For bit F_i, $i = 2$ to n, let circuit C_i be:
   a) If $F_i = 0$, C_1 in series with C_{i-1}, or
   b) If $F_i = 1$, C_1 in parallel with C_{i-1}.

See Figure 2 for an example which realizes $11/16$; namely, we use the B-algorithm with $F = 1011_2$.

Theorem 1: The B-algorithm synthesizes a stochastic switching circuit that is closed with probability F.

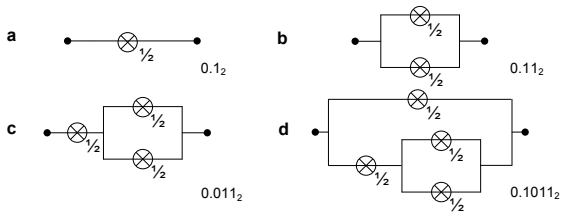

Fig. 2. **Realizing** $F = \frac{11}{16} = 0.1011_2$**.** Progressing from the least-significant to the most-significant bit in the binary representation of F, a pswitch is added in series if '0' and in parallel if '1'. The probability that each circuit is closed as a binary fraction is printed beneath the circuit. The final circuit is optimal in the number of pswitches.

Proof: The proof is by induction on the number of bits in F. The base case is when $F_1 = 1$. We begin with C_1 as the single-pswitch circuit closed with probability 1/2; hence, $Pr(C_1) = 0.1_2$.

Now, suppose that some circuit C_i is closed with probability $Pr(C_i) = 0.\overline{x}$, where $\overline{x}$ is a bit vector. Then, we will show that a pswitch added in series or parallel yields $Pr(C_{i+1}) = 0.0\overline{x}$ or $Pr(C_{i+1}) = 0.1\overline{x}$, respectively. Adding a pswitch in series yields $Pr(C_{i+1}) = Pr(C_i)/2$, namely, a right shift with an addition of '0' in the most significant bit of F. Adding a pswitch in parallel yields $Pr(C_{i+1}) = 1/2 + Pr(C_i)/2$, namely, a right shift with an addition of '1' in the most significant bit of F.

Hence, by using this construction for each of the n bits in F, an n-pswitch circuit that realizes F is synthesized. ■

Note that the B-algorithm only produces a subset of all switching circuits – those synthesizable by adding single pswitches in series or in parallel. We will now prove that even when *all* switching circuits are considered, the B-algorithm is optimal. In the following theorem, we shall prove a general lower bound for pswitch sets. Here, the optimality of the B-algorithm corresponds to the case $q = 2$.

Theorem 2: Let $q \in \mathbf{N}$ be an arbitrary integer. Given $\mathbf{S} = \{1/q, 2/q, ..., (q-1)/q\}$, an optimal size circuit C that realizes $F = a/q^n$, $0 < a < q^n$, using the pswitch set $\mathbf{S}$ requires at least n pswitches.

Proof: We will assume that every optimal size circuit C as defined in the claim of the theorem has size at most $n-1$. Then, we will reach a contradiction. The idea is to show that if C (which realizes $F \in \{0, q-1\}^n$, the base-q representation of the desired probability) of size $n-1$ exists, then eventually we must realize a non-integral probability with zero pswitches, a contradiction.

Here is the idea in the proof. Suppose we have a circuit C_i such that F^i associated with $Pr(C_i)$ has i digits in the alphabet $\{0, \ldots, q-1\}$. We can assume that F^i has a nonzero value in the least significant digit. Then, we will choose some pswitch x in C_i, create two new circuits by opening or closing x, and prove that one of the circuits has probability represented by F^{i-1}, with $i-1$ digits and a nonzero value in its least significant digit. Namely, we can reduce the number of pswitches by one and get a probability value that uses one

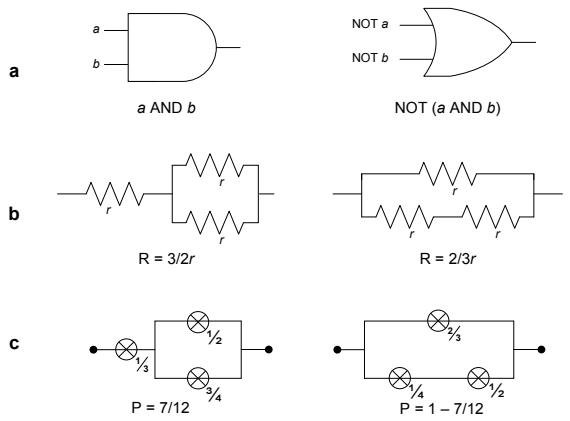

Fig. 3. **Duality.** Duality has played an important role in the analysis of circuits. *(a)* The dual of logic gates, by De Morgan's Law; *(b)* The dual of series-parallel resistor circuits of equal resistance, by Macmahon. Series connections are now parallel, and vice versa; the equivalent resistance coefficients are reciprocals. *(c)* The dual of stochastic series-parallel switching circuits. Each pswitch closed with probability p is closed with $1-p$ in the dual. Note the similarity to the dual of a resistor circuit.

less digit. This process will lead to a contradiction.

By the laws of probability,

$$\begin{aligned} Pr(C_i) = \; & Pr(C_i|x \text{ open})Pr(x \text{ open}) + \\ & Pr(C_i|x \text{ closed})Pr(x \text{ closed}) \\ = \; & a/q^i. \end{aligned} \tag{1}$$

We know that $Pr(x \text{ closed}) \in \mathbf{S}$ and $Pr(x \text{ open}) \in \mathbf{S}$, since $Pr(x \text{ open}) = 1 - Pr(x \text{ closed})$. Both denominators are q, so for some $b, c \in \mathbf{N}$ where $0 < b, c < q-1$,

$$\frac{a}{q^{i-1}} = bPr(C_i|x \text{ open}) + cPr(C_i|x \text{ closed}). \tag{2}$$

Let F^i be the string associated with circuit C_i, where $Pr(C_i) = a/q^i$. F^i has length i and a non-zero least significant digit. Then, by opening or closing some pswitch x in C_i, one of the new circuits is at least $i-1$ digits long. Why? Suppose that both of the new circuit probabilities are $r, s < i-1$ bits long. Then, there exists $b', c' \in \mathbf{N}$ such that $a/q^{i-1} = b'/q^r + c'/q^s$, where each fraction has a nonzero digit in its least significant digit. Then, $a = b'q^{i-r-1} + c'q^{i-s-1} = q^{i-r-1}(b' + c'q^{r-s})$. However, $q|a$, so a has a 0 in its least significant digit, producing a contradiction.

If we assume that there exists C as defined in the claim of the theorem with at least $n-1$ pswitches realizing an F with n digits, then we can apply the above process $n-1$ times and eliminate all the pswitches. However, the resulting probability will still be a fraction, and we reach a contradiction. ∎

III. Duality.

Duality is an important property integral to the study of circuits. De Morgan showed that the dual of a logic gate $A \wedge B$ is $\neg(\neg A \vee \neg B)$ (see Figure 3a). Macmahon showed that the dual of a series-parallel resitor network composed of r-ohm resistors with equivalent resistance $(p/q)r$ has the equivalent resistance $(q/p)r$ [3] (see Figure 3b). We have found that duality exists in series-parallel stochastic switching circuits as well (see Figure 3c). In this context, we will use duality to find algorithms for realizing general probability classes (e.g. all binary fractions).

The construction of a series-parallel circuit C is an ordered sequence of actions – we either synthesize a single-pswitch circuit or combine two series-parallel circuits in series or parallel. To construct the dual of C, we follow the same sequence of actions. However, when a pswitch p is added to C, we add a pswitch $1-p$ to the dual; when a pswitch is added in series, we add it in parallel to the dual (and vice versa).

Hence, the dual of C only exists if C is series-parallel, and if for every pswitch p used in C, the pswitch $1-p$ exists in $\mathbf{S}$. We will now show an important property of the dual of C; it is closed with probability $1 - Pr(C)$.

Theorem 3: Given some stochastic series-parallel circuit C and its dual $\overline{C}$, then $Pr(C) + Pr(\overline{C}) = 1$.

Proof: This is shown using induction on the definition of series-parallel. For the base case, the dual of a single-pswitch circuit with pswitch p is the single-pswitch circuit with pswitch $1-p$. Now, suppose that the dual of a stochastic circuit C is closed with probability $1 - Pr(C)$. Adding a second series-parallel circuit C' in series with C to form C_s yields $Pr(C_s) = Pr(C)Pr(C')$. Adding C' in parallel to the dual of C to form $\overline{C_p}$ yields $Pr(\overline{C_p}) = 1-(1-(1-Pr(C')))(1-(1-Pr(C))) = 1 - Pr(C)Pr(C') = 1 - Pr(C_s)$. The other direction is similar. ∎

This duality property is a powerful tool for analyzing stochastic switching circuits. Suppose that for every pswitch p in a circuit C, a pswitch $1-p$ is in $\mathbf{S}$. As follows, the duality property can be used to prove which classes of probabilities can be realized by all series-parallel circuits given $\mathbf{S}$.

Theorem 4: $\mathbf{S} = \{\frac{1}{2}\}$. All $Pr(C^n) = \frac{a}{2^n}$, $0 < a < 2^n$, (i.e. all n-bit binary fractions) can be realized with n pswitches.

Proof: Suppose that all $a/2^n$ can be realized. Now, add a pswitch in series with each circuit, realizing all $(1/2)(a/2^n) = a/2^{n+1}$, $0 < a < 2^n$. Then, by the duality theorem, the other half of the numerators, $2^n < a < 2^{n+1}$, also can be realized (by adding 1/2 in parallel). Hence, all $(n+1)$-bit binary fractions can be realized with n pswitches (see Figure 4a). ∎

Theorem 5: $\mathbf{S} = \{\frac{1}{3}, \frac{2}{3}\}$. All $Pr(C^n) = \frac{a}{3^n}$, $0 < a < 3^n$, (i.e. all n-trit ternary fractions) can be realized with n pswitches.

Proof: Suppose that all $a/3^n$, $0 < a < 3^n$, can be realized. Now, add a $1/3$ pswitch in series with each circuit, realing all $a/3^{n+1}$, $0 < a < 3^n$. By the duality theorem, $2 * 3^n < a < 3^{n+1}$ can also be realized (by adding 2/3 in parallel). The evens of $3^n < a < 2 * 3^n$ can be realized by adding $2/3$ in series, and the duality theorem ensures that the odds can be synthesized by adding $1/3$ in parallel. Hence, all

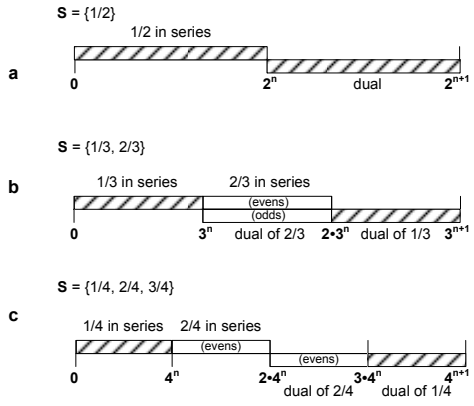

Fig. 4. **Expressive Power.** Here, we are given an initial pswitch set $\mathbf{S}$ and that we can realize all a/q^n, $0 \leq a < q^n$, for some $q \in \mathbf{N}$. Using duality, we show how to realize all b/q^{n+1}, $0 < b < q^{n+1}$ by adding a single pswitch. The numerator b is shown on each number line along with which pswitch to add to realize it. *(a)* All $a/2^n$ can be synthesized using n pswitches. *(b)* All $a/3^n$ can be synthesized using n pswitches. *(c)* All $a/4^n$ can be synthesized using $n+1$ pswitches. Note that using n pswitches we can only generate the evens in the middle half. To generate some odd numerator o, place a $1/2$ pswitch in series with $2o$, using $n+1$ pswitches (if $o > 2 * 4^n$, then use duality).

n-trit ternary fractions can be realized with n pswitches (see Figure 4b). ■

Note that an optimal algorithm for realizing any fraction can be obtained from the proof above. From theorem 2 ($q = 3$), a minimum of n pswitches is required to realize all n-trit ternary fractions; hence, the strategy in the proof is optimal. Given a desired probability F and $\mathbf{S} = \{1/3, 2/3\}$, then the algorithm is:

1) Begin with an open circuit.
2) If $F = 1$, then halt. Otherwise, let a be the numerator of F.
3) Add a pswitch:
   a) If $a < 3^n$, add a 1/3 pswitch in series. (Let $p = 1/3$.)
   b) If $3^n < a < 2 * 3^n$, then:
      i) If a is odd, add a 1/3 pswitch in parallel. (Let $p = 1/3$.)
      ii) If a is even, add a 2/3 pswitch in series. (Let $p = 2/3$.)
   c) If $2 * 3^n < a < 3^{n+1}$, add a 2/3 pswitch in parallel. (Let $p = 2/3$.)
4) Find the new desired probability:
   a) If a pswitch was added in series, let $F' = F/p$.
   b) If a pswitch was added in parallel, let $F' = \frac{F-p}{1-p}$.
5) Let F = F'. Goto 2.

Now we take a brief diversion and show that this trend of n-pswitch circuits realizing all a/q^n cannot continue. For $q > 3$, prime numerators exist between the fractions obtainable by adding two $(q-1)/q$ in series and two $1/q$ in parallel. Since these primes cannot be realized, then all a/q^n cannot be generated for arbitrary n.

Theorem 6: No pswitch set containing all a/q, $0 < a < q$, for any $q > 3$, can realize all $Pr(C^n) = \frac{b}{q^n}$, $0 < b < q^n$.

Proof: We shall show that a prime numerator exists for each denominator q^2 which cannot be realized, for all $q > 3$. If a pswitch is added in series to the single-pswitch circuit, then the resulting numerator is composite (for $a > q - 1$). If a pswitch is added in parallel, then the smallest numerator possible is realized by placing $\frac{1}{q}$ in parallel with $\frac{1}{q}$, yielding a numerator of $2q - 1$. Hence, the range of numerators for which only composite numbers can be generated is $q \leq a < 2q-1$. By Bertrand's Postulate, there exists at least one prime between q and $2q - 2$, for $q > 3$; hence, a prime numerator always exists within this range that cannot be generated.

The set of all switching circuits is equivalent to the series-parallel set for fewer than four pswitches. Hence, this proof holds for all switching circuits. ■

From the theorem, circuits with $\mathbf{S} = \{1/4, 2/4, 3/4\}$ and $F = a/4^n$ cannot generate all a with fewer than $n + 1$ pswitches. In the following theorem, we will show that at most, $2n - 1$ pswitches are required.

Theorem 7: $\mathbf{S} = \{\frac{1}{4}, \frac{2}{4}, \frac{3}{4}\}$. All $Pr(C^n) = \frac{a}{4^n}$, $0 < a < 4^n$ can be realized with x pswitches, where $n \leq x < 2n$.

Proof: Suppose that all $a/4^n$, $0 < a < 4^n$, can be realized. Now, by adding a $1/4$ pswitch in series, the lower quadrants of $a/4^{n+1}$ can be synthesized. By duality, the upper quadrant is also synthesized. By adding $2/4$ in series or parallel, all even numerators can be synthesized. Now, any remaining odd numerator o can be generated by constructing the circuit for $2o/4^n$ and adding a $1/2$ pswitch in series. Each stage requires at most two switches with the exception of the first, and so all $a/4^n$, $0 < a < 4^n$ can be realized by at most $2n - 1$ pswitches (see Figure 4c). ■

The previous proof suggests that many stages may require two switches. However, in practice often no more than $n + 1$ pswitches are required, provided that certain prime numerators are not synthesized. As an example, $5/16$ cannot be realized with two pswitches (theorem 6); it can be realized with three.

If two switches are used to synthesize each of the odd numerators suggested above, then it can be shown by induction that $2n - 1$ pswitches are required to realize the fraction $(\sum_{i=0}^{n-1} 4^i)/4^n$ for any $n > 0$.

IV. A Universal Probability Generator

We have shown how to minimally realize any binary fraction. Now, we will synthesize a circuit which can realize a "probabilistic truth table" – a map assigning deterministic inputs to probability values.

We define a *universal probability generator* (UPG) to be a circuit which maps n deterministic input bits to all 2^n n-bit binary fractions in increasing order (e.g. for $n = 3$, figure 5a). This can be easily accomplished using an exponential number of switches; we simply construct each of the 2^n probabilistic circuits separately then uniquely select them with deterministic switches.

Here, we propose two constructions which require only $4n-2$ switches. The first construction requires only n pswitches, the fewest possible; the second is monotonic in the value of its deterministic variables. In this section, all pswitches will be closed with probability $1/2$.

Theorem 8: The following recursive construction will synthesize an n-bit deterministic input UPG circuit C_n using

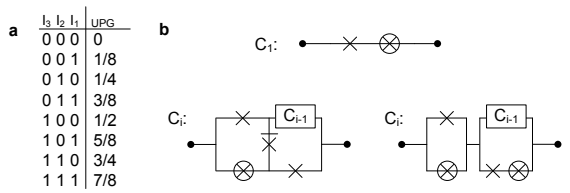

Fig. 5. **A Universal Probability Generator.** Here, we show the construction of a circuit which maps deterministic inputs to probabilities. *(a)* The mappings for a UPG with three deterministic input bits. *(b)* C_1 is two switches in series. Each recursive circuit stage requires an additional four switches. Note that a single pswitch added at each stage is minimal.

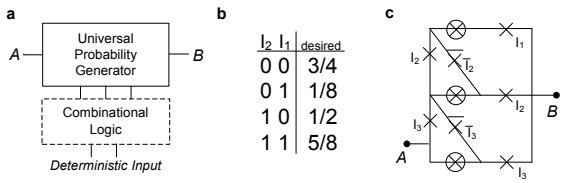

Fig. 6. **Realizing a Probabilistic Truth Table.** As an example, we will synthesize a UPG and combinational logic block which satisfies a given mapping between deterministic inputs and probabilities. *(a)* Combinational logic allows arbitrary mappings to be achieved. *(b)* The desired truth table, mapping two input bits to probabilities. *(c)* A UPG construction which can realize any 3-bit binary fraction.

$4n-2$ switches:

1) Given a deterministic input x, let C_1 be a switch and pswitch in series as in figure 5b.
2) To synthesize circuit C_i, substitute C_{i-1} into the template for C_i given in figure 5b.
3) Let all deterministic switches added for circuit C_i be closed (unless negated) iff the ith bit from the least significant input bit is '0'.

Proof: For C_1, if the deterministic switch is open, we realize 0/2; if it is closed, we realize 1/2. Hence, we realize all 1-bit binary fractions.

Suppose that we can generate all $(i-1)$-bit binary fractions with circuit C_{i-1}. Then, we shall show we can generate all i-bit binary fractions with circuit C_i. If the ith least significant input bit is '0', then the deterministic switches added for C_i are open (unless negated). Hence, in both constructions in figure 5b, a $1/2$ pswitch is connected in series with C_{i-1}. This yields the first half of the new numerators, since $a/2^n * 1/2 = a/2^{n+1}$. Similarly, if the ith bit is '1', then a $1/2$ pswitch is connected in parallel with C_{i-1}, yielding the second half of the new numerators, since $1-1/2*(1-a/2^n) = a/2^{n+1} + 1/2$. Hence, every i-bit binary fraction is generated for each recursive step, mapping each deterministic input x to $x/2^n$.

In both constructions, four switches are required for each C_i, excluding C_1 for which only two are required. Hence, after $n-1$ recursions and the base case, we can generate 2^n probabilities with $4n-2$ switches. ■

In addition to these two constructions, also note that the dual of the series-parallel construction (the right template in figure 5b) is a valid UPG circuit. By the duality theorem, this construction will realize all $1 - Pr(C_n)$, yielding again 2^n unique n-bit binary fractions. Also, note that a parallel circuit can also be used for C_1; if used, this would map each deterministic input x to $(x+1)/2^n$, generating an always-closed circuit $(2^n/2^n)$ rather than an always-open circuit $(0/2^n)$.

After generating this UPG, deterministic inputs yield probabilities in increasing order. To create an arbitrary mapping, a combinational logic block can be added (see Figure 6a) which maps the desired deterministic inputs to the UPG deterministic inputs using classical logic synthesis.

We will now provide an example of constructing a circuit which realizes the truth table in figure 6b. First, since 3-bit binary fractions must be realized by the circuit, we build a 3-bit deterministic input UPG by following the construction rules (see Figure 6c). The UPG maps three deterministic inputs to probabilities as shown in figure 5a. Hence, we will add combinational logic to map the circuit deterministic inputs I to the UPG deterministic inputs I'. This can be accomplished using the following Boolean formulas – $I'_1 : I_1$, $I'_2 : \neg I_1 \wedge \neg I_2$, and $I'_3 : \neg I_1 \vee I_2$.

Note that the mentioned probabilistic "truth table" also can be interpreted as a discrete probability distribution. By only using pswitches and deterministic switches, by the procedure above any discrete probability distribution of binary fractions can be generated.

V. Conclusions

In this paper, we introduced probabilistic switches as an extension to classical deterministic switches. We showed that a random variable, particularly a Bernoulli random variable, can be associated with each pswitch, allowing circuits to realize probability distributions. We found an algorithm to generate the minimal circuit for any binary or trinary fraction. We showed how duality extends from resistor networks and logic gates to the pswitch realm, using it to prove existence results. Finally, we constructed a linear-size universal probability generator, capable of mapping any set of deterministic inputs to unique probabilistic outputs.

Extending the work to find algorithms for more general random variables and multiple terminals would be useful for applied work, particularly in modeling stochastic events in biology and engineering.

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