Sealing of Micromachined Cavities Using Chemical Vapor Deposition Methods: Characterization and Optimization

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***Abstract*—This paper presents results of a systematic investigation to characterize the sealing of micromachined cavities using chemical vapor deposition (CVD) methods. We have designed and fabricated a large number and variety of surface-micromachined test structures with different etch-channel dimensions. Each cavity is then subjected to a number of sequential CVD deposition steps with incremental thickness until the cavity is successfully sealed. At etch deposition interval, the sealing status of every test structure is experimentally obtained and the percentage of structures that are sealed is recorded. Four CVD sealing materials have been incorporated in our studies: LPCVD silicon nitride, LPCVD polycrystalline silicon (polysilicon), LPCVD phosphosilicate glass (PSG), and PECVD silicon nitride. The minimum CVD deposition thickness that is required to successfully seal a microstructure is obtained for the first time. For a typical Type-1 test structure that has eight etch channels—each 10 μm long, 4 μm wide, and 0.42 μm tall—the minimum required thickness (normalized with respect to the height of etch channels) is 0.67 for LPCVD silicon nitride, 0.62 for LPCVD polysilicon, 4.5 for LPCVD PSG, and 5.2 for PECVD nitride. LPCVD silicon nitride and polysilicon are the most efficient sealing materials. Sealing results with respect to etch-channel dimensions (length and width) are evaluated (within the range of current design). When LPCVD silicon nitride is used as the sealing material, test structures with the longest (38 μm) and widest (16 μm) etch channels exhibit the highest probability of sealing. Cavities with a reduced number of etch channels seal more easily. For LPCVD PSG sealing, on the other hand, the sealing performance improves with decreasing width but is not affected by length of etch channels. [281]**

I. Introduction

SEALED micro cavities are crucial components in many micromachined sensors and actuators. These cavities are typically formed using sacrificial-layer etching techniques and are sealed using a variety of methods including chemical vapor deposition of thin films (under either low pressure or atmosphere pressure) [1], [2], [4]–[8], thermal oxidation [5], electron-beam evaporation [9], [10], metal evaporation [11], [12], wafer-to-wafer bonding [13]–[15], and solder glass fritting [16].

Low-pressure encapsulation and packaging is important for many MEMS applications. It can be applied to reduce air damping for electromechanical resonators and filters [1], to establish pressure-measurement [2], [4], or to produce vacuum electronics components [10], [14], [12]. Chemical vapor deposition methods are frequently employed to produce vacuum-sealed cavities with pressure below a few hundred millitorr. Both low pressure CVD (LPCVD) and plasma enhanced CVD (PECVD) techniques are available. The schematic diagram of a cavity is shown in Fig. 1(a); it contains a suspended diaphragm and connects to a number of etch channels. In a CVD chamber, material deposition occurs on both the bottom and top surfaces of the diaphragm and also on the substrate. Below the diaphragm, two opposite deposition fronts, one originating from the diaphragm and one from the substrate, approach each other during the deposition process. The typical profile of deposited materials at the point of sealing is shown in Fig. 1(b), in conjunction with simulation results obtained using a Stanford Profile Emulator and Deposition in IC Engineering—SPEEDIE [17]. The thickness of deposited material at the opening of etch channels can be more pronounced than the nominal deposition thickness in open areas on top of the diaphragm. This phenomenon is attributed to the increased space angle near the opening. These two fronts will eventually meet near the open end of the etch channel and form chemical bonding, thus establishing a permanent hermetic seal that isolates the cavity with the ambient. Both experimental measurement and theoretical models exist to confirm the general contour of the deposited material [17].

For each individual cavity, sealing occurs when the nominal thickness of deposited material (measured in an open area on top of a substrate) reaches a threshold value. This threshold thickness can be influenced by design parameters (notably, the dimensions of etch channels), by structural and CVD materials, and by CVD conditions (e.g., temperature, pressure, and flux). In order to successfully implement the sealing process in the fabrication of MEMS devices, it is critical to 1) predict the threshold thickness based on dimensions and sealing materials, and 2) to minimize the threshold-thickness requirement by implementing efficient material and design.

A small threshold thickness is generally desirable. In many MEMS devices, the CVD materials used for sealing become an integral part of the cavity diaphragm and contribute significantly to its overall thickness. The thickness of the CVD material, therefore, can significantly influence the device performance. For a surface-micromachined pressure sensor [4], a smaller diaphragm thickness generally increases the sensitivity. The thickness of deposited sealing material in-

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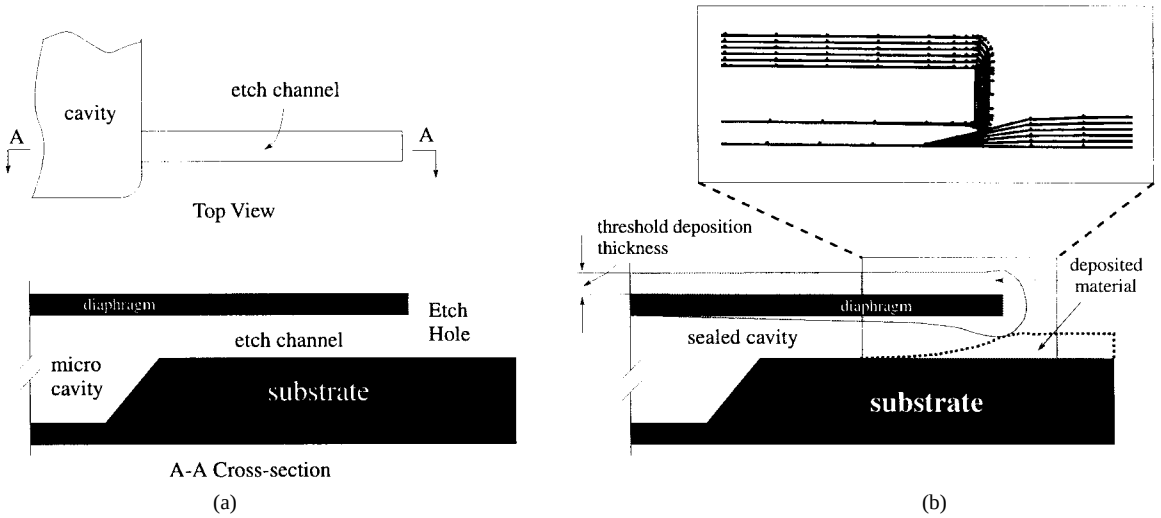

Fig. 1. (a) Schematic views of an as-fabricated test structure and an associated etch channel and (b) profile of deposited materials when sealing occurs. The insert is a result of computer simulation of LPCVD silicon nitride deposition using a Stanford Profile Emulator and Deposition in IC Engineering—SPEEDIE, with the surface sticking coefficient being 0.5.

evitably increases the thickness of the diaphragm and reduces the device sensitivity to ambient pressure. A thin CVD deposition generally would translate into increased sensitivity to pressure variations. A fluidic shear-stress sensor [18] based on thermal-transfer principles offers another example. In such a sensor, a heated element is located on top of a suspended diaphragm. In order to reduce the conductive heat loss from the heated element to the substrate, it is necessary to reduce the thickness of the diaphragm and increase the conductive thermal resistance. In both cases, detailed knowledge about the threshold thickness will enable a flexible process control while satisfying performance needs.

Information on the threshold deposition thickness with respect to cavity geometry and sealing-deposition materials is currently missing. Although many MEMS devices containing CVD-sealed microcavities have been developed, the sealing process itself has never been systematically studied. As a result, sealing processes are conducted based on empirical data, allowing large margins for surety.

Difficulties arise both in experimental measurements and in computational simulation. On one hand, there is no established technology available for *in-situ*, continuous monitoring of the sealing status of a cavity during high-temperature CVD processes. On the other hand, existing computer models cannot accurately predict deposition profile and sealing conditions of surface microcavities. Although computational models and tools have been developed and proven successful for predicting step coverage on relatively simple geometries (e.g., isolation trenches or vias in integrated circuit processes) [19]–[21], complex three-dimensional structures encountered in MEMS pose new challenges. The simulation program, SPEEDIE, has not been able to successfully predict the deposition thickness required for sealing. It also does not accommodate all the sealing materials under this study. More investigation such as the data presented in this paper may help the development of CAD programs with better accuracy.

In this paper, we present results of a first systematic study on the behavior of microcavity sealing. It is conducted by depositing CVD materials onto surface-micromachined test structures at controlled, incremental thickness and monitoring the sealing status of all test structures at every thickness interval. Test structures with systematically varying dimensions yield quantitative evaluation of sealing results with respect to etch-channel dimensions (including length, width, quantity, and distribution). Results on sealing individual structures by different materials provide a direct comparison of their effectiveness.

II. Approach of Studies

In this study we have concentrated mainly on an experimental approach which provides direct and reliable results. A large variety and quantity of test structures with systematically varying geometric parameters are developed using a process flow described in Section IV. CVD materials are deposited on wafers that contain test structures. Important CVD deposition parameters are summarized in Table I. At the end of each CVD deposition interval, we record the sealing results for all individual test structures. This deposition-measurement cycle is repeated for several times until a majority of cavities are sealed.

Shown in Fig. 2 is the schematic of a test structure (Type 1). It contains a cavity and associated etch channels that radiate from the perimeter of the cavity. The common feature among all test structures is a square-shaped cavity that is 200 μm long on each side and approximately 1.5 μm deep. In addition to Type-1 structure, three other types of test structures have been explored; their configurations and related sealing results are discussed in Section IV-F.

Etch channels are filled with sacrificial-layer material that bridges the interior of a cavity with the etch-hole opening, allowing the sacrificial-layer material inside the cavity to be removed. Because of their small quantity and width, etch channels in Type-1 structures exert minimum effects on the mechanical integrity of the diaphragms. The longitudinal extent of etch channels can generally reduce the amount

TABLE I
CVD PROCESSING PARAMETERS FOR VARIOUS SEALING MATERIALS

Material	flow ratio	pressure(mTorr)	temp.(°C)/power(W)
LPCVD nitride	NH_3/DCS~3/1	330	820/ N.A.
LPCVD Polysilicon	Silane(SiH4)	220	620/N.A.
LPCVD PSG	$O_2/SiH_4/PH_3$ ~6:1:2	150	450/N.A.
PECVD nitride	NH_3/SiH_4~7:3	400	300/50

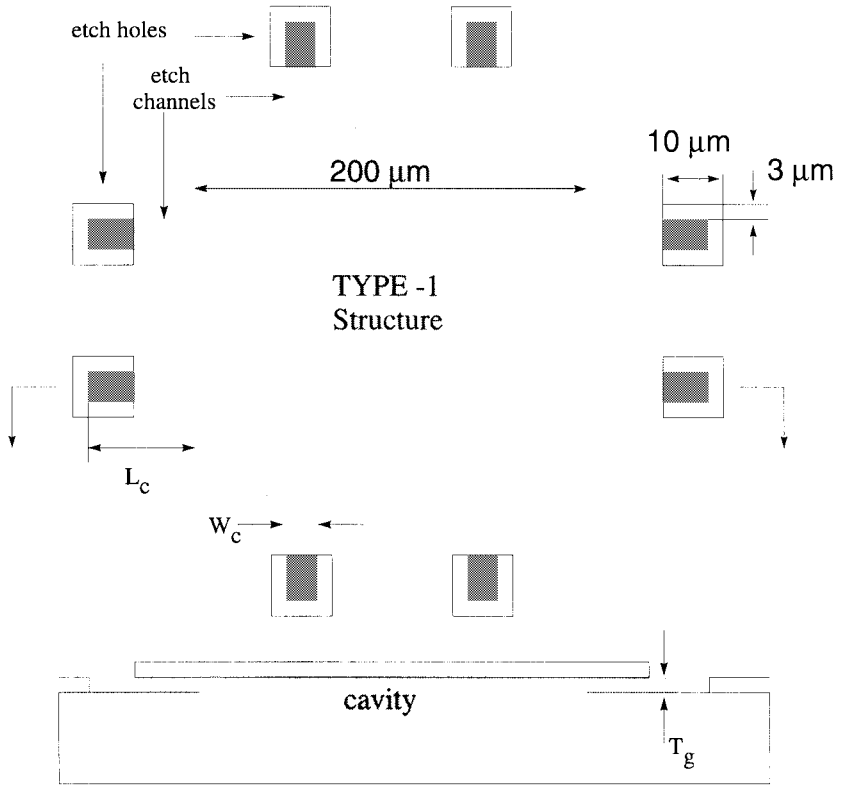

Fig. 2. Schematic configurations of a Type-1 test structure.

of chemical vapor deposition on interior surfaces of cavities.

The quantities and dimensions of etch channels vary. Test structures in our experiments have different numbers (8, 10, and 12) of etching channels with various channel widths (4, 6, 8, 10, and 16 μm) and lengths (8, 18, and 38 μm). The dimensions of etch holes are standardized: their length (in longitudinal direction of etch channels) is 10 μm; their width is always 6 μm more than the widths of corresponding etching channels.

Since our current study is based on statistical data, a large number of samples are generated. A 4-in-diameter silicon wafer contains 48 dies, each occupying an area of 1×1 cm^2 and containing 126 different test structures (72 are of Type 1). The sample space of each unique test structure is therefore 48 on each wafer. In our experiments, each wafer undergoes four to six runs of incremental CVD deposition until a majority of Type-1 structures are sealed. At the end of each deposition, wafers are removed from the deposition chamber and cooled. We examine all test structures (totalling $126 \times 48 = 6048$) using an optical microscope to determine their sealing status. The number of sealed cavities for each test structure is obtained.

Type-1 test structures are the focus of our studies because these have been most commonly used in previously published work [2]–[4]. In addition, Type-1 structures yield robust and complete sealing results; experiments show that these structures have been successfully sealed by all four CVD deposition materials. Results obtained from three other types of structures are summarized in Section V.F. Sealing results for other structure types are less uniform. While certain individual structures seal as easily as Type-1 structures, some are proven to be inefficient or vulnerable to process damages.

Major objectives of our work are to systematically characterize the sealing process with respect to the following design and process parameters:

1) CVD sealing materials;
2) CVD deposition thickness with respect to etch-channel heights;
3) test-structure dimensions including etch-channel length and width;

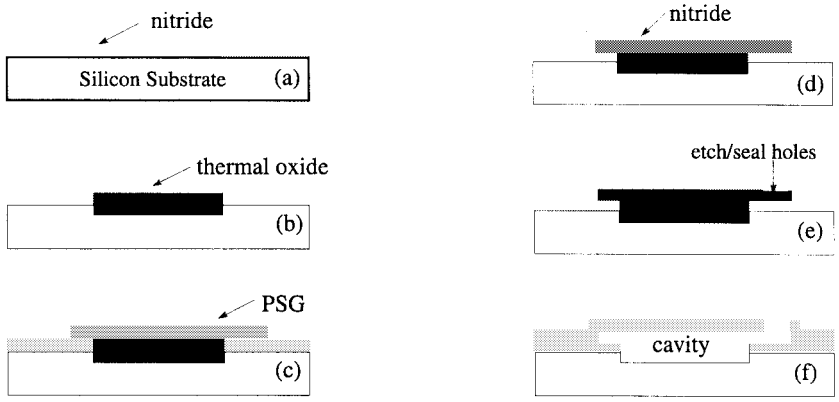

Fig. 3. Major fabrication steps for microcavity structures.

4) the quantities of etch channels associated with individual cavities.

Material deposition on the interior surfaces of a cavity is not characterized in our studies.

The thickness of the deposited sealing material inside the cavity is also a major concern for device performance. Studies by Lin *et al.* have confirmed the thickness of internally deposited silicon nitride material as being 1500 Å for the micromechanical filters [22] when the overall deposition thickness is 2 μm. In this current work, however, the internal deposition is not the focus; it will be investigated in future studies.

III. Standard Fabrication Process

The overall fabrication process for all test structures is illustrated in Fig. 3. We first deposit 300 nm of low-stress LPCVD silicon nitride onto 4-in-diameter silicon wafers. This nitride layer is patterned and plasma-etched to define cavity-well regions (each 200 $\times$ 200 μm^2 in area) inside which the substrate silicon material is exposed. In order to achieve high yield in test structures, over-etch (10%) is applied to account for wafer-scale nonuniformity of etch rates. As a result, silicon surfaces may be etched slightly in certain areas of a wafer.

The ideal depth of each well, measured from the silicon nitride top surface to the exposed silicon surface at the bottom, is 0.7 μm. This depth is reached by etching silicon surfaces in an HNA etchant (hydrofluoric acid : nitric acid : acetic acid = 1 : 3 : 8) that exhibit a slow etch rate of 0.5 μm per minute. (Etching on the silicon nitride material is negligible.) This measure ensures that when a controlled thickness (1.3 μm) of silicon dioxide is selectively regrown within the well region in the next process step, the resultant oxide surface will line up with the silicon nitride surface exactly, minimizing topology variation.

A silicon dioxide layer is then grown using steam-assisted thermal oxidation at 1050 °C for 4 h. As the oxide forms, the interface of silicon and silicon-dioxide moves below the starting silicon surface that has resulted after HNA etch. At the end of this oxidation process, the thickness of oxide grown below the starting silicon surface accounts for approximately 44% of the total oxide thickness (1.3 μm). The silicon nitride layer prevents diffusion of oxygen; as a result, there is no oxide growth underneath the silicon nitride layer. Along the perimeter of each cavity, a small amount of lateral thermal oxidation will occur at the interface of the silicon substrate and silicon nitride, resulting in so-called "bird's beak" structures. Topological variation is created, but its effect on the sealing performance is small and beyond the scope of the current study.

LPCVD phosphosilicate glass is then deposited and patterned. Part of the patterned PSG layer overlaps with the cavity well while the rest forms etch channels outside of the cavity. Wafers are annealed in nitrogen ambient at 950 °C for one hour in order to 1) reflow PSG and smooth out patterned edges, and 2) densify the PSG material. The most frequently used PSG thickness is 220 nm (measured after the high-temperature reflow). In order to study the sealing behavior created by varying etch-channel heights, wafers each with a different PSG thickness must be prepared. In our experiments, three representative sacrificial-layer thicknesses (280, 480, and 720 nm) have been used.

A low-stress silicon nitride film (800 nm) is deposited as the diaphragm material; it is patterned and plasma-etched to create etching holes and expose the underlying PSG layer. Using concentrated (49%) hydrofluoric (HF) solution, the PSG and the thermal oxide inside the well can be completely removed within 20 min. HF also etches silicon nitride at a typical etch rate of 50 Å per minute. During the sacrificial layer etch, a portion of the silicon nitride material will be consumed, which results in a change of the etch-channel geometric parameters including the gap height. The *modified etching-channel gap height* is the original PSG thickness plus an expansion, which doubles the thickness of silicon nitride that is consumed on both the diaphragm and the substrate during the 20-min etch period (Fig. 4).

Wafers are then subjected to a thorough rinsing in deionized (DI) water for 60 min to allow HF to diffuse out of the cavity. The DI water content within each cavity is then removed by spin drying at 5 Kr/min. There was no single case in which the diaphragm stuck to the bottom of the cavity; the roughness of the cavity bottom is believed to be the reason for this fact.

Finally, wafers are baked at 400 °C in nitrogen ambient for 10 min to remove residual moisture inside the cavities. Sealing depositions are then performed over these wafers immediately

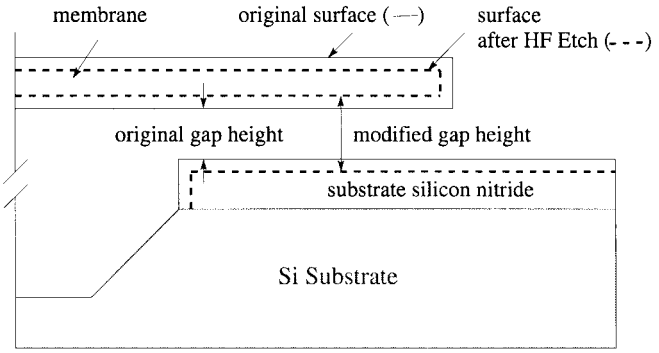

Fig. 4. Schematic diagram showing the original and modified etch-channel geometry before and after the sacrificial-layer removal.

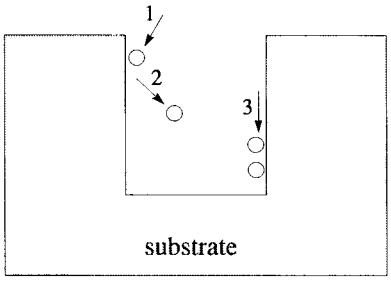

Fig. 5. Schematic diagram showing molecule transport and deposition mechanisms (using a simple 2-D trench model): 1: direct deposition, 2: surface re-emission, and 3: surface diffusion.

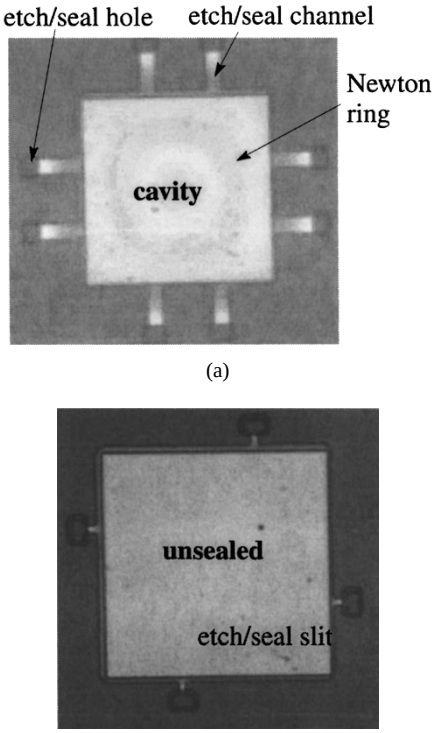

Fig. 6. Optical micrographs of two Type-1 test structures: (a) a sealed Type-1 structure (with eight etch channels), (b) an unsealed structure (with four etch channels). Newton rings are clearly seen on the diaphragm of the sealed cavity.

after the drying process (see Table I for process parameters). In a CVD system with pressure ranging form 50 to 300 mTorr, gas diffusion is not important because the mean-free-path lengths (λ) of gas molecules are larger than the dimensions of microcavities. The mean-free-path length can be estimated using

$$\lambda = \frac{kT}{\sqrt{2}\pi d^2 P} \tag{1}$$

where d is the radius of rigid molecule spheres, P and T are the pressure and temperature of the system, respectively, and k is Boltzmann's constant. If we assume that the average d for air molecules is 3.5 Å, λ is equal to 190 μm at temperature of 300 K and pressure of 300 mTorr (40 N/m^2); if the deposition is conducted at 900 K, λ increases to 570 μm. Typical length scale of the etch-hole opening, however, ranges below 50 μm.

Under these processing conditions, the three-dimensional profile of the deposited material is governed by the complex interaction of three molecular-transport mechanisms (Fig. 5): direct deposition, surface re-emission, and surface diffusion. Indirect deposition from re-emission and surface diffusion allows precursors to reach regions that are less accessible to direct molecule flux.

Here, we only use one standard deposition recipe for each sealing material. Parameters governing molecular transport are therefore fixed. Studies by others have found that the deposition conditions (total flux and temperature) will influence the step coverage and therefore the sealing performance.

When a cavity is sealed under vacuum, the atmospheric pressure will cause the diaphragm to bend; subsequently, interference patterns (Newton rings) can be observed over the diaphragm. The presence of the Newton ring is thus an indication of complete sealing. Pictures of sealed and unsealed structures are shown in Fig. 6; the cavity shown in (a) is sealed while that shown in (b) is unsealed.

IV. Results and Discussion

A. Nomenclature

To facilitate the discussion of experimental results, we define two terms: *sealing factor* and *normalized thickness*.

A *sealing factor*, denoted *SF*, is the number of sealed cavities normalized by the total number of such cavities on a single wafer (48 in our experiments). After each CVD deposition step, an SF is experimentally obtained for each kind of test structure by counting the number of sealed cavities on a wafer. An *SF* of 1 indicates that all 48 cavities are successfully sealed. Although the sealing status of each individual cavity is binary in nature (SF equals either 0 or 1), nonuniformity of cavity geometry and deposition thickness at the wafer scale can cause the overall sealing factor to fall between 0 and 1. For example, an SF of 0.5 indicates that half the 48 cavities are sealed; another interpretation is that a single cavity has a 50% probability of being sealed.

Cavities with different etch-channel heights require varying threshold deposition thicknesses to become sealed. To study effects due to gap heights, we define a normalized thickness t_n as the cumulative CVD deposition thickness on a certain wafer normalized by the *modified etching-channel gap height*. A minimum t_n to achieve complete sealing is denoted $t_{n,\min}$.

B. Uncertainties in Data

A relationship between SF and t_n is obtained for each structure. In practice, it is impossible to obtain a large number of closely spaced data points and determine the exact deposition thickness at which sealing occurs. There are uncertainties involved in the $t_{n,\min}$ measurement. Errors are introduced through two major sources: 1) finite deposition thickness steps and 2) wafer-scale nonuniformities in patterning and deposition. We speculate that sequential deposition-measurement cycles may alter the deposition characteristics. To observe the sealing status, wafers must be removed from the CVD environment, cooled, and reintroduced into the high-temperature tube after measurement. To avoid excessive thermal cycling and potential contamination, the number of deposition steps performed on a given wafer is generally limited to below six. This finite deposition thickness step causes an inherent error margin associated with $t_{n,\min}$ measurement.

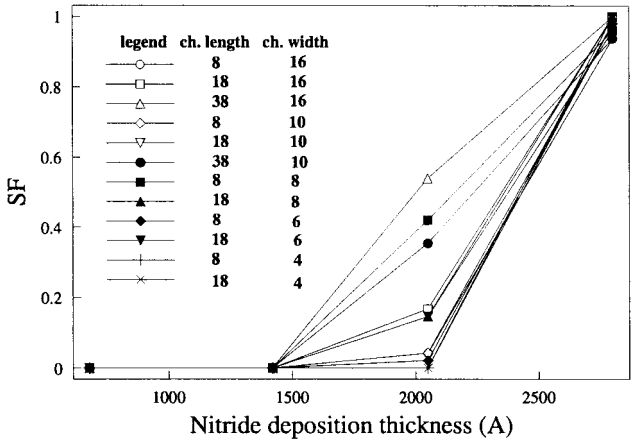

Fig. 7. SF as a function of deposition thickness of LPCVD silicon nitride for 12 Type-1 structures. Each cavity has eight etching channels. The channel height is 420 nm; their lengths are 8, 18, and 38 μm and the widths are 16, 10, 8, 6, and 4 μm.

C. Effects of Sealing Materials—Type-1 Structures

One major objective of this study is to identify the most efficient sealing material which requires the least amount of material deposition to achieve sealing. For each test structure, we evaluate the *SF* as a function of t_n and identify the $t_{n,\min}$ associated with each sealing material. Figs. 7, 8, and 9 show the history of the sealing process (*SF* versus the deposition thickness t_n) for 12 representative Type-1 structures using LPCVD silicon nitride, polysilicon, and PSG, respectively. Each test structure contains eight etch channels, each with a gap height of 420 nm (resultant from the sacrificial-layer etch). Etch channels in these structures have varying length (8, 18, and 38 μm) and width (16, 10, 8, 6, and 4 μm). In these three plots, SF data points at discrete deposition thickness are connected using straight lines. It should be noted that these lines are not valid data extrapolation (refer to Section V.B.). For sealing with LPCVD silicon nitride, experiments identify a lower-bound t_n value of 0.338 (or 1420 Å) below which no single structure is sealed (Fig. 7). For polysilicon deposition, the lower bound is 0.173 (726 Å) with the exception of two structures that exhibit SF values of larger than zero at this thickness (Fig. 8). Certain structures seal at a t_n of lower than 0.5; it is conjectured that the height of etch channels may have been changed. The lower bound t_n for PSG is 1.86 (Fig. 9). On the other hand, there is an upper bound $t_{n,\min}$ [0.67 for nitride (Fig. 7), 0.62 for polysilicon (Fig. 8), and 4.52 for PSG (Fig. 9)] above which *the test structure with the best sealing result (out of 12)* exhibits an SF greater than 0.95 (more than 95% sealed).

It is noted from Figs. 7, 8, and 9 that certain individual cavities achieve sealing when $t_n < t_{n,\min}$ even though the SF is below 1. In addition, at the final deposition thickness, there still remain unsealed cavities. These structures that demonstrate either advanced or delayed sealing are visually inspected under the optical microscope; no specific alteration or defects have been observed, nor does the occurrence of advanced or delayed sealing correspond to specific locations on a wafer.

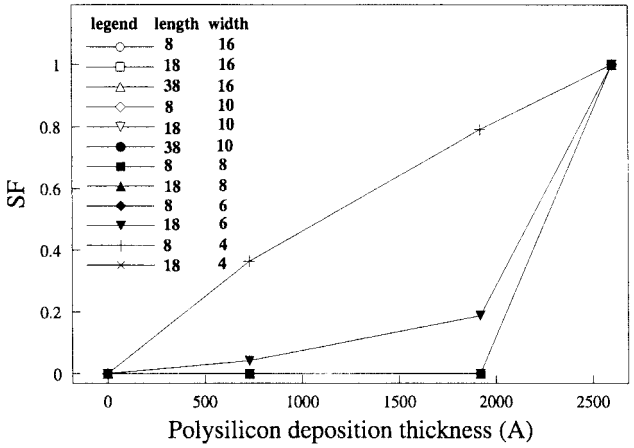

Fig. 8. SF as a function of deposition thickness of LPCVD polysilicon for 12 Type-1 structures. All cavities have eight etching channels. The channel height is 420 nm. The lengths are 8, 18, and 38 μm and the widths are 16, 10, 8, 6, and 4 μm.

Next, we cross-examine the sealing results of individual test structures by different materials. For a typical structure with eight etching channels, each 18 μm long and 4 μm wide, the comparison of sealing results by four CVD materials is shown in Fig. 10, which plots the *SF* with respect to T_n using data extracted from Figs. 7, 8, and 9. The value of $t_{n,\min}$ is 5.2 for PECVD nitride, 4.5 for LPCVD PSG, 0.67 for LPCVD nitride, and 0.62 for LPCVD polysilicon. Clearly, LPCVD polysilicon and silicon nitride are the most efficient sealing materials. PECVD material requires the largest deposition thickness to result in complete sealing. It could offer an advantage if low process temperature is desired (300 °C) to accommodate materials with low thermal stability.

D. Effects of Gap Heights—Type-1 Structures

In Section V-C, $T_{n,\min}$ data points have been obtained for a single etch-channel height. To investigate whether $t_{n,\min}$ remains unchanged at different etch-channel heights, we have performed sealing (with LPCVD silicon nitride) on four wafers

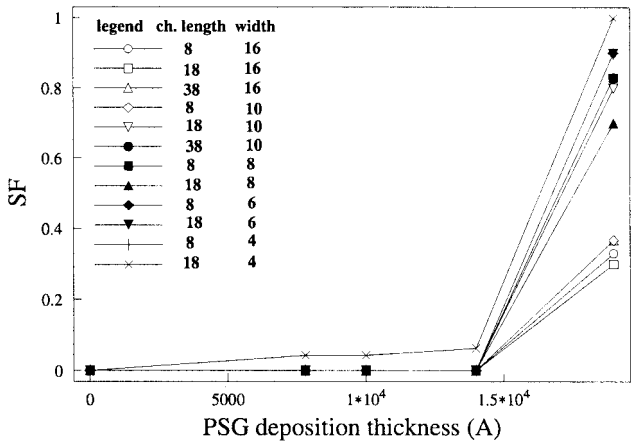

Fig. 9. SF as a function of deposition thickness of LPCVD PSG for 12 Type-1 structures. Each cavity has eight etch channels. The channel height is 420 nm. The lengths are 8, 18, and 38 μm and the widths are 16, 10, 8, 6, and 4 μm.

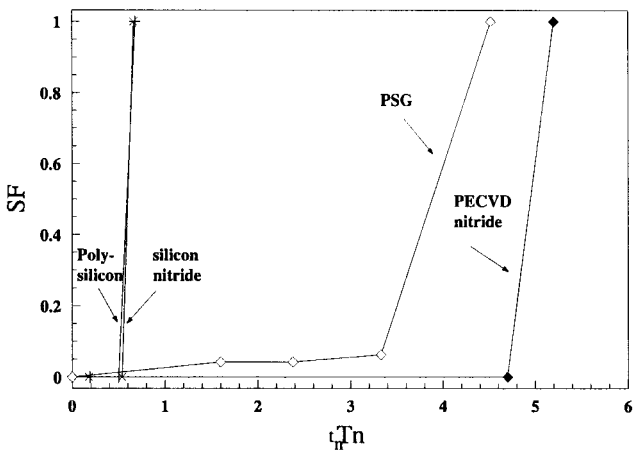

Fig. 10. SF versus t_n plots for different materials, including LPCVD nitride, LPCVD polysilicon, LPCVD PSG, and PECVD nitride. Structures under study are Type-1 with eight etching channels, each 18 μm long and 4 μm wide. Etching channel height is 420 nm. Clearly, $t_{n,\min}$ required for successful sealing depends on the sealing materials, 0.67 for LPCVD nitride, 0.62 for LPCVD polysilicon, 4.5 for LPCVD PSG, and 5.2 for PECVD nitride.

with various gap heights. Fig. 11 shows typical experimental results of $t_{n,\min}$ for a Type-1 structure with eight etch channels. The measured $t_{n,\min}$ values are 0.57 $\pm$ 0.08, 0.347 $\pm$ 0.03, 0.449 $\pm$ 0.04 and 0.44 $\pm$ 0.03 for the four gap heights of 420 nm, 520 nm, 743 nm, and 1.01 μm, respectively. Taking into account the above-mentioned data uncertainties, the results indicate that $t_{n,\min}$ is not sensitive to gap heights. (It is noteworthy that since the increment of deposition thickness is fixed, the relative error in $t_{n,\min}$ decreases with increasing gap heights.)

Effects due to gap heights are only calibrated with LPCVD nitride sealing. Attempts to conduct the same measurement procedure on other CVD materials were met with difficulties. In the case of LPCVD PSG and PECVD sealing, diaphragms may fracture when the deposited film (in compressive stress) is over 4 μm thick. This limits the achievable range of gap heights. When LPCVD polysilicon is used, the deposited film becomes opaque when the polysilicon thickness exceeds 300 nm, making it impossible to determine the sealing status through the established measurement procedure. In the future, scanning probe instruments with low loading force (<10 mg) can be used to examine the curvature of an optically opaque diaphragm and determine the sealing of underlying cavities.

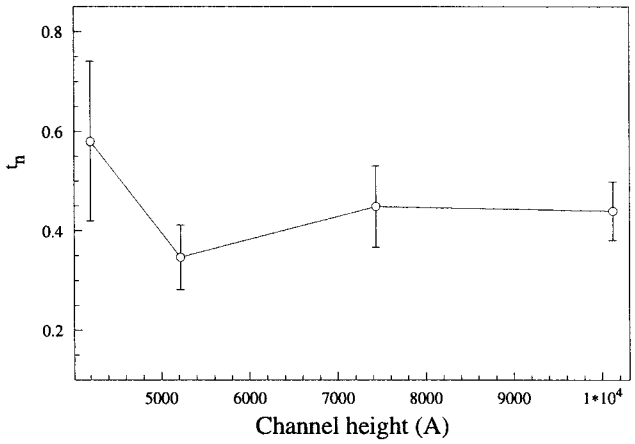

Fig. 11. Values of $t_{n,\min}$ at various channel heights (420 nm, 520 nm, 743 nm, and 1.01 μm) using LPCVD nitride sealing. The test structure is a Type-1 cavity with eight channels, each 18 μm long and 4 μm wide.

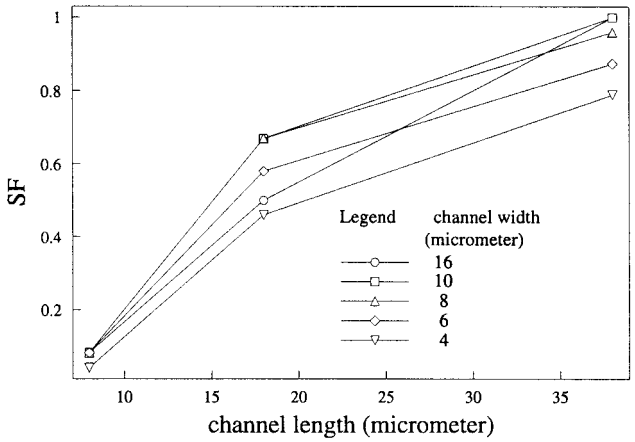

Fig. 12. SF as functions of channel lengths and widths for LPCVD silicon nitride sealing.

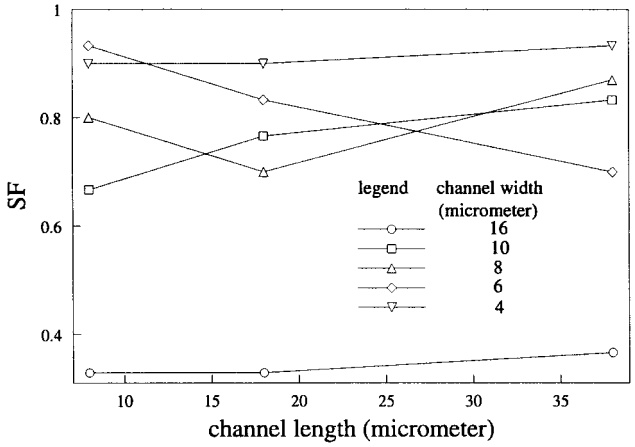

Fig. 13. SF as functions of channel lengths and widths for LPCVD PSG sealing.

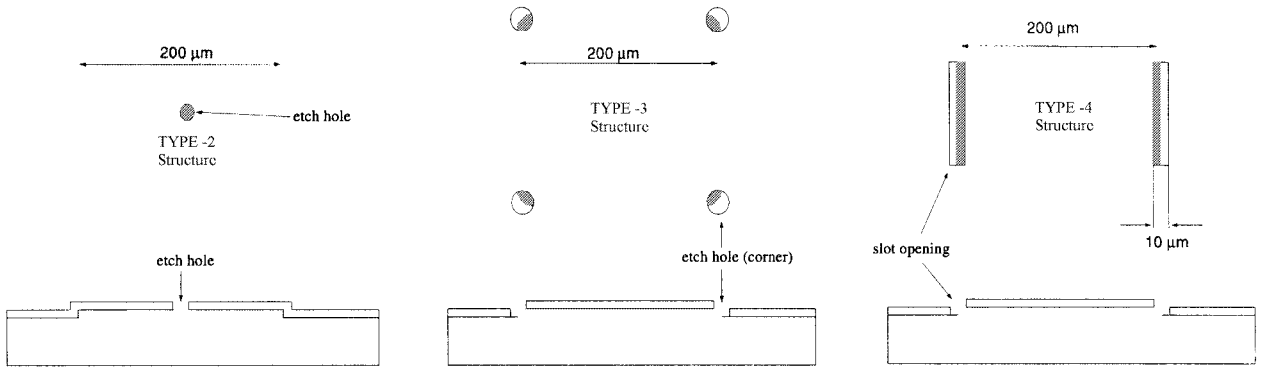

Fig. 14. Schematic diagrams of Types 2, 3, and 4 test structures.

E. Quantity and Dimensions of Etch Channels—Type-1 Structures

The dimensions (width and length) and quantity of etching channels affect the overall molecular transport and influence sealing results. To study the effects of cavity geometry, we cross-examine sealing results of a number of test structures at certain deposition thicknesses which lie between the lower bound (below which SF equals to 0) and the upper bound (above which SF equals 1) of deposition thickness for specific CVD materials.

The *number of etching channels* affects the speed of cavity undercut: a large quantity of etch-channels enhances chemical transport and shortens the time necessary to achieve complete cavity undercut. From the point of view of sacrificial-release process, it is therefore advantageous to have more etch channels. However, the number of etching channels can adversely affect the speed of cavity sealing. A cavity will not become sealed until *all* etch-channels develop hermetic sealing. Increased number of etch channels can therefore lower the probability of sealing a cavity.

Experimental data have confirmed the effects of etch-channel quantity. A limited set of results is presented here for a selected group of Type-1 cavities with fixed channel length and width of 8 and 4 μm, respectively. The number of etch channels on a cavity can be 8, 10, or 12. The distribution of etch channels is fixed in our designs. For cavities with 8 and 12 channels, the number of etch channels on each side is identical and the channels are distributed uniformly along the perimeter. For the ten-channel cavity, two opposing sides contain two channels while the remaining two sides have three channels. For sealing using LPCVD polysilicon, it has been discovered that SF increases with decreasing number of channels (12, 10, and 8). At t_n of 0.36, SF equals 0.08, 0.38, and 0.54 for cavities with 12, 10, and 8 channels. At t_n of 0.95, SF equals 0.63, 0.95, and 1 for cavities with 12, 10, and 8 channels.

We then investigate the effects on SF due to etch-channel length and width. The sealing results of 15 test structures at a particular deposition thickness of silicon nitride $(t_n = 0.49)$ are plotted in Fig. 12. These test structures can have three channel lengths (8, 18, and 38 μm) and five channel widths (4, 6, 8, 10, and 16 μm). It is concluded that SF improves with increasing etch-channel length and width, except for one disagreeing data point, contributed by a structure with channel length of 35 μm and width of 15 μm.

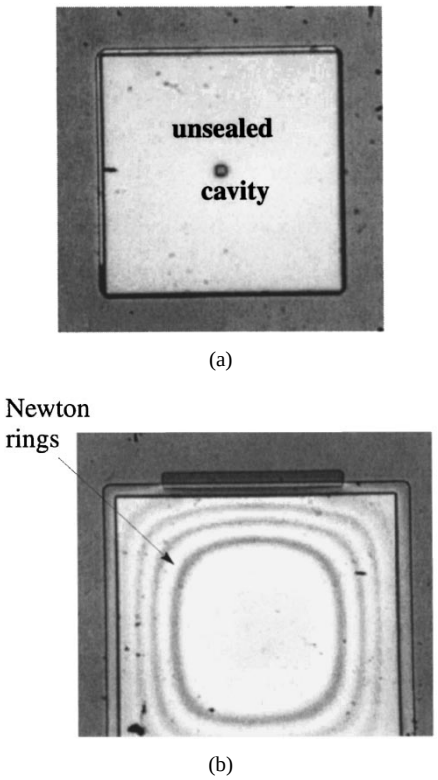

Fig. 15. SEM micrographs of (a) an unsealed Type-2 structure and (b) a sealed Type-4 structure.

For LPCVD PSG sealing of the same group of structures, results are plotted in Fig. 13 at a t_n of 4.5 (thickness being 1.4 μm). The sealing factor improves with decreasing channel width, whereas channel length seems to have little influence.

The overall trends of the geometric effects of sealing Type-1 structures are summarized in the following (for $t_n < t_{n,\min}$).

1) For silicon nitride sealing, the SF increases with increasing length and width of the etch channels.
2) For polysilicon sealing, the correlation between SF and etch-channels dimensions has not been conclusive.
3) For LPCVD PSG sealing, SF increases with decreasing width; SF does not change with length.

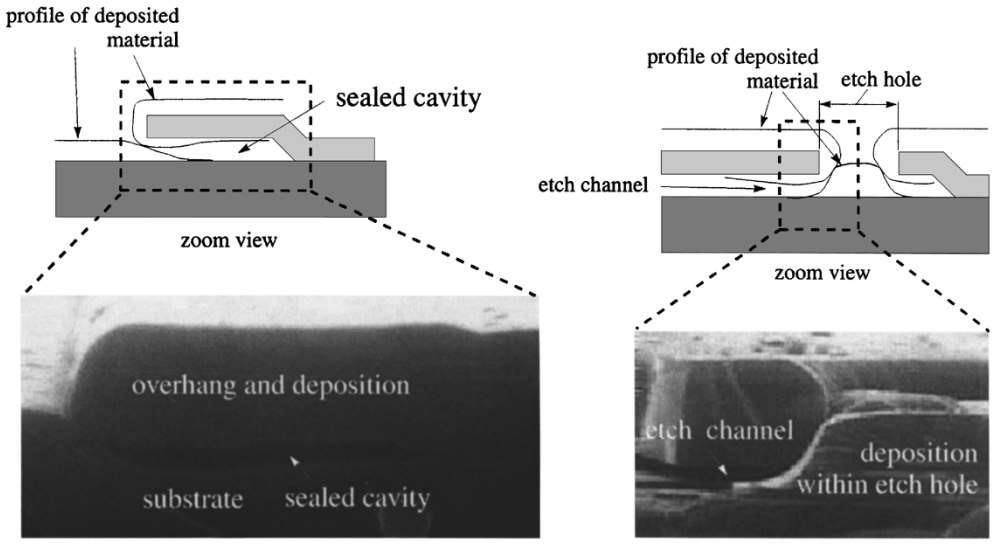

Fig. 16. SEM micrographs of the sealing profile after approximately 1.9 μm of PSG deposition. White lines indicate the contour of deposited PSG. (a) Side profile of deposition over an overhanging test structure; (b) profile of deposition near an etch hole of a Type-1 structure. The etch-channel height is 4200 Å.

TABLE II
GENERAL SEALING PERFORMANCE OF TYPE 2, 3, AND 4 STRUCTURES BY THE THREE LPCVD MATERIALS. HERE, *na* INDICATES THAT CONCLUSIVE EXPERIMENTAL RESULTS ARE NOT AVAILABLE. SEALING PERFORMANCE IS GOOD WHEN SF IS COMPARABLE WITH THAT OF TYPE-1 STRUCTURES; IT IS POOR WHEN SF IS SIGNIFICANTLY LESS THAN THAT OF TYPE-1 STRUCTURES. FOR TYPE-4 STRUCTURES, ONLY THOSE WITH ONE SIDE-OPENING SURVIVED THE ETCHING AND DRYING PROCESS

	TYPE 2	TYPE 3	TYPE 4
LPCVD nitride	poor	good	good
LPCVD polysilicon	poor	good	good
LPCVD PSG	na	good	na

F. Other Types of Test Structures

Test structures with other etch-channel configurations have also been explored. Schematic diagrams of structures of Types 2, 3, and 4 are shown in Fig. 14. Out of 126 test structures on each die, 36 are of Type 2. There are three Type-3 and 15 Type-4 devices. SEM micrographs of a Type-2 and a Type-4 structure are illustrated in Fig. 15.

Structures of Types 2, 3, and 4 do not contain extended etching channels but have etch holes that directly overlap with the cavity membrane. Compared with Type-1 structures, these structures can be more densely packed because etch channels and holes do not occupy extra chip area. However, it is likely that CVD deposition in the cavity interior will be more pronounced compared with that of Type-1 structures. *Type-2 and Type-3 structures* contain etching holes that are located in the center and corners of the cavity diaphragms, respectively. (Type-2 structures have been used by authors of [7].) We incorporate a variety of etch-hole sizes (2–16 μm) and quantities (1, 2, and 6) with the current design.

In Type-2 structures, etch holes are located on the cavity diaphragm, separated from the cavity bottom by the thermal oxide (1.3 μm thick) and the PSG layer. As expected, Type-2 structures are less efficient, requiring greater CVD thickness to seal because of the large gap height. The SF of Type-2 structures is significantly smaller (below 0.1) compared with that of Type-1 structures at respective deposition thickness for all three LPCVD sealing materials.

Type-3 structures can be efficiently sealed using all LPCVD sealing materials. Compared with Type-1 structures, these structures have identical gap heights and thus comparable sealing performance; *SF*'s for all Type-3 structures exceed 0.95 at t_n of 0.67 (for silicon nitride), 0.62 (for polysilicon), and 4.5 (for PSG).

Type-4 structures contain wide slot openings along the perimeter of a diaphragm. Although these structures have never been employed in the past, it is speculated that wide openings will enhance transport of reactant chemicals (or gas products) into and out of the cavity, therefore allowing for faster cavity etch. Designed slots are either 120 or 180 μm long, and are 10 μm in width. The number of openings on each cavity range can be one, two, or four.

On the other hand, the mechanical integrity of the diaphragms will likely be affected due to disturbance to the boundary-layer conditions. It has been observed that Type-4 structures with more than one slot opening suffer from yield loss that is attributed to stiction during the drying process. Fortunately, cavities with only one side opening have survived the sacrificial release and drying process. Under LPCVD silicon nitride and PSG depositions, the resultant SF for these Type-4 structures is comparable to that of Type-1 structures. As an example, for one cavity with one side opening 120 μm long (60% of the cavity side length), *SF* of greater than 0.95 has been achieved at deposition thickness that equals $t_{n,\min}$ determined using Type-1 structures.

For structures of Types 2, 3, and 4, fabrication yield is generally low except for cases noted above. In addition to stiction, some test structures may fracture during the cavity release process due to stress concentration created at etch holes. Table II summarizes sealing efficiency for Types 2, 3, and 4 structures that exhibit *high fabrication yield*.

G. Profile of Deposited Materials

Direct observation of the deposition profile has been achieved by performing SEM micrography on cleaved samples. Fig. 16(a) shows the profile of deposited PSG near an overhanging test structure, whereas part (b) represents PSG deposition profile near an etch hole. These micrographs confirm that for PSG sealing, deposition inside the cavity is minimal compared to the deposition on the front of the wafer; this observation agrees with the conclusion of Cheng *et al.* [20] that surface diffusion is not a strong factor in the LPCVD PSG step coverage.

V. Conclusion

The sealing of micromachined cavities using chemical vapor deposition methods has been systematically studied for the first time. We have fabricated test structures and studied their sealing behavior using specially designed experimental procedures. Statistical measurement of sealing probability for test structures provides sealing characteristics of test structures under various process and geometric parameters. Guidelines on optimizing design and processing parameters are derived.

Among all tested CVD materials, LPCVD nitride and polysilicon require the least normalized deposition thickness $(t_{n,\min})$ to seal Type-1 structures. The required normalized deposition thickness is 0.67 and 0.62 for LPCVD silicon nitride and polysilicon, respectively. With LPCVD silicon nitride, it has been observed that $t_{n,\min}$ is not strongly affected by the etch-channel gap heights. Data for other materials, including LPCVD polysilicon, PSG, and PECVD nitride, are not available. LPCVD PSG and PECVD nitride require higher $t_{n,\min}$ to seal. The normalized thickness is 4.5 and 5.2 for LPCVD PSG and PECVD nitride, respectively. Nonetheless, the PECVD material allows sealing at a low temperature and may offer some advantages for devices that cannot withstand high temperatures (e.g. above 600 °C).

It has been conjectured that a smaller number of etch channels increases the chance for a cavity to become sealed. Experiments have shown that for a typical cavity design, the sealing factor increases with decreasing number of etch channels associated with the cavity.

Geometries of etch channels affect the sealing performances of associated test structures. Within the current range of design, sealing results with respect to etch channel length and width have been discovered. In the case of LPCVD sealing, for example, *SF* increases with increasing etch-channel length and width at a given thickness of CVD material. When LPCVD PSG is the sealing material, the SF increases as the width of etch channels is reduced. The value of *SF* is not strongly influenced by the length of channels.

We have also studied three other types of test structures with unique etch-channel contours. The fabrication yield for many of these structures is low. Type 2 is inefficient and exhibits minimal probability of sealing under CVD depositions. Type-3 and selected Type-4 structures (those with high fabrication yields) are as efficient as Type-1 structures. These results suggest that straight channels are sufficient for producing effective sealing.

A more comprehensive study focusing on individual devices and a wider range of design parameters is warranted for future work. To study the profile of deposited materials, both inside and outside of the diaphragm, more rigorous experimental techniques [e.g., transmission electron microscopy and Rutherford backscattering (RBS)] are needed. This would allow the optimization of sealing process with respect to minimized internal deposition. Accurate computer simulation is critical as it may reduce the cost associated with experiments. The computer-aided simulation of the sealing process is not adequate for quantitative evaluation. Results from this investigation can help the development of accurate CAD tools.

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