

DC AND MILLIMETER-WAVE PERFORMANCE OF WATT-LEVEL BARRIER-INTRINSIC-N⁺ DIODE-GRID FREQUENCY MULTIPLIER FABRICATED ON III-V COMPOUND SEMICONDUCTORS

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ABSTRACT

This paper reports the fabrication and millimeter-wave performance of a new class of monolithic metal-semiconductor heterostructure devices, the Barrier-Intrinsic-N⁺ (BIN) diode-grid frequency multipliers, which are fabricated on III-V compound semiconductors. This work also involves the measurement of the DC and low frequency electrical properties of the BIN diode-grid frequency multiplier. In addition, a new analytical model which accurately describes the structure has been developed and is presented for the first time.

INTRODUCTION

Inexpensive watt-level CW solid-state sources are required for a variety of millimeter and submillimeter wave applications. Available solid-state oscillators, such as GaAs Gunn diodes and IMPATTs, are currently limited to frequencies up to about 75 GHz and 150 GHz, respectively. Much higher frequencies can be obtained by generating harmonics of the fundamental frequency from solid-state oscillators operating at a lower frequency. To overcome the power limitations of a single-diode multiplier, we have developed the design of a diode grid for frequency multiplication [1]. In this approach, a grid is monolithically integrated with thousands of diodes thereby resulting in potentially low-cost fabrication and small-size realization. The power is distributed among many diodes making possible watt-level output power. The feasibility of this approach has been demonstrated by a Schottky diode-grid frequency doubler with watt-level output power at 66 GHz [2].

THE BIN DIODE-GRID FREQUENCY MULTIPLIER

Device Concept

The Barrier-Intrinsic-N⁺ (BIN) diode incorporates a thin (1000 Å) undoped semiconductor layer (I) on a heavily doped layer (N⁺) serving as a back contact. On top of the undoped layer there is an ultrathin (≥ 100 Å) electron-blocking barrier layer (B) in contact with a metal top layer. This blocking layer can be formed by an insulator, a semiconductor with a very wide band gap, or a Mott barrier. The device can be switched rapidly

between two capacitance states which correspond to accumulation of electrons at the barrier and depletion of the intrinsic layer, respectively, by the applied bias. This results in a highly nonlinear capacitance-voltage characteristic that is needed for efficient harmonic generation. Due to the blocking barrier of the BIN structure, two diodes can be operated back-to-back generating a sharp symmetric spike in the capacitance-voltage curve, which eliminates even harmonics and thus favors tripling operation. The height and width of this capacitance-voltage curve can, in principle, be adjusted by doping control alone. This arrangement needs no external ohmic contact resulting in a highly efficient frequency tripler.

In summary, the advantages of the BIN diode over the Schottky diode are seen in (1) the stronger nonlinearity of the C-V curve, which generates harmonics more efficiently (especially the third harmonic without using an idler) and (2) the ability to reach a high capacitance state before forward conduction sets in, making possible the capacitive tripler.

Previously, we have proven the feasibility of near-millimeter wave operation with a SiO₂/Si BIN diode used in a waveguide/whisker contact configuration as a frequency doubler [3]. This diode (Fig. 1) had a transit time of 1 ps and an intrinsic cut-off frequency of 320 GHz. A maximum efficiency of 15% was experimentally obtained at 95 GHz which is in good agreement with the theoretical predictions [4,5].

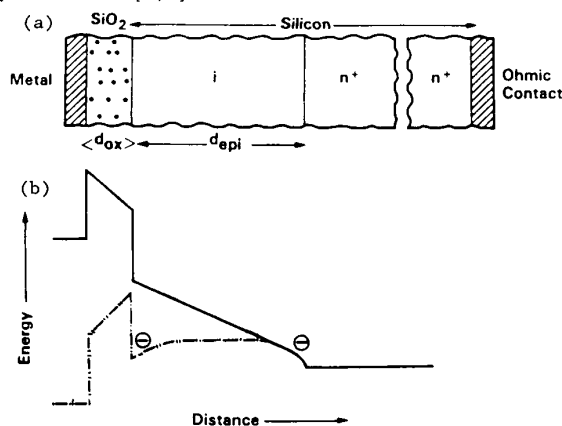


Fig. 1 (a) Structure of the SiO₂/Si Barrier-Intrinsic-N⁺ diode, (b) Conduction band profile of the silicon BIN diode.

Recently, a novel concept which allows the construction of a GaAs BIN diode entirely by selective doping during MBE growth (Fig.2) has been proposed [6]. A Mott-barrier is formed by a thin (300 Å) intrinsic layer sandwiched between the top metal contact and a charge sheet created by selective doping. GaAs is superior to Si due to the higher mobility and maximum velocity which will reduce the transit time to about 0.3 ps and render the negligible parasitic resistance of the back contact. An intrinsic cut-off frequency of 960 GHz was achieved. A tripling efficiency of 35% at an output frequency of 99 GHz is therefore predicted. Figure 3 shows the capacitance-voltage and conductance-voltage characteristics of an experimental device.

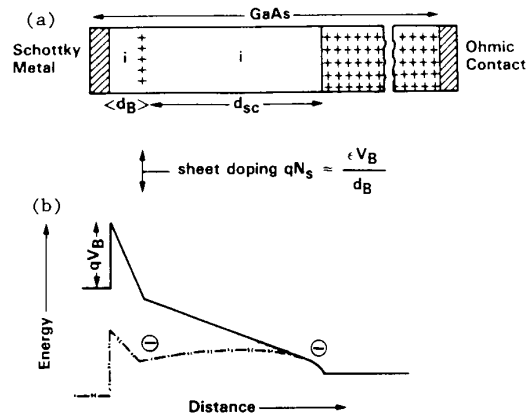


Fig. 2 (a) Structure of the Mott Barrier-Intrinsic- N^+ diode, (b) Conduction band profile of the GaAs BIN diode.

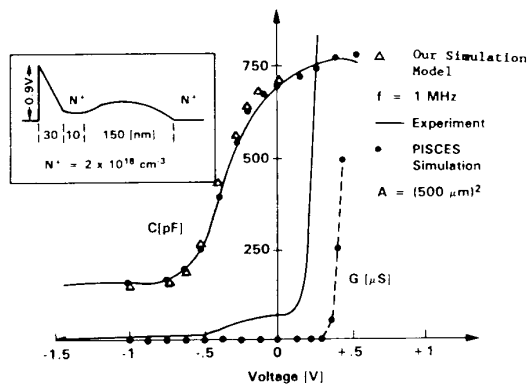


Fig. 3 Capacitance vs. voltage curve from our simulation model shows good agreement with the experimental measurement for the GaAs BIN diode.

Device Modelling

A new numerical technique to solve the Poisson equation in multilayer semiconductor devices having a stepwise doping profile has also been developed. The model allows for detailed simulation of the device and provides crucial physical insight into the key performance parameters in a variety of formats that numerical device-analysis programs,

although powerful in their own right, are unable to provide. The Poisson equation is solved by a set of coupled analytical expressions which accurately describe each region of the GaAs BIN diode. Band and carrier continuity between layers is included and properly accounted for. The final expressions derived are transcendental and require carefully structured algorithms to avoid inaccurate and unrealistic convergent difficulties. The capacitance-voltage curve obtained from our numerical modelling is in excellent agreement with a PISCES-II simulation and the experimental measurement of the GaAs BIN diode (Fig. 3). In addition, this model does not require large computer memory arrays.

Device Fabrication

A novel grid structure has recently been designed for the BIN diode tripler array as shown in Fig. 4. The metal grid consists of a columnar mesh of aluminum strips with Schottky electrodes on each end. The small dimensions of the Schottky electrode area minimizes the zero-voltage capacitance and series resistance to increase the cut-off frequency of the diode. The two neighboring Schottky electrodes are designed to provide the back-to-back configuration for the GaAs BIN diodes. Proton bombardment is used on the region surrounding the active device area to convert it to semi-insulating GaAs. A 7 μm thick of photoresist layer is required to protect the active diode area from the implantation, with an oxygen plasma employed to remove the thick photoresist. The symmetric capacitance-voltage and conductance-voltage curves from two back-to-back connected GaAs BIN diodes illustrated in Fig. 5 demonstrate the concept of the back-to-back operation.

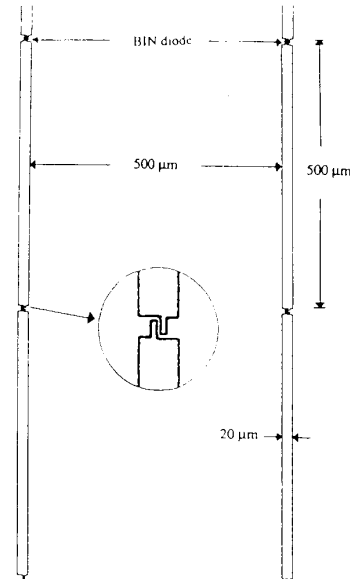


Fig. 4 Schematic of the BIN diode grid as a tripler array.

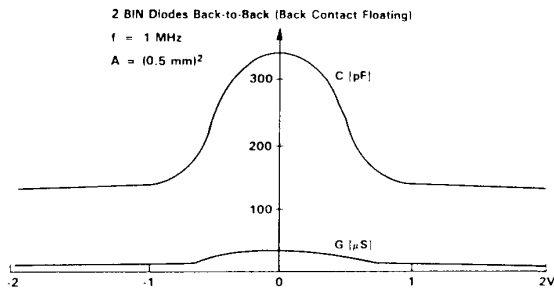


Fig. 5 Symmetric capacitance-voltage characteristic from the experimental measurement of two back-to-back connected GaAs BIN diodes.

Device Performance

Figure 6 shows the theoretical diode multiplication efficiency. The quasi-optical tripler configuration we have developed (see Fig. 7) has been tested and verified using a previously fabricated monolithic Schottky diode array. An unoptimized output power of 0.5 W was achieved at 99 GHz for the diode grid with a low cut-off frequency (≈ 115 GHz, $f_o/f_c \approx 0.29$), in excellent agreement with the theoretical predictions [4,5]. From the large-signal multiplier analysis study [7] using the measured capacitance-voltage data of Fig. 5, a maximum tripling efficiency of 24% at an output frequency of 99 GHz is achieved for the GaAs BIN array which has recently been fabricated. This can be clearly seen from the results in Fig. 8. It should be recalled that, due to the symmetric capacitance-voltage characteristic of two back-to-back connected GaAs BIN diodes, even harmonic currents cancel, therefore even harmonic idler circuits are unnecessary. This can also be shown from the large signal analysis results in Fig. 9, which shows that the efficiency is insensitive to second harmonic impedance.

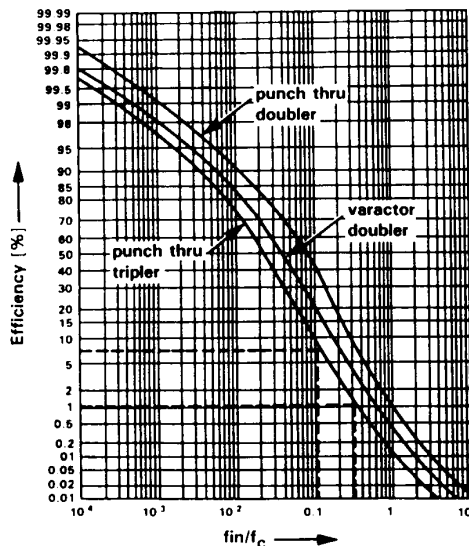


Fig. 6 Theoretical predictions of the doubler and tripler efficiencies of the punch through diode and the doubler efficiency of the varactor diode.

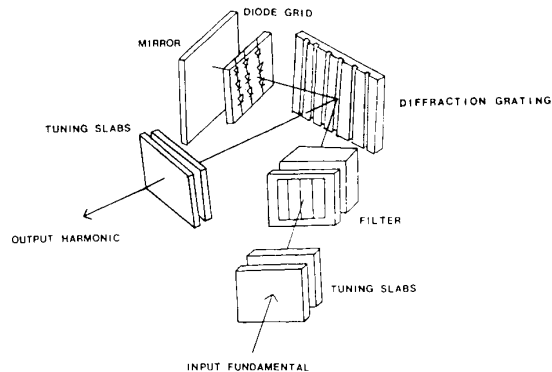


Fig. 7 Configuration of the quasi-optical BIN diode-grid tripler circuit with a diffraction grating plate as the high-pass transmission filter.

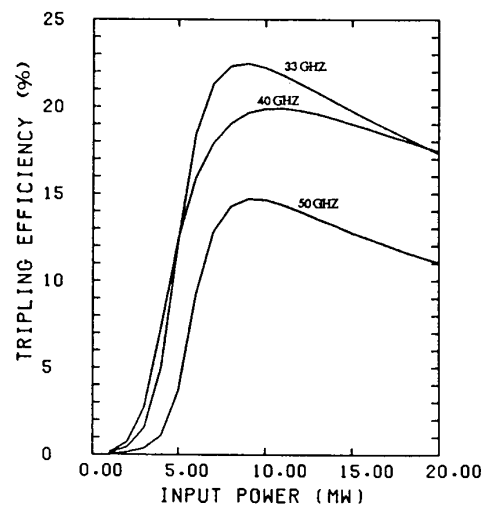


Fig. 8 Tripling efficiency of the GaAs BIN diode tripler versus input power.

SUMMARY

Based on the theoretical and experimental studies presented in this paper, we are confident in predictions of watt-level CW output power at 90 - 180 GHz from a monolithic diode-grid multiplier design employing the GaAs BIN concept.

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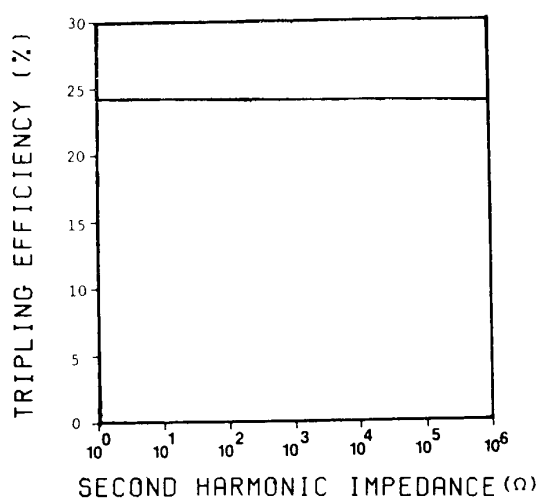


Fig. 9 Tripling efficiency of the GaAs BIN diode tripler versus second harmonic impedance.