An Optimized Design of Distributed Active Transformer

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***Abstract*—A novel structure distributed active transformer (DAT), which significantly reduces the coupling from the DAT to the feed line is demonstrated. A grounded guard line is implemented to isolate the feed line from the magnetic field of the DAT. The measured result of the DAT on a GaAs substrate shows a 10.5-dB reduction in the coupling. To reduce DAT loss, an air-bridge connected double primary DAT structure is implemented. The DAT at 2 GHz shows a 0.7-dB loss reduction in comparison to the conventional DAT. The improved DAT performance is related to the reduced metal resistance and closer coupling between the primary and secondary loops without any increase in the DAT area.**

***Index Terms*—Circular geometry, distributed active transformer (DAT), magnetic coupling reduction, passive loss reduction, power amplifier, power combining.**

I. Introduction

THE increasing demand for mobile communications requires a highly integrated, low-cost, and highly efficient RF power amplifiers. A silicon technology is a promising choice for high-volume production, and numerous monolithic integrated silicon RF power amplifiers have been reported. However, several attempts have demonstrated that the performances of a fully integrated power amplifiers using conventional design topologies do not meet the efficiency and power level required by many applications, such as cellular phones, indicating that an integrated power amplifiers with high output power and high power-added efficiency (PAE) at a low supply voltage is a real challenge. Therefore, a fully integrated power amplifier in silicon with good output power, efficiency, and linearity has been one of the major obstacles in today's pursuit of a single-chip radio with an integrated power amplifier and transceiver. The first successful demonstration of a watt-level gigahertz-range power amplifier in silicon integrated circuits (ICs) has been reported recently by Aoki *et al.* at the California Institute of Technology (Caltech), Pasadena. In the circuit technique, a circular-geometry distributed active transformer (DAT) [1], [2] elegantly combines power serially, boosting up the impedance level and reducing circuit loss on the conductive Si substrate in a fully integrated topology. Also, the low breakdown voltage of the short-channel MOS transistor and thermal dissipation problem have been solved by the structure. Despite these advantages, the DAT still has some drawbacks, which are unavoidable structural characteristics. The DAT, shown in Fig. 1, consists of four parts, which are: 1) feed lines to drive the signal to the base or gate of each power transistors; 2) the transistors to generate ac current on the primary loop; 3) a distributed primary loop to collect the ac current from the devices and to generate magnetic fields; and 4) a single-turn secondary loop to couple the magnetic field and deliver it to the load. There are two problems with this circuit topology. The first problem is the DAT to feed-line coupling. The input feed lines of this amplifier pass through the inside of the DAT where a strong magnetic field is created. The consequential magnetic coupling generates positive feedback, which might be fatal to amplifier stability, and asymmetry in the push/pull input if not suppressed properly. The asymmetry might be further enhanced by process-related asymmetries, and the performance can be degraded significantly. We can see the oscillation tendency of the magnetic coupling between the DAT and feed line from the gain curve of measured results in [1]. The second problem is the passive circuit loss of the DAT mostly caused by metal resistance and substrate conductance, which is a decisive factor in the power-amplifier efficiency. In this study, the feed-line isolation from the magnetic coupling and the DAT loss are greatly improved using the novel structure DAT. Although we have analyzed DAT performances and demonstrated them by a DAT on the GaAs substrate, the results can be applied to the DAT on the Si substrate without loss of generality.

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II. Feed-Line Isolation From the Magnetic Field

Here, the principle for the feed-line isolation from the magnetic field is explained. Two types of prototypes are also designed and fabricated to confirm the principle.

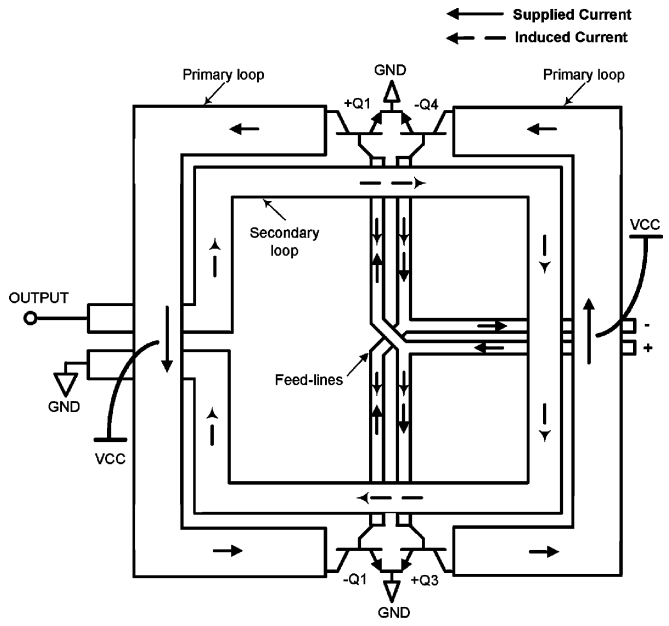
A. Principle of Feed-Line Isolation

Fig. 2(a) shows the magnetic coupling from the slabs to feed line known as Faraday's law of electromagnetic induction [3]

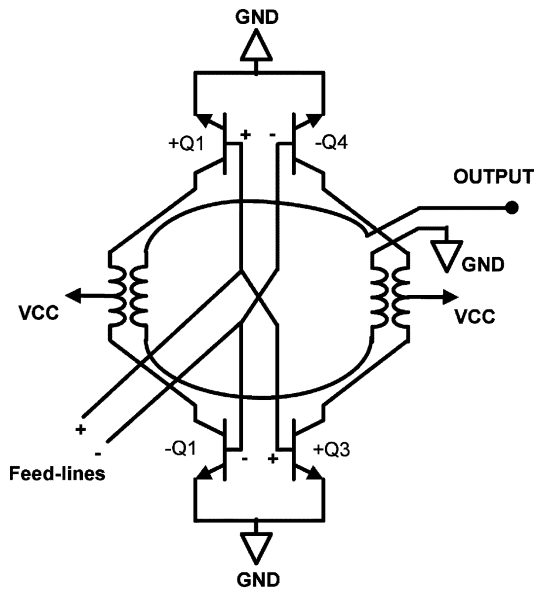
$$V = -\frac{d\Phi}{dt}\,(V) \tag{1}$$

where

$$V = \oint_C E \cdot d\ell = \text{EMF induced in circuit by contour } C\,(V) \tag{2}$$



(a)

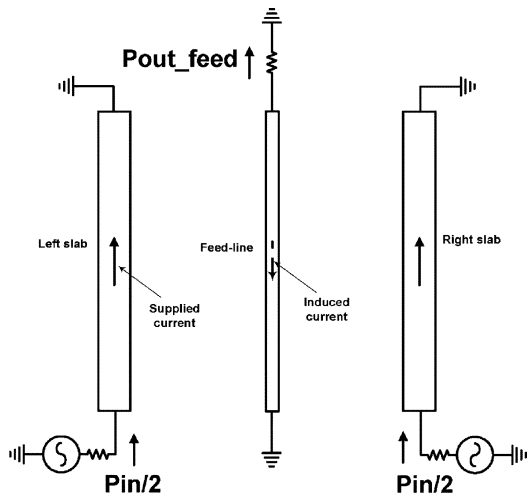


(b)

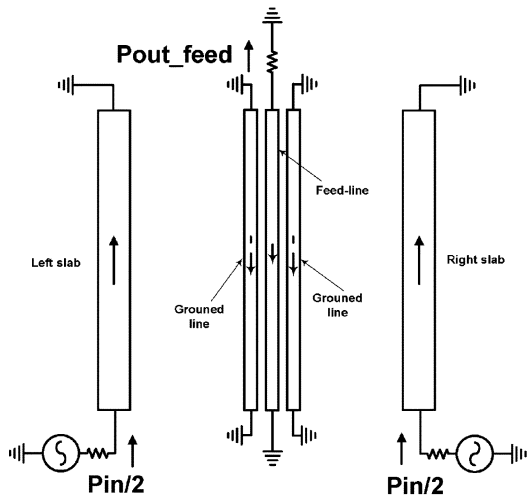
Fig. 1. (a) Illustration of distributed active-transformer. (b) Its corresponding electrical diagram.

$$\Phi = \int_S B \cdot d\mathbf{s} = \text{magnetic flux crossing surface } S\ (Wb). \tag{3}$$

In Fig. 2, the length of slabs and feed line are 1.5 mm. Two slabs are separated by 1 mm. The widths of the slabs and feed line are 120 and 10 μm, respectively. The feed line is placed at the middle of the two slabs. The induced electromotive force (EMF) generates a current in the feed line. Fig. 2(b) is similar to Fig. 2(a), but the grounded lines are included. The induced EMF by the two slabs generates currents in the feed line and two grounded lines. This situation can be regarded as two shunt resistors connected to a voltage source. In this case, most of the current flows through the lower resistor. By this principle,



(a)



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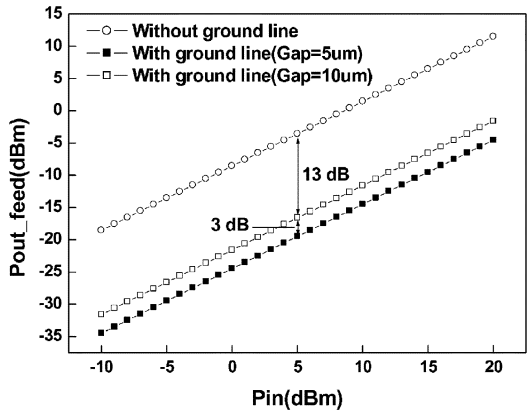
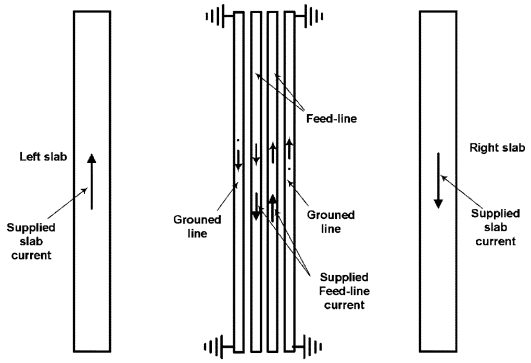


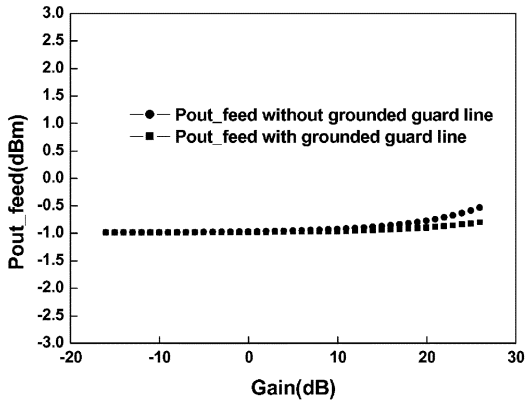
(c)

Fig. 2. Two different feed-line configurations and their simulated results. (a) Normal feed line. (b) Feed line with grounded guard lines. (c) Simulated feed-line output powers from feed line versus input power to slabs.

most of the induced current flows through the grounded lines. Therefore, these grounded guard lines can be regarded as a magnetic-field shielding block. The induced currents of the structures are simulated using the SONNET electromagnetic simulator [4] and the results are depicted in Fig. 2(c). The magnetic



(a)



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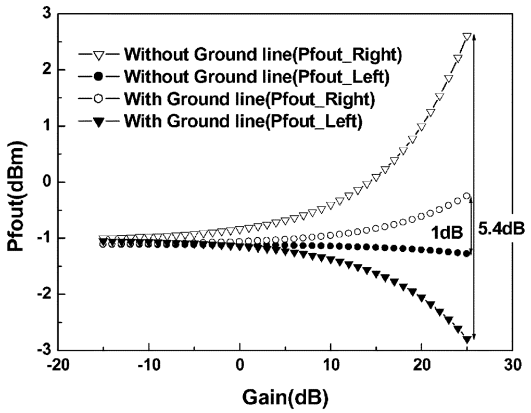

(c)

Fig. 3. Guarded feed-line structure and the simulated results for coupling to feed lines (a) The structure composed of two slabs, two feed lines, and two grounded guard lines. (b) Simulated results of center-positioned feed-line case. (c) Simulated results of 40-μm right-shifted feed-lines case.

coupling could be reduced over 13 dB, depending on the structure arrangement.

B. Feed-Line Isolation From the Magnetic Field Created by the Slabs

The shielding technique is applied to our feeding line, as shown in Fig. 3(a). It consists of two wide slabs, two narrow feed-lines, and two grounded guard lines. Quasi-three-dimensional (3-D) simulation using SONNET and circuit simulation using ADS [5] have been performed on the complete structure as a part of the design cycle to verify the performance of the structures at 2 GHz. The process parameters used in the simulation are summarized in Table I.

TABLE I
PROCESS PARAMETERS ON A TYPICAL GaAs SUBSTRATE

Description	Value
Metal thickness	4 um
Metal resistivity	6.1 mΩ/sq
Metal type	Gold
Substrate thickness	200 um
Substrate ε_r	13

The sizes of the slabs and lines in Fig. 3 are identical to the section A case. The supplied currents flow upward in the left-hand-side slab and the right-hand-side feed line, and flow downward in the right-hand-side slab and left-hand-side feed line. The current amplitudes and directions are represented by the arrow-headed solid lines and the induced currents on the feed lines are represented by the arrow-headed dashed lines, as shown in Fig. 3(a). As the power in the slab increases, the induced current also increases. The induced current flows in the oppose direction to the change in the linking magnetic field, which is known as Lenz's law. The left-hand-side feed line is closer to the left-hand-side slab than the right-hand-side slab and the resultant induced current flows downward after cancellation of the two induced currents. The resultant induced current in the right-hand-side feed-line will flow upward in a similar manner. As can be seen in Fig. 3(b), the induced output power in the line, without grounded guard lines, increased approximately 0.5 dB when the power-level difference between the slabs and feed lines increases to 25 dB. In the real power-amplifier operation, this power-level difference is identical to the gain of the power amplifier, and the horizontal axis is placed as gain. With the guard lines, the feed-line output power level is increased by 0.2 dB, which is lower by 0.3 dB. To test the applicability of the guard lines for the process variation, the feed lines are shifted 40 μm to the right-hand-side direction from the center position, making both the feed lines closer to the right-hand-side slab than the left-hand-side slab and perform the same test. In this case, the induced currents in both feed lines flow upward, the opposite direction to the current in the right-hand-side slab. Since the applied current direction on the right-hand-side feed line is the same as the induced current, but the current on the left-hand-side feed line is opposite to the induced current, the total current in the right-hand-side feed line is increased and that of left-hand-side feed line is decreased, as shown in Fig. 3(c). Using the guard lines suppress the feed-line output power deviation 1 dB, a 4.4-dB improvement compared to the no-guard line case of 5.4 dB. To confirm the simulation results, 40-μm shifted lines are fabricated on a GaAs substrate, as shown in Fig. 4. In addition to the above design, one other design with long air-bridge connected grounded guard lines is also fabricated, as shown in Fig. 4(c). Fig. 4(d) shows the measured data. Due to the guard line, the feed-line output power deviations is reduced to 0.9 dB from 5.2 dB of the nongrounded guard line case at a power level difference of 25 dB. The deviation becomes further reduced to 0.1 dB when the guard lines are connected to each other by the air bridge. These results clearly indicate that

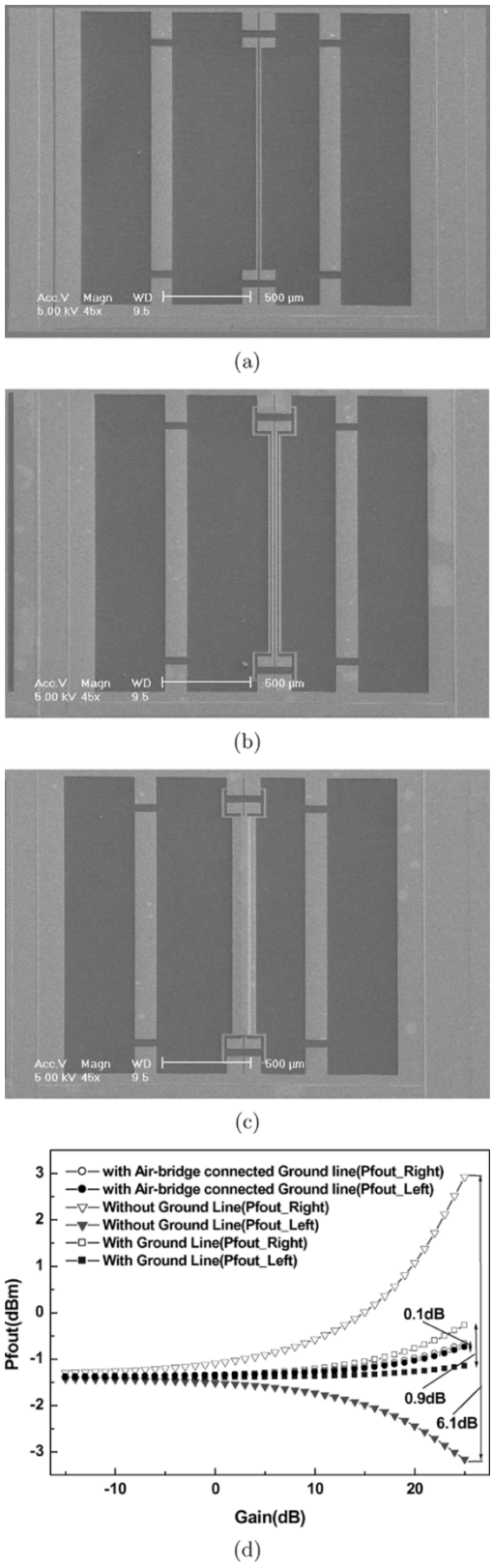

Fig. 4. Micrographs of the feed lines and measured results. (a) Feed lines without grounded guard lines. (b) Feed lines with grounded guard lines. (c) Feed lines with air-bridge-connected grounded guard lines. (d) Measured results of the three cases.

the shield effect of the grounded guard line is excellent, regardless of structure asymmetry.

C. Feed-Line Isolation From the Magnetic Field of the DAT

The DAT circuit consists of two parts, i.e., a primary loop for driving ac current around the structure generating magnetic fields, and a secondary loop for coupling the magnetic field to deliver the power to the load. The typical structure and current flows are depicted in Fig. 1. $Q1 \sim Q4$ represent transistors. The collectors or drains of the transistors are connected to the primary loop and the four terminals of the feed lines are connected to the bases or gates of the transistors to supply input power. The current in the primary loop is driven by two push/pull transistor pairs, i.e., transistor Q1-Q4 and Q2-Q3. The magnetic field generated by the primary loop current creates the induced current on the secondary loop. When a clockwise current flows in the primary loop, the induced current in the secondary loop flows in a counterclockwise direction. In the DAT, the feed lines are placed inside the primary loop, and due to the magnetic coupling from the primary loop, the power levels of the feed lines are deviated from the balance input. We can classify the feed lines into two groups according to their direction—called horizontal feed lines—placed from the right- to left-hand sides, and vertical feed lines placed from top to bottom. The vertical feed lines are twice as long as the horizontal feed lines. Hence, the dominant magnetic coupling arises between the primary loop and vertical feed lines. The only vertical slabs, placed from top to bottom, participate in the magnetic coupling with vertical feed lines because the horizontal slabs cross the vertical feed lines at right angles. Therefore, most of the feed-line coupling problem is the magnetic coupling between the vertical slabs and vertical feed lines, which is identical to the magnetic coupling between vertical slabs and vertical feed lines depicted in Fig. 3. Hence, using the grounded guard line, the magnetic coupling can be reduced drastically. We have built two DATs with and without guard lines and the microphotographs are shown in Fig. 5(a) and (b), respectively. The process parameters are the same as Table I, except for the thicker substrate with 470 μm. For a clear distinction between the two cases, the vertical feed lines are shifted 40 μm from the center to the right-hand side. The measured results of the DATs for power level difference of 25 dB are shown in Fig. 5(c). These results suggest that the effect of the grounded guard line is consistent. For the reduction of the horizontal magnetic coupling, a horizontally placed grounded line can additionally be inserted in the DAT.

III. DAT Loss Reduction

A. Design and Fabrication of Novel DAT Structure

The DAT is a rather large-size component and a compact DAT with a low loss is a primary design factor for power amplifiers. In this study, we have a fixed DAT area as 1.2×1.2 mm^2 and the process parameters in Table I, except for a substrate thickness of 470 μm and metal resistivity of 10 mΩ/sq, and optimized the structure for a low loss. The important design parameters are a low metallic loss and tight magnetic coupling by a large mutual inductance. If two neighboring closed loops (C_1 and C_2) with currents of I_1 and I_2 form surfaces S_1 and S_2 with magnetic

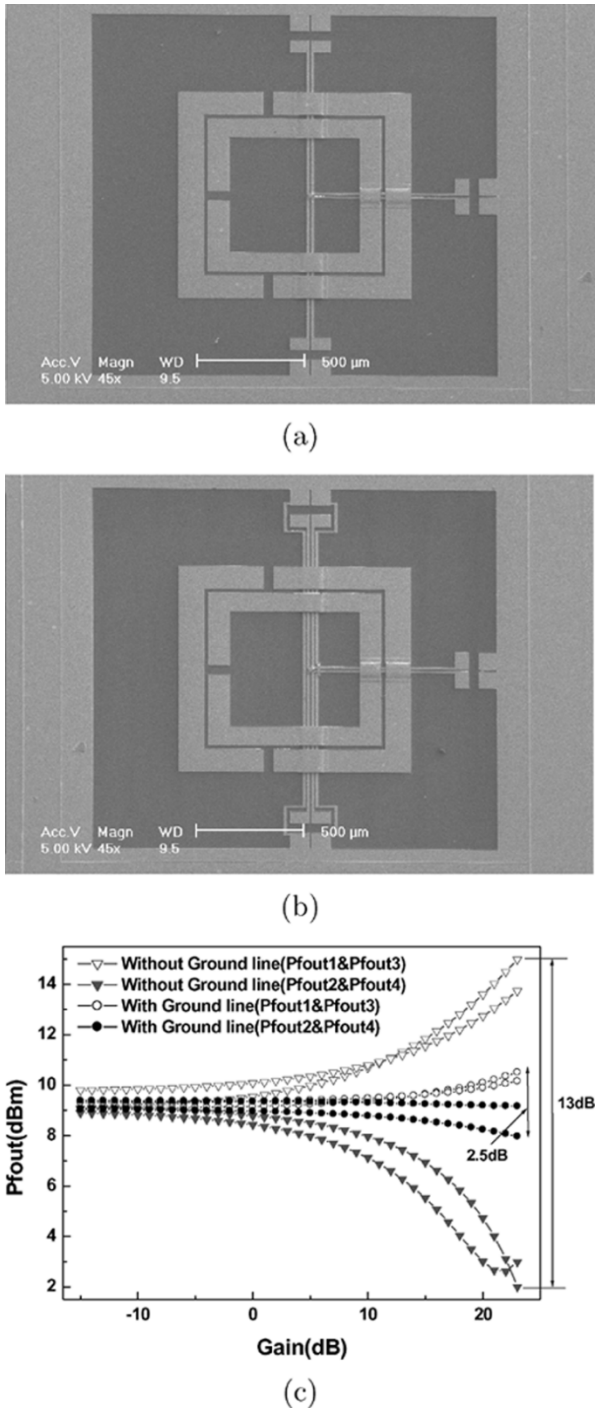

Fig. 5. Micrographs of two DATs and measured results. (a) Micrograph of the DAT without grounded guard lines. (b) Micrograph of the DAT with grounded guard lines. (c) Measured results for two DATs.

fields of B_1 and B_2, respectively, the mutual inductance of the structure can be represented as follows [3]:

$$M = \frac{\Phi_{12}}{I_1} \ (H) \tag{4}$$

where Φ_{12} is called the mutual flux, which is represented by

$$\Phi_{12} = \int_{S_2} B_1 \cdot dS_2 \ (Wb). \tag{5}$$

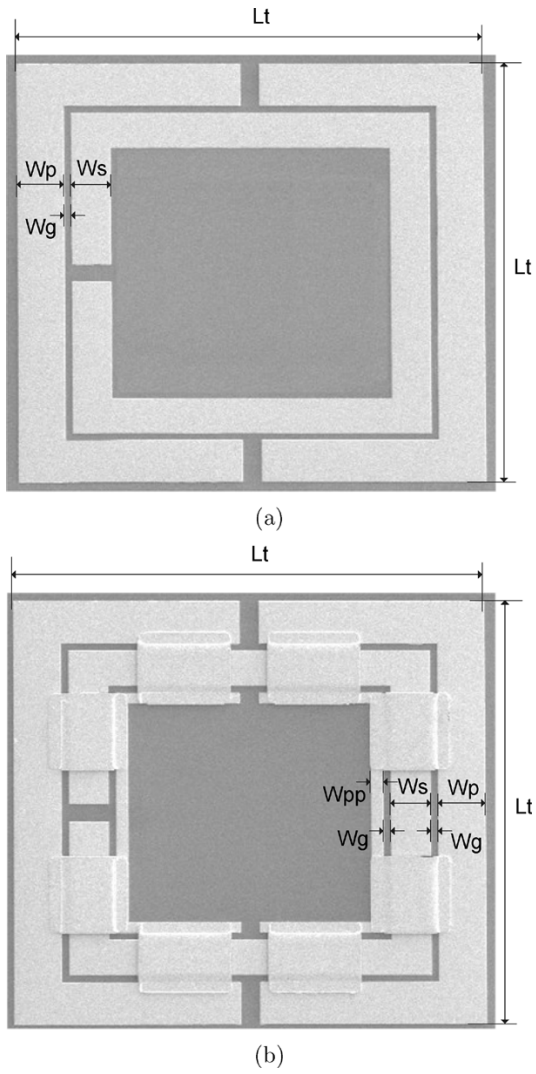

Fig. 6. Micrographs of the fabricated DATs. (a) Micrograph of a conventional DAT structure. (b) Micrograph of a novel DAT structure.

To maximize the magnetic coupling under a constant primary current, the distance between the primary loop and center of the secondary loop must be as small as possible and the area of the secondary loop must be as large as possible. The widths of the primary and secondary loops should be wide to reduce metallic loss, resulting in a large-size DAT. Therefore, the widths of each loop should be optimized for a given size constraint. Using SONNET for the structure in Fig. 6(a), the upper group of lines in Fig. 7(a) represents the simulation result. The optimum primary- and secondary-loop widths are 120 and 100 μm, respectively, under the fixed DAT area of 1.2×1.2 mm^2 with a minimum loss of 1.54 dB. To reduce the DAT loss further, we have enlarged the width of the primary loop through the upper space of the secondary loop. To realize it, we insert a sub-primary loop inside the secondary loop and connect it with the primary loop using wide air bridges, covering half of the girth as shown in Fig. 6(b). The width of the sub-primary loop is restricted to as narrow as possible for maintaining the effective secondary loop area. The new DAT delivers a far better performance because

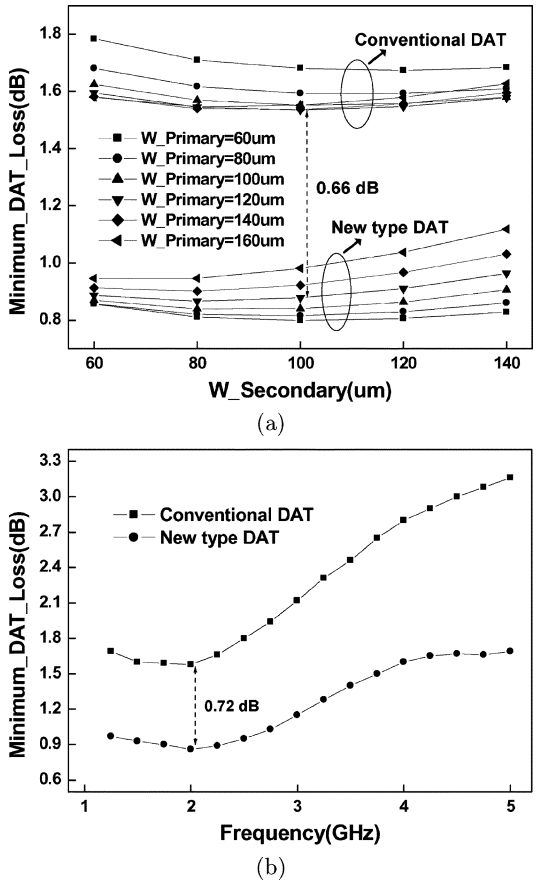

Fig. 7. Simulated and measured results of two DATs. (a) Simulated result with DAT loop width variation. (b) Measured results of DAT loss with frequency variation.

the effective metal loss and the distance from the primary- to secondary-loop center are reduced without sacrifice of the secondary-loop size. The lower group of Fig. 7(a) represents SONNET simulation result of the structure. The minimum loss is determined as approximately 0.88 dB when the widths of the primary and secondary loops are both 60 μm. To verify these results, two DATs are fabricated on a GaAs substrate. They have the same primary and secondary widths of 120 and 100 μm, respectively, but different structures, one as shown in Fig. 6(a) and the other as shown in Fig. 6(b). The process parameters are the same as Table I, except a substrate thickness of 470 μm and a metal resistivity of 10 mΩ/sq. The measured results of the fabricated DATs are shown in the Fig. 7(b). The minimum loss of the conventional DAT is 1.58 dB, and that of the new DAT is 0.86 dB, a 0.72-dB improvement. The improvement of the loss is similar to the simulated result of 0.66 dB. The results cannot be the same because the substrate thickness, metal resistivity, and roughness are slightly different from each other. We can still see a big improvement in DAT losses. These loss reduction methods can be extended to the other applications such as transformers, baluns, and inductors, which need a low loss.

B. Theoretical Analysis of the DAT

The DAT is identical to a single-turn coupled-inductor transformer. Hence, analyzing the standard transformer model, we can obtain the basic parameters for the DAT such as input

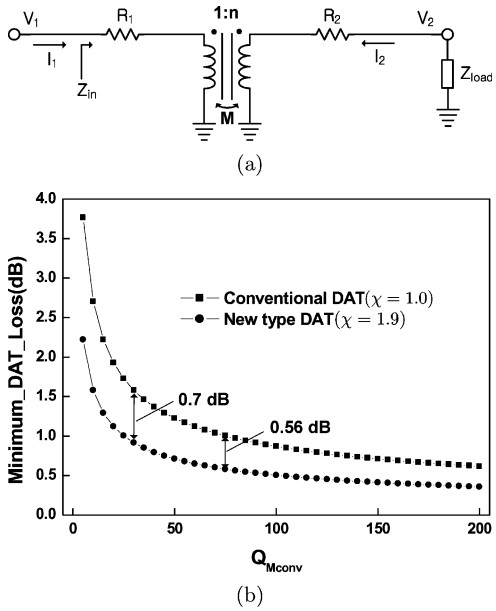

Fig. 8. (a) Model for the transformer with two single-turn loops. (b) Calculated results for DAT loss versus $Q_{M\mathrm{conv}}$.

impedance, circuit loss, optimal output impedance for minimizing the DAT loss, etc. Fig. 8(a) shows the equivalent model of transformer, where the lossy inductors of the transformer are modeled by the equivalent series resistors R_1 and R_2 and net inductances L_1 and L_2 [6]. The magnetic field created by the port-1 current I_1 through the primary inductor L_1 generates a voltage in the secondary inductor L_2. I–V relationship equations including input, output impedances, and transformer characteristics can be represented by

$$V_1 = Z_{\mathrm{in}} I_1 = \left(R_{\mathrm{in}} + jX_{\mathrm{in}}\right) I_1 \tag{6}$$

$$V_2 = Z_{\mathrm{load}} I_2 = \left(R_{\mathrm{load}} + jX_{\mathrm{load}}\right) I_2 \tag{7}$$

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} R_1 + j\omega L_1 & -j\omega M \\ j\omega M & -R_2 - j\omega L_2 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{8}$$

where Z_{in} is the input impedance, Z_{load} is the output impedance, and M is the mutual inductance. For ease of manipulation, all I and V have been represented in terms of I_1 as follows:

$$\begin{aligned} V_1 &= (R_1 + j\omega L_1) I_1 - j\omega M \frac{j\omega M I_1}{Z_{\mathrm{load}} + R_2 + j\omega L_2} \\ &= \left[R_1 + j\omega L_1 + \frac{\omega^2 M^2}{Z_{\mathrm{load}} + R_2 + j\omega L_2} \right] I_1 \\ &= \left\{ R_1 + \frac{\omega^2 M^2 (R_{\mathrm{load}} + R_2)}{(R_{\mathrm{load}} + R_2)^2 + (X_{\mathrm{load}} + \omega L_2)^2} \right. \\ &\qquad \left. + j \left[\omega L_1 - \frac{\omega^2 M^2 (X_{\mathrm{load}} + \omega L_2)}{(R_{\mathrm{load}} + R_2)^2 + (X_{\mathrm{load}} + \omega L_2)^2} \right] \right\} I_1 \end{aligned} \tag{9}$$

$$\begin{aligned} V_2 &= Z_{\mathrm{load}} I_2 \\ &= \frac{j\omega M Z_{\mathrm{load}}}{Z_{\mathrm{load}} + R_2 + j\omega L_2} I_1 \end{aligned} \tag{10}$$

$$I_2 = \frac{j\omega M}{Z_{\mathrm{load}} + R_2 + j\omega L_2} I_1. \tag{11}$$

From (9), the real part and imaginary parts of the input impedance are given by

$$R_{\text{in}} = R_1 + \frac{\omega^2 M^2 (R_{\text{load}} + R_2)}{(R_{\text{load}} + R_2)^2 + (X_{\text{load}} + \omega L_2)^2} \tag{12}$$

$$X_{\text{in}} = \omega L_1 - \frac{\omega^2 M^2 (X_{\text{load}} + \omega L_2)}{(R_{\text{load}} + R_2)^2 + (X_{\text{load}} + \omega L_2)^2}. \tag{13}$$

We can represent P_1, the power delivered into port 1 of the network, and P_2, the power delivered to the load as follows:

$$\begin{aligned} P_1 &= \frac{1}{2}\text{Real}\,(V_1 {I_1}^*) \\ &= \frac{1}{2} R_{\text{in}} |I_1|^2 \end{aligned} \tag{14}$$

$$\begin{aligned} P_2 &= \frac{1}{2}\text{Real}(V_2 {I_2}^*) \\ &= \frac{1}{2} R_{\text{load}} |I_2|^2 \\ &= \frac{R_{\text{load}} \omega^2 M^2 |I_1|^2}{(R_{\text{load}} + R_2)^2 + (X_{\text{load}} + \omega L_2)^2}. \end{aligned} \tag{15}$$

The transformer efficiency η is the ratio of P_2 and P_1 and the transformer loss in decibels can easily be obtained from it as follows:

$$\begin{aligned} \eta &= \frac{P_2}{P_1} \\ &= \frac{R_{\text{load}}}{R_{\text{in}}} \frac{\omega^2 M^2}{(R_{\text{load}} + R_2)^2 + (X_{\text{load}} + L_2)^2} \\ &= \frac{R_{\text{load}} \omega^2 M^2}{[(R_{\text{load}} + R_2)^2 + (X_{\text{load}} + \omega L_2)^2] R_1 + \omega^2 M^2 (R_{\text{load}} + R_2)} \end{aligned} \tag{16}$$

$$\begin{aligned} &\text{Loss (dB)} \\ &= -10 \log \eta \\ &= 10 \log P_1 - 10 \log P_2. \end{aligned} \tag{17}$$

To minimize DAT loss, X_{load} should resonate ωL_2 at the operating frequency, i.e.,

$$X_{\text{load}} = -\omega L_2. \tag{18}$$

This can be realized using a shunt capacitance in the transformer output terminal. For the case, the equation is simplified as follows:

$$\frac{P_2}{P_1} = \frac{R_{\text{load}} \omega^2 M^2}{(R_{\text{load}} + R_2)\left[R_1 (R_{\text{load}} + R_2) + \omega^2 M^2\right]}. \tag{19}$$

To obtain the optimum value of R_{load} for the minimum loss, (19) is differentiated in terms of R_{load} and the differential should be zero as follows:

$$R_{\text{load}} = \sqrt{{R_2}^2 + \omega^2 M^2 \frac{R_2}{R_1}} = R_2 \sqrt{1 + \frac{\omega^2 M^2}{R_1 R_2}}. \tag{20}$$

For the optimum R_{load}, the maximum efficiency is given by

$$\begin{aligned} \eta_{\max} &= \frac{R_{\text{load}} \omega^2 M^2}{(R_{\text{load}} + R_2)\left[R_1 (R_{\text{load}} + R_2) + \omega^2 M^2\right]} \\ &= \frac{\sqrt{1 + \dfrac{\omega^2 M^2}{R_1 R_2}} - 1}{\sqrt{1 + \dfrac{\omega^2 M^2}{R_1 R_2}} + 1}. \end{aligned} \tag{21}$$

As is already known, the quality factors Q_1 and Q_2 of the primary and secondary inductors are represented in terms of R_1 and R_2 by

$$Q_1 = \frac{\omega L_1}{R_1} \tag{22}$$

$$Q_2 = \frac{\omega L_2}{R_2}. \tag{23}$$

For the sake of simplicity, we can define a new quality factor for the mutual inductance M as follows:

$$Q_M \equiv \frac{\omega M}{\sqrt{R_1 R_2}}. \tag{24}$$

From the above equations, we can rearrange the output and input impedances for the minimum DAT loss as follows:

$$R_{\text{load}} = R_2 \sqrt{1 + Q_M^2} \tag{25}$$

$$X_{\text{load}} = -\omega L_2 \tag{26}$$

$$R_{\text{in}} = R_1 \left[1 + \frac{Q_M^2}{1 + \sqrt{1 + Q_M^2}}\right] \tag{27}$$

$$X_{\text{in}} = \omega L_1. \tag{28}$$

The load impedance originates from antenna impedance, typically 50 Ω, and the input impedance should be matched to the transistor output impedance. Using a shunt capacitance and bonding wire at the transformer output terminal, 50 Ω, typical antenna impedance, can be easily converted to the optimum output impedance and, using a shunt capacitance at the transformer input terminal, the transformer input impedance can be converted to the transistor impedance. In some cases, a further structure optimization can be applied to obtain better values of L_1, L_2 and M, which make the above impedance converting easier at the expense of a slight transformer loss. By applying the mutual quality factor Q_M to (21), the maximum efficiency can be represented as follows:

$$\eta_{\max} = \frac{\sqrt{1 + Q_M^2} - 1}{\sqrt{1 + Q_M^2} + 1}. \tag{29}$$

This is a monotonously increasing function of Q_M. Therefore, to obtain maximum efficiency, we must have Q_M as high as possible. The mutual inductance m is closely related to the amount of magnetic coupling between two loops and the strength of the

magnetic field inside the secondary loop. Hence, we can represent m as $M \propto A/L_d$, where A is a secondary loop area and L_d is the effective distance from the primary loop to the center of the secondary loop. To calculate m precisely, an accurate model of m is needed, but we want to verify the loss difference between the novel DAT and the conventional one. Hence, the only important factor is not the exact value of Q_M, but the ratio of Q_M for the two cases, and Q_M, for this purpose, can be approximated as $Q_M \propto (A/L_d)(1/\sqrt{R_1 R_2})$. All parameters for calculating Q_M of the conventional DAT, A, R_1, R_2, and L_d can be approximated as

$$A_{\rm conv} = \left[L_t - 2(W_p + W_s + W_g)\right]^2 \tag{30}$$

$$R_{1\rm conv} = \frac{4\rho(L_t - W_p)}{W_p} \tag{31}$$

$$R_{2\rm conv} = \frac{4\rho(L_t - 2W_p - 2W_g - W_s)}{W_s} \tag{32}$$

$$L_{d\rm conv} = \frac{1}{2}(L_t - W_p). \tag{33}$$

The widths and lengths are properly described in Fig. 6(a) and (b). Considering that half of the primary loop is covered with an air bridge, the parameters of the new type of DAT can be represented as

$$A_{\rm new} \cong A_{\rm conv} \tag{34}$$

$$R_{1\rm new} = \frac{2\rho(L_t - 2W_p - 2W_s - W_{pp} - 2W_g)}{W_p + W_s + W_{pp} + 2W_g} + \frac{2\rho(L_t - W_p)}{W_p} \,\|\, \frac{2\rho(L_t - 2W_p - 2W_s - 4W_g - W_{pp})}{W_{pp}} \tag{35}$$

$$R_{2\rm new} \cong R_{2\rm conv} \tag{36}$$

$$L_{d\rm new} = \frac{1}{4}(2L_t - W_p - W_s - 2Wg - W_{pp}). \tag{37}$$

For the sake of simplicity, we omit all subscripts representing "conv" or "new" and we define another parameter, i.e., χ, to represent the ratio of mutual quality factor of the new type DAT $Q_{M\rm new}$ to that of the conventional DAT $Q_{M\rm conv}$ as follows:

$$\chi \equiv \frac{Q_{M\rm new}}{Q_{M\rm conv}} = \frac{A_{\rm new} L_{d\rm conv}\sqrt{R_{1\rm conv} R_{2\rm conv}}}{A_{\rm conv} L_{d\rm new}\sqrt{R_{1\rm new} R_{2\rm new}}}. \tag{38}$$

By inserting fabrication parameters, χ can be calculated as

$$\chi = \frac{L_{d\rm conv}\sqrt{R_{1\rm conv}}}{L_{d\rm new}\sqrt{R_{1\rm new}}} \cong 1.9. \tag{39}$$

The losses of DATs are calculated as a function of $Q_{M\rm conv}$ and depicted in Fig. 8(b). Around $Q_{M\rm conv} = 35$, the loss of the conventional DAT is approximately 1.6 dB, and that of the new DAT with $\chi = 1.9$ is 0.9 dB, a 0.7-dB improvement at 2 GHz. This result agrees very well with the measured results shown in Fig. 7(b). We have simulated the above structure with a metal resistivity of 6.1 mΩ/sq, 4 mΩ lower than fabricated one, and the result shows that the loss of the conventional DAT is approximately 1.0 dB, and that of the new DAT is 0.57 dB, a 0.43-dB improvement. This result agrees with the calculated result shown in Fig. 8(b), which is around $Q_{M\rm conv} = 75$. The metal resistivity can be achieved easily with a thicker layer. Although we have carried out experiments using the GaAs DAT, one can apply our results to the DAT on an Si substrate because the only difference between the two DATs is the substrate loss, which is related to Q_M.

IV. Conclusions

Two ideas that drastically improve DAT performances have been represented and also realized. Using the grounded guard lines along the feed lines, the feed line can be isolated from the strong magnetic field generated by the DAT. The measurement data shows approximately 10.5-dB improvement using the proposed structure. Using the air-bridge connected double primary DAT structure, the DAT loss can be reduced significantly without any increase in the DAT area. Measured results shows 0.72-dB loss reduction at 2 GHz.

References

[1] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Fully integrated CMOS power amplifier design using distributed active-transformer architecture," *IEEE J. Solid-State Circuits*, vol. 37, pp. 371–383, Mar. 2002.

[2] ——, "Distributed active transformer: A new power combining and impedance transformation technique," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 1, pp. 316–331, Jan. 2002.

[3] D. K. Cheng, *Field and Wave Electromagnetics*. Reading, MA: Addison-Wesley, 1989.

[4] *Sonnet Suite User's Manual*, 8.52 ed., vol. 1, Sonnet Software Inc., Liverpool, NY, 2002.

[5] *Advanced Design System 2001 User's Guide*, Agilent Technol., Palo Alto, CA, 2001.

[6] W. K. Chen, *The Circuits and Filters Handbook*. Boca Raton, FL: CRC, 1995.

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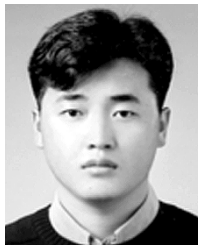

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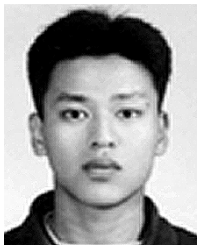

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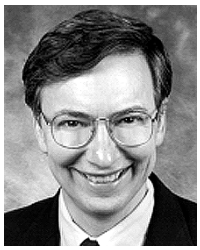

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