[6]. The unknown equivalent electric current on the dipole surface

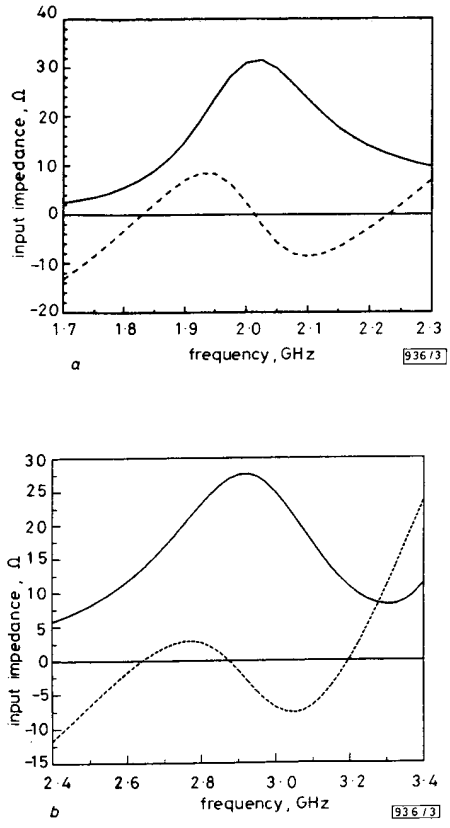

Fig. 3 *Input impedances for half-split CDRA*

ε_r = 8.9, h = 3.0cm, a = 2.25cm, a_w = 0.0118cm
a TE_{01} mode with x_f = 1.6cm, z_f = 0.0cm, and l_f = 1.25cm
b HEM_{12} mode with $x_f = z_f$ = 0.0cm, and l_f = 0.838cm

is modelled as piecewise linear subdomain functions [3]. After application of a Galerkin procedure to the integral equations, the resulting MoM matrix is solved for the current distribution on the wire and the input impedance is computed from the current at the driving source. Other parameters such as the radiation pattern and the near field distribution can also be obtained.

Numerical results: Excitation of the TE_{01} mode of the antenna of Fig. 1 will result in a broadside radiation pattern. This broadside radiation pattern is similar to the radiation pattern of a narrow slot in a ground plane. Excitation of the HEM_{12} mode results in a radiation pattern with a null along the *y*-axis. The radiation patterns for the TE_{01} and HEM_{12} modes for the split cylindrical dielectric disc of Fig. 1 with a = 2.25cm, h = 3.0cm and ε_r = 8.9 are plotted in Fig. 2*a* and *b*, respectively. A monopole of radius a_w = 0.0118cm and length l_f = 1.25 and positioned at x_f = 1.6cm, z_f = 0.0 was used to excite the TE_{01} mode. The input impedance of this mode is plotted as a function of frequency and is shown in Fig. 3*a*. To assure the convergence of the numerical solution, azimuthal modes from –2 to +2 are included in this analysis. The impedance level can be controlled by adjusting the length and position of the dipole. To properly excite the hybrid HEM_{12} mode, the probe length and position were adjusted to l_f = 0.838cm and $x_f = z_f$ = 0. in this position, only the ±1 azimuthal modes are excited. The input impedance is plotted as a function of frequency in Fig. 3*b*.

The computed resonance frequencies and the radiation Q factors were computed in the complex plane without excitation and are, respectively, 2.033GHz and 7.7 for the TE_{01} and 3.021GHz and 6.25, for the HEM_{12} mode.

Summary: A numerical design tool has been used to design a half-split CDR antenna excited by a coaxial probe which promises improved bandwidth, radiation efficiency, and power handling capabilities as compared to conventional microstrip and slot-coupled transmission line antennas. Although results were presented only for the TE_{01} and HEM_{12} modes, other quasi-TE modes can be excited using this configuration.

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Computing centroids in current-mode technique

M. Tartagni and P. Perona

Indexing terms: Circuit design, Analogue computer circuits

A novel current-mode circuit for calculating the centre of mass of a discrete distribution of currents is described. It is simple and compact, an ideal building block for VLSI analogue IC design. The design principles are presented as well as the simulated behaviour of a one-dimensional implementation.

Introduction: The idea of using resistive sheet or grids of linear resistors to determine the position of objects, a small bright spot for example, is not new and has been used in earlier systems [1]. More complex analogue VLSI chips have also been proposed to find the centroid and higher-order moments [2]. Analogue designs overcome the problem, critical for real-time system operation, of the significant A/D conversion overhead required by digital systems. However, a number of difficulties remain:

(i) so far, linear resistive sheet implementations require either complex area-expensive circuitry, or technology-dependent solutions that are not electronically tunable;

(ii) the computation of the centroid often requires off-chip processing using sophisticated buffers;

(iii) they do not work well for very low levels of injected current, thus preventing direct interface of photodiodes with resistive grids for low light levels.

The above-mentioned problems led us to investigate a new circuit technique using a current-mode approach [3]. This Letter presents a novel CMOS circuit using a current-mode subthreshold MOS approach [4] that is simple, requires little area, does not require off-chip processing, works well with small currents and has low power consumption.

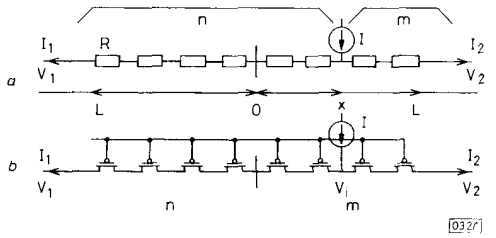

Fig. 1 *Current dividers*

Circuit description: The well known idea underlying our position-sensitive device is described in Fig. 1*a*. For a discrete 1-D resistive network it may be proved that the relative position x/L of current injection is related to the boundary currents I_1, I_2 and voltages V_1, V_2 by the following expression:

$$\frac{x}{L} = \frac{n-m}{m+m} = \frac{I_2 - I_1}{I_2 + I_1} + 2\frac{V_2 - V_1}{(n+m)IR} \qquad (1)$$

where n and m are the number of elements on the left- and right-hand sides of the injection node, R is the single-element resistance value and L is the half-length of the structure as illustrated in Fig. 1*a*. It can be seen from the above equation that if $V_1 = V_2$ the position may be calculated by means of a simple fractional function of the output currents independently of the value of the node voltages. However, owing to the intrinsic differences of device characteristics, a sufficiently accurate matching of the boundary voltages is difficult to achieve, making the position estimation through the function $(I_2 - I_1)/(I_2 + I_1)$ accurate only for high values of R and/or I. Thus the requirement to keep R high is extremely important for low values of injected current, but hard to meet in VLSI by using either passive layers or complex circuit strategies. To overcome this limitation we propose the solution described in Fig. 1*b*, where each resistor has been substituted by an MOS transistor. Assuming the general current expression of an MOS transistor $I_D = K\,(f(V_G, V_D) - f(V_G, V_S))$ it is easy to show that

$$\frac{x}{L} = \frac{n-m}{m+m} = \frac{I_2 - I_1}{I_2 + I_1} + 2\frac{K(f(V_G, V_2) - f(V_G, V_1))}{(n+m)I} \qquad (2)$$

where K is the channel width to length ratio. Note that the current division technique is valid in all operating regions of an MOS transistor: weak and strong inversion, linear region and saturation as recently reported also in [5]. For example, referring all voltages to bulk, the value of $f(V_G, V_P)$ for *p*MOS transistors working in weak or strong inversion is $I_0\exp(-\kappa V_G + V_P/U_T)$ or $\mu C_{ox}/2\kappa\ (\kappa(-V_G + V_T) + V_P)^2$, respectively, where V_P could be either V_D or V_S, κ is the gate effectiveness coefficient, related to the body effect, and U_T is the thermal voltage. Furthermore, note that eqn. 2 is still consistent for MOSFETs in moderate inversion, whatever is the expression of $f(V_G, V_P)$.

This implementation offers the capability of controlling the voltage-dependent term of eqn. 2 simply by adjusting the level of V_G, thus determining the resistivity of the network, which trades off time response for boundary offset cancellation. It is easy to see that for both networks, in the presence of multiple inputs and assuming $V_1 = V_2$, the output currents encode the normalised first moment $\bar{x}/L$ of the current distribution:

$$\frac{\bar{x}}{L} = \frac{1}{L}\frac{\sum_{x=-L}^{L} I(x)x}{\sum_{x=-L}^{L} I(x)} = \frac{I_2 - I_1}{I_2 + I_1} \qquad (3)$$

In order to calculate the $(I_2 - I_1)/(I_2 + I_1)$ function we propose using the translinear principle in a circuit with subthreshold MOSFETs (Fig. 2). Two current-controlled current conveyors consisting of the two pairs *M*0-*M*1 and *M*10-*M*11 ensure equal magnitude to V_1 and V_2 while the currents flowing out of the resistive network are delivered at the drain of *M*5 and *M*6, avoiding any current-mirror mismatch. Applying the translinear principle to the loop of *M*3, *M*4, *M*5 and *M*6 we can prove that $I_{D5}\,I_{D4} = I_{D3}\,ID_6$; hence $I_o = I_b(I_2 - I_1)/(I_2 + I_1)$, giving the required function normalised to the biasing current of the differential pair I_b. Finally, note how the above approach and the current-division technique are not directly constrained by power supply margins, an attractive feature for low-voltage applications.

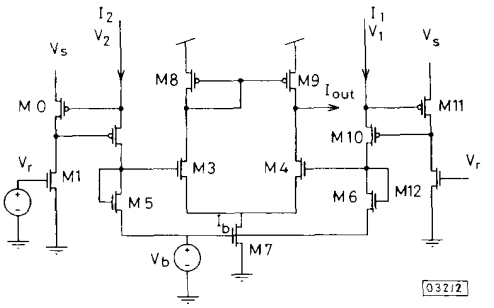

Fig. 2 *Computational circuit*

Circuit evaluation: The proposed architecture has been simulated by using ANALOG [6] which is particularly tailored for evaluating MOSFET circuits working in mixed operating regions. A 13-node current divider, along with the proposed computational block, has been simulated with typical parameters of a general-purpose 2μm CMOS process. All transistors have the same size W/L = 4μm/4μm to ensure maximum compactness to the structure. In Fig. 3 the output current is plotted against the centre of

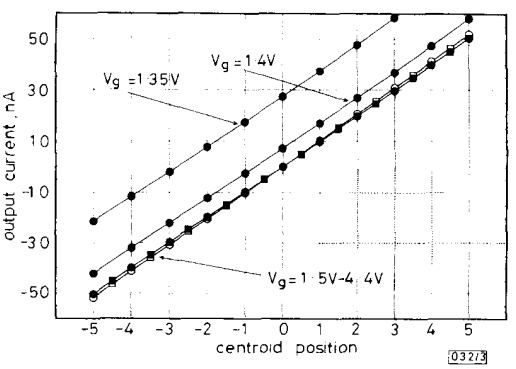

Fig. 3 *Steady-state position characteristics*

V_1 = 2.88V, V_2 = 2.38V, V_r = 0.6V, V_b = 0.747V

O, u 10nA
●,■ 10pA

mass position of the input distribution assuming a 50mV offset between V_1 and V_2. The circle marked characteristics belong to a three-current pattern whose centroid corresponds to the indicated node while the square marked characteristic is related to a four-current pattern whose centre of mass is aligned to an internode position. The circuit has been simulated for different values of V_G, in the range 1.35–4.4V (voltages referred to ground) to evaluate the current division performance for different transistor operating regions and to analyse the offset cancellation effect as predicted by eqn. 2. Note that the linearity of the characteristic is not affected by the transistor working region, and that the offset effect gradually decreases for increasing values of V_G. For all characteristics we have observed high linearity with correlation coefficient deviation below 0.01%. Fixing V_G in the range 1.5–4.4V, we then varied the total amount of input current over three decades, from 20pA/ (solid markers) to 20nA/ (open markers), obtaining a small variation (<1.5%) of static characteristics. The lower limit is set by the leakage currents of diffusions and the upper one by the strong

inversion operation of the computational block transistors.

Conclusions: W have investigated a new technique for locating in analogue fashion the centre of mass of a discrete distribution of currents using current-mode concepts. The simulation results presented above, which exhibit high linear characteristics over three decades of input values, indicate that this architecture has application versatility in the design of position-sensitive devices (PSD), D/A conversion systems and neural networks. Analysis of similar architectures in BiCMOS technology is currently in progress to overcome time-response requirements.

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Novel PLL-based clock distribution scheme

S.H.K. Embabi and K.I. Islam

Indexing terms: Clocks, Phase-locked loops

A technique for minimising clock skew in VLSI chips and multichip modules is proposed. A phase-locked loop is used to tune the delay of the clock interconnects. Negative, zero and positive delays can be achieved. This allows for clock synchronisation between individual modules with locally optimised clock distribution to minimise global clock-skew.

Introduction: The throughput of synchronous processors can be enhanced by reducing the clock cycle time [1]. The cycle time can be reduced by decreasing the delays of flipflops and logic blocks in the signal path. This has been achieved by scaling down the device feature size and through other technological breakthroughs. The remaining factor which has not been given enough attention until recently, is the skew time. The skew time must be within 10% of the cycle time [2] to prevent race conditions.

Several strategies which have been proposed to minimise clock skew revolve around *RC* balancing techniques (e.g. H-tree [3]). These techniques, however, are unsuitable for asymmetric distribution of synchronous elements and become complex when used recursively for clock synchronisation on larger chips. A skew reduction strategy which lends itself particularly well to the hierarchical nature of VLSI design is the Friedman–Powell scheme [4]. In this scheme, the master clock source is first buffered to drive the central clock buffers. Parallel connections carry the clock signal from the centralised clock buffer to each of the functional elements (FEs). The clock distribution within each FE is assumed to be locally optimised. The global skew is minimised by compensating for the differences in the phase delays [see note 1] of the different FEs through parameterising each of the FE's clock buffers in the central clock buffer. This skew minimisation technique is inherently susceptible to drift in the transistor characteristics brought on by process and environmental variations.

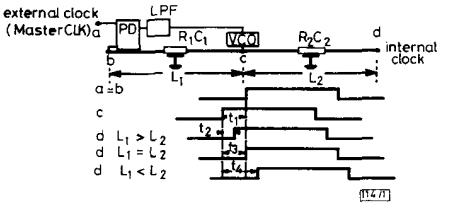

Fig. 1 *PLL system with remote VCO to control the delay between the clock at d with respect to the reference clock at a*

PLL-based clock distribution: The clocking strategy outlined in this Letter is based on the Friedman–Powell scheme [4]. However, a phase locked loop (PLL) with a remote voltage controlled oscillator (VCO) is used to compensate for the phase delay of individual FEs. The concept of a PLL with a remote VCO is first discussed followed by its application for an on-chip clock distribution scheme. Assume that the master clock (see Fig. 1) is to be carried from point *a* to point *d* via an interconnect *L* μm long ($L = L_1 + L_2$). The delay of that line is proportional to the *RC* product of the interconnect. Hence, the clock signal is skewed by the amount of that delay. If, however, a PLL is used as shown in Fig. 1, where the phase detector (PD) and the lowpass filter (LPF) are kept in the proximity of the clock source, and the VCO is remotely located such that its output taps the line at its middle point *c* (i.e. $L_1 = L_2$), the delays of the two halves will be equal. The clock at point *c* will be leading the clock at *a* (and *b*) by t_1 which is proportional to R_1C_1. Because $R_2C_2 = R_1C_1$, the delay between point *c* and *d* is equal to that between *c* and *a*. Hence, the skew between *a* and *d* is ideally zero as opposed to twice t_1 if the PLL is not used. By the same token, if the tapping point *c* is shifted to the right or left, an intentional skew can be introduced. For example if $L_1 > L_2$, the delay between *c* and *b* will be greater than that between *c* and *d*; hence, the clock at *d* leads the clock at *a* as shown in Fig. 1. This implies that the skew achieved is negative, which is an interesting result. The opposite case is also illustrated in Fig. 1. This approach can be used to tune the intra-element delay, an effect achieved by the individual sizing of buffers in the Friedman–Powell scheme [4]. Fig. 2 illustrates this application. Let us assume that

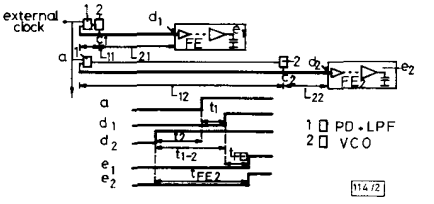

Fig. 2 *Compensation of phase delay of FEs using PLL-controlled intra-element interconnects*

the phase delays of functional elements FE_1 and FE_2 are t_{FE1} and t_{FE2} respectively, with $t_{FE1} < t_{FE2}$. To avoid skewing between e_1 and e_2, the delay of the first interconnect (*a* to d_1) should be larger than that of the second interconnect (*a* to d_2). This requirement contradicts the fact the length of the first interconnect is shorter than that of the second. However, using negative skewing by proper positioning of the remote VCO, the clock at d_2 may be made to lead the reference *a* by t_2 and the clock at d_1 to lag the reference by t_1. The net result of this arrangement is that the clock at d_1 lags the clock at d_2 by $t_{1\text{-}2}$, which is equal to $t_1 + t_2$. If $t_{1\text{-}2}$ equals $t_{FE2}-t_{FE1}$, the skew between e_1 and e_2 is zero. The condition

Note 1: The phase delay is the maximum delay between the master clock source and any leaf node