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Organic field-effect transistors with nonlithographically defined submicrometer channel length

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We developed an underetching technique to define submicrometer channel length polymer field-effect transistors. Short-channel effects are avoided by using thin silicon dioxide as gate insulator. The transistors with **1** and **0.74** μm channel length operate at a voltage as low as 5 V with a low inverse subthreshold slope of **0.4–0.5** V/dec, on–off ratio of $\mathbf{10^4}$, and without short-channel effects. The poly(3-alcylthiophene)'s still suffer from a low mobility and hysteresis does occur, but it is negligible for the drain voltage variation. With our underetching technique also device structures with self-aligned buried gate and channel length below **0.4** μm are fabricated on polymer substrates. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1758775]

Organic field-effect transistors (OFETs) are of interest for many applications including organic displays, complementary circuits, and all-polymer integrated circuits.[1–3] Low-cost fabrication requires the use of solution-processible polymers instead of vacuum deposited low-molecular weight organics. Although mobilities of up to 0.1 $cm^2/V\,s$ have been demonstrated for soluble regioregular poly(3-alkylthiophene),[3,4] poly-(9,9-dioctylfluorene-bithiophene),[5] and pentacene from soluble precursors,[6] OFETs needed for high-performance circuits still require extremely small gate length to be modulated at competitive frequencies. The cut-off frequency $f_0 = g_m/(2\pi C_{GS})$ is determined by the maximum transconductance g_m and the gate–source capacitance C_{GS}. Neglecting parasitic capacitances, the latter is approximated by the gate oxide capacitance. Using the simple Shockley current characteristics one obtains as an estimation $f_0 < \mu U_{GS,\mathrm{eff}}/(2\pi L^2)$, where $U_{GS,\mathrm{eff}}$ is the gate-source voltage relative to the threshold voltage. With a voltage of at most 10 V, a realistic upper value of 0.01 $cm^2/V\,s$ for the mobility and a lower limit for the cut-off frequency of 100 kHz, one obtains as an upper limit for the channel length $L < 4\ \mu$m. Since additional parasitic capacitance cannot be avoided, only submicrometer devices lead to applicable circuits. Demonstrations of different patterning techniques such as screen printing,[7] soft lithographic stamping,[8] or inkjet printing[9] have so far not demonstrated both resolution and alignment accuracy desired. Photolithography[2] is expected to be costly for the submicrometer regime. Recently, Stutzmann *et al.*[10] used embossing to fabricate vertical-channel field-effect transistors with submicrometer channel lengths, but could not observe saturation in the measured output characteristics. These authors also presented a self-aligned gate structure with reduced overlap capacitance. We demonstrate the fabrication of submicrometer field-effect transistor channels by employing an underetching technique for submicrometer patterning, to enable the use of low-resolution photolithographic steps and standard microelectronic processes.

Transistor design and dimensions are closely related to the material properties. At first, in order to reach the off-state and saturation, the active layer thickness must be less than the depletion length.[11] We use poly(3-octylthiophene) (P3OT) and poly(3-hexylthiophene) (P3HT), which are both unintentionally highly doped (of the order $10^{17}\ cm^{-3}$ Refs. 11–13). To successfully deplete the layers their thickness must be of the order of 30 nm or less, which can be achieved by controlling the solution concentration and the spin-coating process.[11] Down-scaling comprises also the gate insulator thickness in order to avoid short-channel effects. They have been analyzed by two-dimensional simulations (method and standard parameters are described in Refs. 12 and 14). With an organic insulator (poly-4-vinylphenol, P4VP) thickness of 400 nm one can prevent leakage currents, but the simulated output characteristics show saturation only for channel length larger than 1 μm and a large supralinear current for shorter channels. A reduction of the insulator thickness down to 50 nm for devices with 0.5 and 0.3 μm channel length reduces this effect sufficiently. Since such organic insulators are not yet available, we demonstrate the short-channel OFET fabrication here with a hybrid structure: The gate insulator is a 30 nm silicon dioxide layer on a n^+-silicon wafer serving as the gate electrode.

Undercutting is a phenomenon well known in microelectronics[15] and usually occurs unintentionally leading

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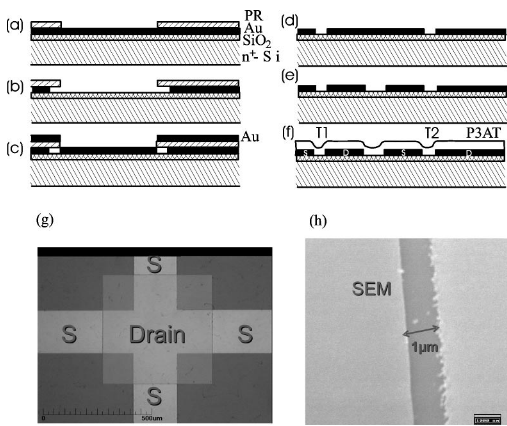

FIG. 1. Fabrication steps for the OFET (a)–(f), cross section of two transistors T1 and T2 (f), optical micrograph (g), and a SEM image of the transistor with $L = 1\ \mu$m.

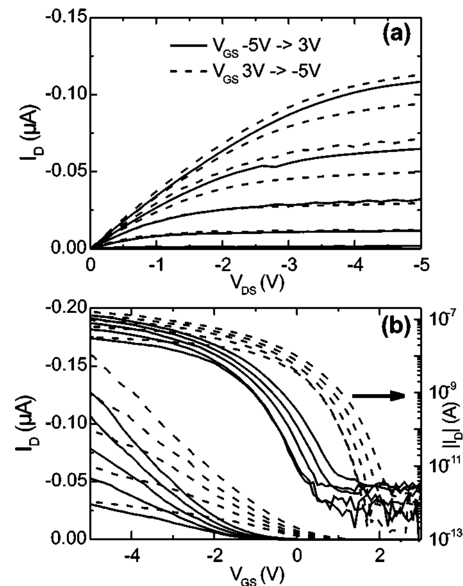

FIG. 2. Output (a) and transfer characteristics (b) on a linear and logarithmic scale for a P3HT OFET with $L = 0.88\ \mu$m, $w = 2000\ \mu$m. For the output characteristics the gate-source voltage is varied as $-5(1)3$ V and back as $3(-1)-5$ V, depicted are the curves between -5 and 0 V. For the transfer characteristics the drain-source voltage is varied as $-7(1)-1$ V. For each V_{DS} the gate-source voltage is varied from $V_{GS} = -5$ to 3 V and back from 3 to -5 V.

to an increased effective channel length.[16] We used underetching technique, in combination with low-resolution photolithographic steps and further standard microelectronic processes, for the inexpensive and manufacturable definition of the submicrometer channel length devices. The following fabrication steps are carried out. First, a large-area gold layer is sputtered (50 nm) on top of the oxidized highly doped silicon wafer. Then a low-resolution photolithographic step is used to fabricate a structured photoresist layer [Fig. 1(a)]. Subsequently, a wet chemical etching and underetching is applied to remove the gold. We have systematically investigated this etch process to determine the etch rate of gold on different substrates. As a result, the underetched length can be controlled in the submicrometer region and ultimately defines the channel length of the transistor [Fig. 1(b)]. To complete the source/drain structure, a 10-nm-thick chromium and 40-nm-thick gold layer are evaporated [Fig. 1(c)] followed by a lift-off process to remove the photoresist [Fig. 1(d)]. A separation step [Fig. 1(f)] defines an addition electrode by low-resolution photolithography and an etch step. Finally, the active organic layer of a thickness $\sim$30 nm is deposited (unpatterned). An example for the cross section of the resulting structure is depicted in Fig. 1(f). For the photolithographic steps, we used a mask layout realizing transistor channels with different widths w in the range of 200 up to 2000 μm. The optical micrograph [Fig. 1(g)] shows the source and drain regions as well as the 200 μm channel situated in between. In the scanning electron microscopy (SEM) image [Fig. 1(h)] the source and drain are again visible and separated by a 1 μm channel length. Considering the uniformity of the channel, even for shorter channels (few hundred nonometers) the variation of the prepared channel length remains small over the channel width.

The output characteristics for an OFET with P3HT ($\approx$30 nm) as active layer, channel length $L = 0.88\ \mu$m, and width $w = 2000\ \mu$m [Fig. 2(a)] indicate high performance with the following peculiarities: (i) The transistor operates at the desired voltage below 5 V. (ii) There is a clear transition into saturation indicating that short-channel effects are almost suppressed in the device. From the transfer characteristics [Fig. 2(b)] one obtains (iii) an approximately linear slope in the active region indicating that the contact resistances are negligible (a small curvature at lower drain voltages is seen for the sweep from positive to negative gate voltage, since this curvature does not occur in the opposite sweep direction, it is unlikely to be caused by contact effects and is probably related to hysteresis), (iv) a high on–off ratio (larger than 10^4), and (v) a low inverse subthreshold slope of $S \approx 400$ mV/dec. This performance compares well with the usually unfavorable high values of several V/dec in OFETs.[12,17,18] In all cases, S is larger than estimated solely from the insulator thickness. This deviation may be caused by recharging of interface states.[12] Since we focused on the short-channel fabrication, regioregular P3HT for the active layer was used, purified (by Dr. S. Janietz, IAP Golm, Germany) but without special steps for higher ordering. Correspondingly the hole mobility estimated from the current characteristics is with $\mu \approx 3 \times 10^{-5}$ cm^2/V s below the best values mentioned above. We also observe the hysteresis which is well known for OFETs,[14,19,20] but which can be reduced by using a higher-mobility polymer for the active layer as in Ref. 10. However, the hysteresis occurs only in the gate voltage sweep and the difference between the threshold voltages for up and down sweeps of the gate-source voltage is less than 1.5 V for a given drain voltage, much smaller than usually reported. We observe also a drain-source voltage dependence of the subthreshold current, typically attributed to short-channel effects, that can be also caused by rechargeable interfaces or bulk traps.[12,13] For devices with P3OT similar properties are obtained.

With the underetching technique, the channel length can be defined in a controlled manner well below $L = 1\ \mu$m. Figure 3 shows the output characteristics of a P3HT OFET with channel length $L = 0.74\ \mu$m and with $w/L \approx 1350$. The main features are the same as before, with mobility $\mu \approx 4 \times 10^{-5}$ cm^2/V s. The hysteresis resulting from the variation of the gate voltage sweep direction does occur again. How-

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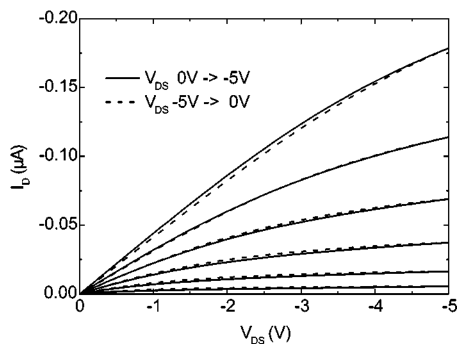

FIG. 3. Output characteristics for a P3HT OFET with $L=0.74$ μm, $w=1000$ μm. The gate-source voltage is varied as $-5(1)0$ V. For each V_{GS} the drain-source voltage is varied from $V_{DS}=0$ to -5 V and back from $V_{DS}=-5$ to 0 V.

ever, in Fig. 3 now the influence of the drain voltage sweep direction is shown. For each gate voltage the drain voltage is varied from 0 to -5 V and back from -5 to 0 V. In this case practically no hysteresis is observed, similar to Ref. 10. A possible asymmetry in the $I-V$ characteristics due to the differently prepared contacts was investigated by switching source and drain. The difference in the drain current is very small and it is partly covered by the hysteresis in subsequent measurements.

Underetching in combination with low resolution lithography and simple lift-off processing enables the efficient fabrication of organic field-effect transistors with well-defined and controllable channel lengths in the submicrometer region. Hybrid-design transistors feature low voltage operation, saturation, negligible short-channel effects, high on–off ratio, and low inverse subthreshold slope. A small hysteresis does occur only for the gate voltage sweep. It is expected to become sufficiently small by using improved polymers[3–6,10] with higher mobilities.

All-organic circuits must ultimately be fabricated on plastic substrates, with an organic gate insulator, and with self-aligned gates. Furthermore, high cut-off frequencies are only possible for transistors with low parasitic capacitances. In our fabricated hybrid OFET [Fig. 1(f)] the silicon wafer is the gate leading to high overlap capacitances. As a first step, using a plastic substrate (Mylar), a self-aligned, buried gate structure has been prepared. The same technological steps as shown in Figs. 1(a)–1(e) are realized to fabricate the source/drain contacts. Subsequently, a trench between source and drain is prepared by reactive ion etching followed by gold evaporation. A SEM image of such a structure is shown in Fig. 4, with a channel length of 0.37 μm and much reduced overlap capacitances. The completion of this transistor requires solution-processable organic insulators better than available at present. For an optically transparent substrate,

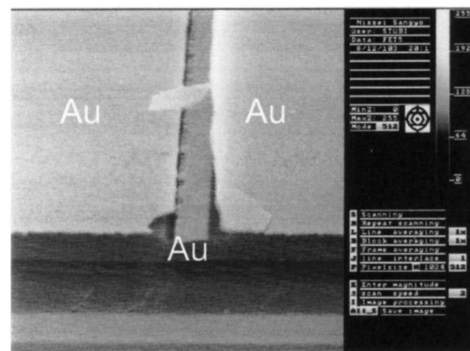

FIG. 4. Structure with a self-aligned buried gate on a plastic substrate.

the fabrication of a self-aligned gate could be accomplished by using the source and drain as opaque optical mask for the gate definition as demonstrated recently for wide-channel (20 μm) devices.[21]

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