

# An Octave-Range, Watt-Level, Fully-Integrated CMOS Switching Power Mixer Array for Linearization and Back-Off-Efficiency Improvement

Shouhei Kousai, *Member, IEEE*, and Ali Hajimiri, *Member, IEEE*

**Abstract**—The power mixer array is presented as a novel power generation approach for non-constant envelope signals. It comprises several power mixer units that are dynamically turned on and off to improve the linearity and back-off efficiency. At the circuit level, the power mixer unit can operate as a switching amplifier to achieve high peak power efficiency. Additional circuit level linearization and back-off efficiency improvement techniques are also proposed. To demonstrate the feasibility of this idea, a fully-integrated octave-range CMOS power mixer array is implemented in a 130 nm CMOS process. It is operational between 1.2 GHz and 2.4 GHz and can generate an output power of +31.3 dBm into an external 50  $\Omega$  load with a PAE of 42% and a gain compression of only 0.4 dB at 1.8 GHz. It achieves a PAE of 25%, at an average output power of +26.4 dBm, and an EVM of 4.6% with a non-constant-envelope 16 QAM signal. It can also produce arbitrary signal levels down to  $-70$  dBm of output power with the 16 QAM-modulated signal without any RF gain control circuit.

**Index Terms**—Back-off efficiency, CMOS power amplifier, distortion dependence shaping, envelope restoration, linearization, overlapping, power mixer array, segmented power generation, switching operation.

## I. INTRODUCTION

DESIGN of low-cost, power-efficient, watt-level, fully-integrated power generation circuits for a non-constant envelope signal is one of the major challenges in today's wireless communication systems. Although several approaches have been proposed in the past [1]–[11], the fully-integrated CMOS power generation circuits reported thus far have low efficiency. Linear PAs are usually used to transmit such signals faithfully at the expense of power efficiency [1]–[3]. Particularly, in a CMOS process, the poor linearity of transconductance and input capacitance with large PVT variations require a large back-off, which severely degrades the power efficiency for non-constant envelope signal amplification. To gain the input signal to watt-level output power, multiple linear amplification stages are necessary and resulting in a large die area and potential stability problems. Doherty amplifiers can be used to improve the peak and

back-off efficiency, which is very important for non-constant envelope signals [4], [5]. However, the large loss and area of an on-chip phase shifter have presented a challenge to realize an efficient, low-cost, fully-integrated CMOS Doherty power amplifier. Linear amplification using nonlinear components (LINC), or out-phasing, is a way to generate a non-constant envelope signal by using nonlinear yet efficient switching power amplifiers [12]. However, similar to the Doherty amplifiers, it generally requires a phase shifter [13]. Although an out-phasing amplifier without using a shifter has been proposed at lower output power level [6], switches at the PA load can severely degrade its efficiency in a watt-level PA. Parallel processing of amplitude and phase information (e.g., EER or polar modulation) has also been proposed as a way of improving the system power efficiency [14]. It can also take advantage of CMOS digital signal processing to ease the generation of phase and amplitude modulation signals. However, many of these schemes require an efficient high-power low-frequency supply modulator to reconstruct the amplitude information [7], [8]. This can be done, for instance, using a switching DC-DC converter with its own limitations in efficiency, bandwidth, and area [15], which requires an external inductor and produces switching spurs. Even for an ideal supply modulator, the linearity is degraded by the AM-AM and AM-PM conversion due to the gate-to-drain feed-through of a switching amplifier. The output power range of the PA is also very limited [16], [17]. To achieve high output power range, PA driver amplifiers should be implemented as linear amplifiers leading to large power consumption and area. Although an envelope tracking (ET) technique can solve the problem of output power range, it still requires a DC-DC converter and it has low peak efficiency as it generally uses class-AB power amplifiers [18], [19]. At lower power levels, digitally modulated polar PAs [9]–[11] have been shown as a possible solution to render the DC-DC converter. However, it still has the problem of output power range, and out-of-band emission due to aliasing and quantization noise should be taken care of. Its implementation in a watt-level fully-integrated CMOS PA for non-constant envelope modulation has not been demonstrated yet.

This paper describes the switching power mixer array transmitter subsystem. It is a novel and efficient modulated power generation system to generate a watt-level non-constant envelope signal in a CMOS process, without using a DC-DC converter. It also overcomes the output power range problem of conventional envelope restoration (ER) systems. Section II describes the proposed non-constant envelope generation system. The circuit details of the power mixer array transmitter subsystem are discussed in Section III, followed by Section IV that explains operation modes and test setups. Finally, measurement results are presented in Section V.

Manuscript received April 28, 2009; revised August 10, 2009. Current version published December 11, 2009. This paper was approved by Guest Editor Nikolaus Klemmer.

S. Kousai is with the Toshiba Corporation, Kanagawa, Japan (e-mail: shouhei.kousai@toshiba.co.jp).

A. Hajimiri is with the California Institute of Technology, Pasadena, CA 91125 USA (e-mail: hajimiri@caltech.edu).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2009.2032271

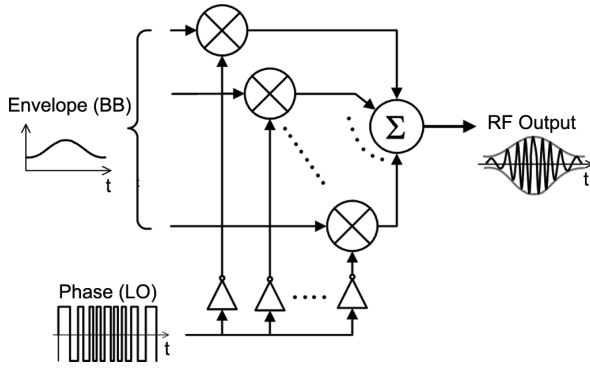


Fig. 1. Proposed power mixer array architecture.

## II. POWER MIXER ARRAY TRANSMITTER SUBSYSTEM

### A. Architecture

In order to overcome the challenges described earlier, we propose the power mixer array transmitter subsystem, whose basic concept is illustrated in Fig. 1. Power generation and amplitude modulation are done by several identical up-conversion power mixer units. The inputs of power mixer units are a phase modulated LO signal and BB envelope signal. A switching power mixer described in Section III can be utilized to obtain high peak efficiency. Identical phase modulated LO signals are buffered using logic gates (e.g., inverters) and then applied to the power mixer units. The power mixer array provides large output power range without any need for RF gain control, as we will explain in Section V. Therefore, simple digital gates such as inverters can be used to buffer the LO resulting in a small die area and low power consumption. In general, different BB input signals can be applied to different power mixer units. The output currents of the mixers are directly combined at their output. It should be noted that the power mixer array also subsumes some of the blocks typically implemented on a transceiver chip (e.g., up-conversion mixers and driver amplifiers), rendering them unnecessary.

### B. Segmented Power Generation

In this section, we will explain the advantages of the proposed *segmented power generation* scheme, in which power is generated by several identical units. The basic operation of the segmented power generation scheme is shown in Fig. 2. When a symbol requires a small output power as shown in Fig. 2(a), most of the power generation units can be turned off and the

power is generated by only few units, where one of unit is operating at an intermediate power levels to produce continuous output power level and the remaining ones are either at full power or off. Fig. 2(b) shows the operation when a symbol requires a large output power. The operation of the first power generation unit remains the same, as it produces an intermediate power, while rest of all power generation units is operating at their full power. In the segmented power generation scheme, the DC power consumption is almost proportional to the output power, as shown in Fig. 3, and thus the back-off efficiency dependence on the output power is as good as a class-B amplifier. Unlike the digitally modulated polar PA mentioned in Section I, the out-of-band emission problem due to the aliasing and quantization noise is avoided since continuous output power is generated.

Another benefit of the segmented power generation scheme is the associated linearity improvement. For a conventional power generation circuits, which has only one power generation unit, the output,  $Y_1$ , is expressed in terms of normalized input,  $x$ . For a third-order memory-less nonlinearity we have

$$Y_1(x) = \alpha_1 x + \alpha_3 x^3 \quad (-1 < x < 1) \quad (1)$$

where we assume  $\alpha_1$  and  $\alpha_3$  are real and  $x$  is the ac input signal (e.g.,  $x = A_{in} \cos \omega_1 t$ ). To understand the nonlinearity limitations, let us consider a system with two power generation units. We assume: 1) power generation unit is scaled by half; 2) the entire input is applied to a single power generation unit for  $-0.5 < x < 0.5$ ; 3) a normalized input amplitude of 0.5 is applied to one power generation unit and the other unit will see of the residue in excess of the half scale for  $0.5 < x < 1$ . Then, the output of the two-unit system,  $Y_2$ , is expressed as shown in (2) at the bottom of the page. By generalizing this idea, for a system which has  $m$  power generation units, as given in (3), also at the bottom of the next page, where  $n = 0, 1, 2, \dots, m-1$ , and  $Y_m$  is the output power of the system with  $m$  power generation unit. In (3), the maximum input level for a unit is limited to  $1/m$ . In general,  $Y_m$  is expressed as shown in (4) at the bottom of the next page, where

$$f(x) = \alpha_1 x + \alpha_2 x^2 + \alpha_3 x^3 + \dots \quad (5)$$

and  $A_0$  is the full-scale input amplitude. In (4), the maximum input level for a unit is limited to  $A_0/m$ . For example, the

$$\begin{aligned} Y_2(x) &= \frac{\alpha_1(2x-1) + \alpha_3(2x-1)^3 + \alpha_1 + \alpha_3}{2} \quad (0.5 < x < 1), \\ Y_2(x) &= \frac{\alpha_1(2x) + \alpha_3(2x)^3}{2} \quad (0 < x < 0.5), \\ Y_2(x) &= -Y_2(-x) \quad (-1 < x < 0) \end{aligned} \quad (2)$$

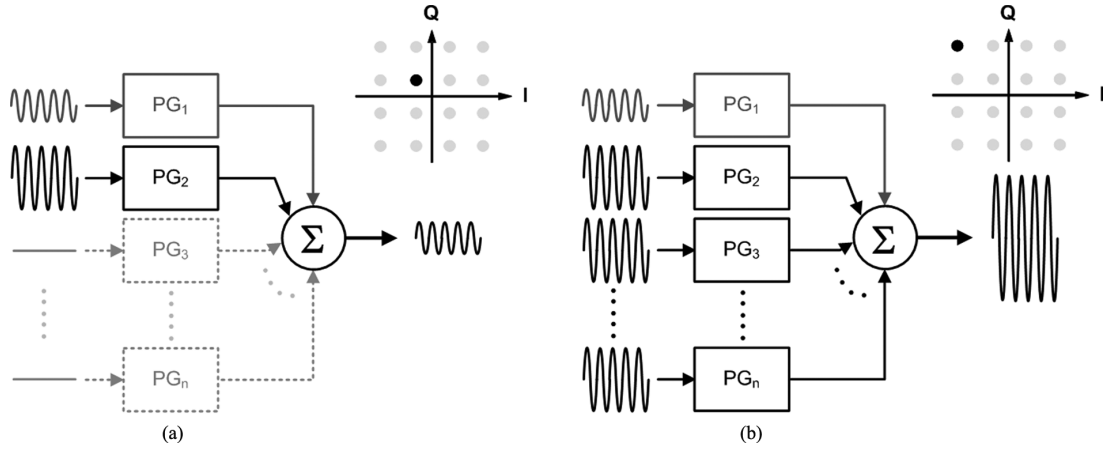


Fig. 2. Segmented power generation scheme with (a) Small output power, and (b) Large output power.

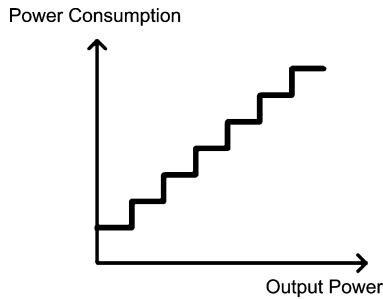


Fig. 3. Power consumption of the segmented power generation scheme.

calculated output amplitude at frequency  $\omega_1$ ,  $A_{OUT}$ , and gain,  $A_{OUT}/A_{in}$  with  $m$  of 1, 4, and 16 are plotted in Fig. 4, for

$$f(x) = 0.83x - 0.52x^3 + 0.19x^5 \quad (6)$$

and

$$x = A_{in} \cos \omega_1 t \quad (0 < A_{in} < A_0) \quad (7)$$

where  $A_{in}$  is the input amplitude. Two interesting phenomena are observed when a large number of power generation unit ( $m$ ) is used. First, integral nonlinearity (INL) improves, as the

output amplitude is almost linearly related to the input amplitude. Second, the output distortion dependence on the input is improved as the linearity at large signal levels improves substantially, whereas linearity at small signal levels degrades slightly. This can be better understood in the context of inter-modulation distortion (IMD). The IMD product is calculated by substituting

$$x = \frac{A_{in} (\cos \omega_1 t + \cos \omega_2 t)}{2} \quad (0 < A_{in} < A_0) \quad (8)$$

into (6). The output amplitude of the third order IMD product (IMD3) at frequency  $2\omega_1 - \omega_2$  or  $2\omega_2 - \omega_1$ , is plotted in Fig. 5. In a conventional system ( $m = 1$ ), the IMD3 product is a cubic function of the input amplitude. However, IMD3 product with  $m$  of 16 is almost linearly related to the input amplitude. This *distortion dependence shaping* turns out to be very effective as we consider the power distribution of modulated signal with a large number of segments as in this work.

To suppress the ripple especially at lower input levels, two techniques can be employed. First, as (4) indicates, the maximum input level of a unit,  $A_0/m$ , is scaled with the input full-scale amplitude of  $A_0$ . This guarantees that all of the units operate with full-scale input signal, and the ripple does not have a large impact on the overall linearity with a modulated signal. In addition, the unit linearity generally improves as the input level of the unit is decreased. In Fig. 4(b), the gain is plotted when  $A_0$

$$Y_m(x) = \frac{\alpha_1(mx - n) + \alpha_3(mx - n)^3 + n(\alpha_1 + \alpha_3)}{m} \quad \left( \frac{n}{m} < x < \frac{n+1}{m} \right),$$

$$Y_m(x) = -Y_m(-x) \quad (-1 < x < 0) \quad (3)$$

$$Y_m(x) = \frac{f(mx - n) + f(A_0)}{m} \quad \left( \frac{nA_0}{m} < x < \frac{(n+1)A_0}{m} \right),$$

$$Y_m(x) = -Y_m(-x) \quad (-A_0 < x < 0) \quad (4)$$

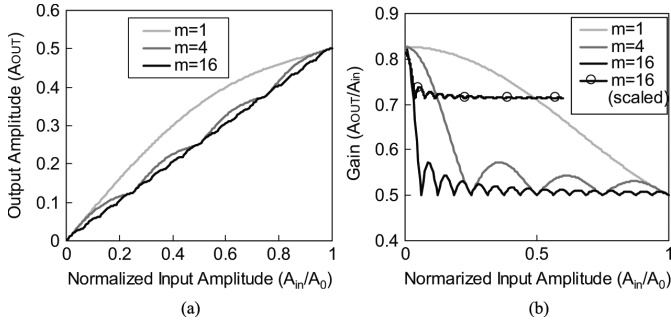


Fig. 4. (a) The output amplitude and (b) gain of the segmented power generation scheme, with  $m = 1, 4$ , and 16.

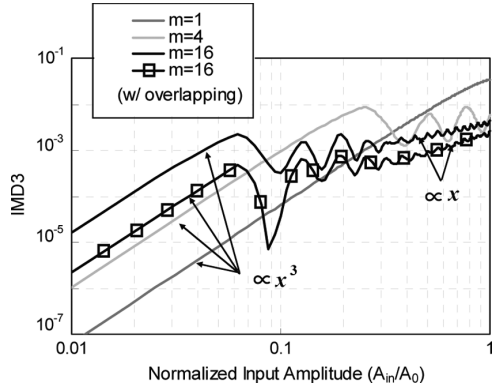


Fig. 5. IMD3 product of the segmented power generation scheme and overlapping.

is scaled to half. A second approach to improve this even further is to allow more than one unit to overlap with others in the range over which they are not at full power thereby averaging the unit nonlinearity, as illustrated in Fig. 6. The IMD3 product with the overlapping technique is plotted in Fig. 5.

To understand the effectiveness of the segmented power generation and the overlapping technique more clearly, EVM of an ideal OFDM signal is calculated using the following equation:

$$EVM = \frac{\int \rho(A_{in}) \bullet A_{out}(A_{in})|_{\omega=2\omega_1-\omega_2} dA_{in}}{\int \rho(A_{in}) \bullet A_{out}(A_{in})|_{\omega=\omega_1} dA_{in}} \quad (9)$$

where  $\rho(A_{in})$  is the probability density function of an OFDM signal in amplitude, and  $A_{out}(A_{in})|_{\omega=2\omega_1-\omega_2}$  and  $A_{out}(A_{in})|_{\omega=\omega_1}$  are the amplitude of the IMD3 product and desired signal, respectively. See (10) at the bottom of the page. Fig. 7 shows the calculated result of EVM for three systems: 1) a conventional system ( $m = 1$ ); 2) segmented power

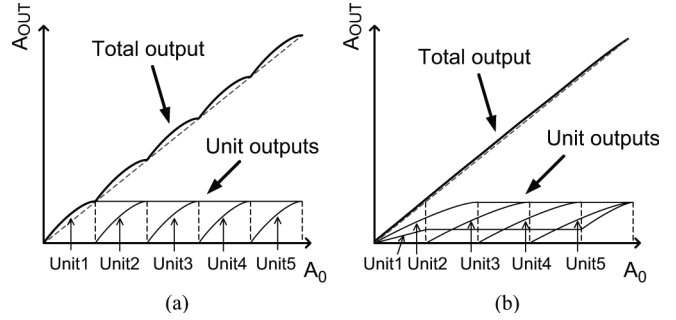


Fig. 6. Concept of the overlapping technique. (a) Without overlapping and (b) with overlapping.

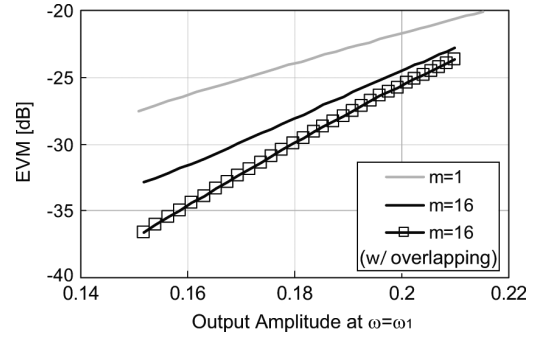


Fig. 7. Calculated EVM for an ideal OFDM signal.

generation system ( $m = 16$ ); and 3) the segmented power generation system ( $m = 16$ ) with the overlapping technique. The segmented power generation system and overlapping technique improve the EVM by 4.6 dB and 2.1 dB, respectively, at an output amplitude of 0.17.

It should be noted that the linearity improvement due to the segmented power generation is limited to input related nonlinearity, such as transconductance and input capacitance nonlinearity. Nonetheless, significant linearity improvement can be achieved since the input related nonlinearity is usually dominant in a power generation circuit. Output related nonlinearity, which is output impedance nonlinearity, is smaller than input related nonlinearity due to the large input amplitude and small output load in a power generation circuit [20].

### C. Mixers as Power Generation Units

Despite benefits of back-off efficiency and linearity improvements in the segmented power generation scheme, there is a practical issue if the units were conventional RF amplifier. Each power generation unit requires an RF input generation circuit. The amplitude of the RF input must be varied individually, while

$$A_{out}(A_{in})|_{\omega=2\omega_1-\omega_2} = |Y_m \left( \frac{A_{in}(\cos \omega_1 t + \cos \omega_2 t)}{2} \right)|_{\omega=2\omega_1-\omega_2}$$

$$A_{out}(A_{in})|_{\omega=\omega_1} = |Y_m \left( \frac{A_{in}(\cos \omega_1 t + \cos \omega_2 t)}{2} \right)|_{\omega=\omega_1} \quad (10)$$

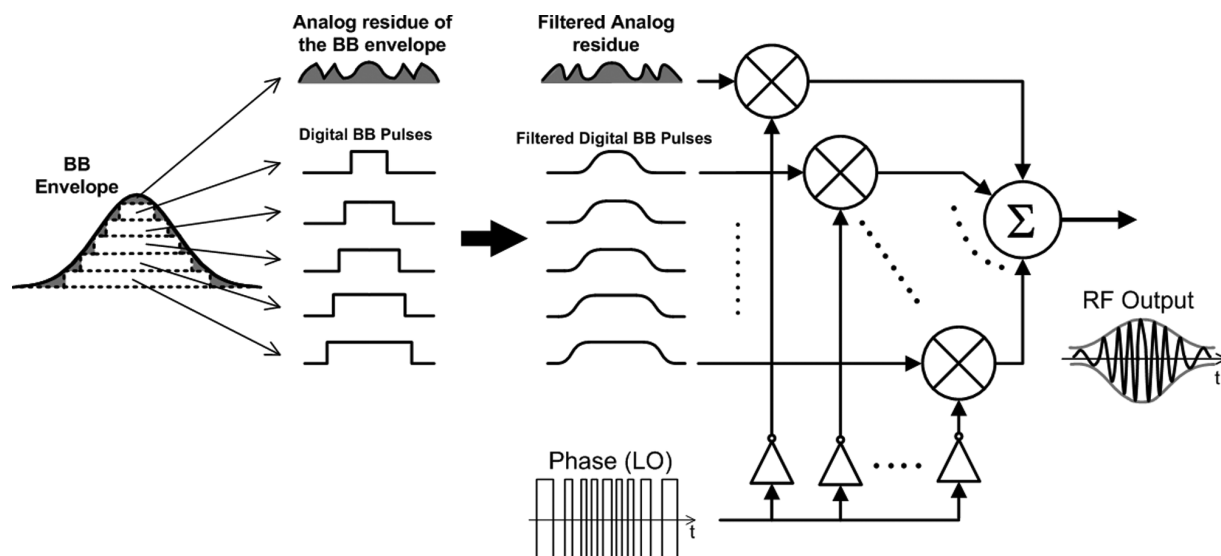


Fig. 8. The concept of power mixer input signal generation.

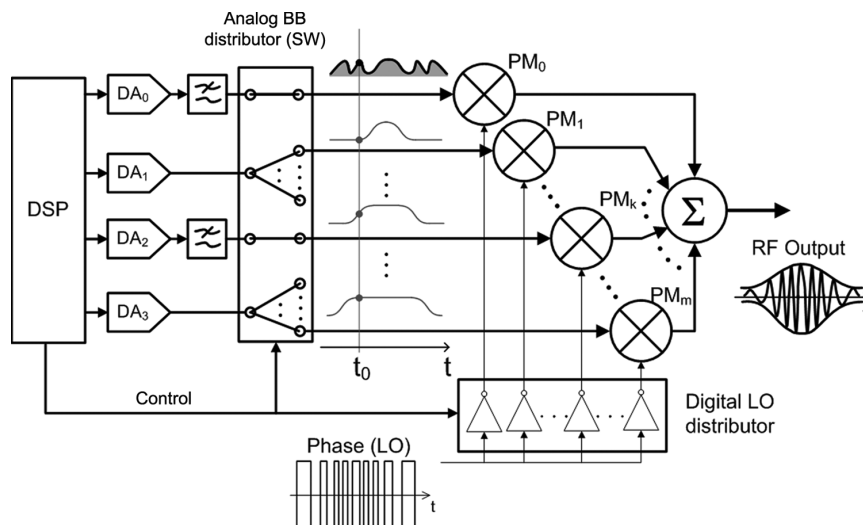


Fig. 9. Conceptual schematic of the BB input signal generation circuit.

the phase must be precisely aligned. Also, RF input signal generation circuits must be capable of well-controlled ramp-up and ramp-down to avoid spurious transient behavior, which add area and power overhead to the system. To circumvent this problem, we propose power mixers as the power generation units. The way the input RF and BB signal are used to generate a non-constant envelope RF signal is depicted in Fig. 8. A baseband envelope signal can be divided into several digital pulses and a residue part. The digital pulses can be filtered and pulse-shaped at low frequency in baseband to avoid the spurious and aliasing problems. Identical digital LO signals can be used to avoid the amplitude and phase mismatch issues of the RF input signal generation circuit. The digital LO signals are selectively applied to the power mixer unit via the digital LO distributor to dynamically shut-down unnecessary power mixer units. Then the pulses and the residue part are up-converted in frequency by the respective power mixer units, and a non-constant envelope RF signal is created at the output of the power mixer array.

The pulse or the residue part can be easily generated by a DAC followed by a LPF. Furthermore, since the input signal to the power mixer array is now at BB frequency, the DAC followed by a LPF can be shared by using a multiplexing network, as shown in Fig. 9. In our implementation a digital signal processing (DSP) circuit controls the input of four DACs, such that two DAC ( $DA_0$  and  $DA_2$ ) followed by the LPF can generate time-varying BB signals, while remaining two DACs ( $DA_1$  and  $DA_3$ ) produce BB signals of a constant voltage. The DSP circuit also controls the analog BB distributor so that the input of each power mixer unit is connected to one of the four BB signals. The input of the power mixer unit which corresponds to the residue part ( $PM_0$ ),  $DA_0$  with the LPF should always be connected to the unit, since it always operates at an intermediate power. The power mixer units which correspond to the BB pulses ( $PM_1, PM_2, \dots, PM_m$ ) are either completely on or completely off for most of the time. Therefore, the

inputs are connected to the constant voltages ( $DA_1$  and  $DA_3$ ) for the most of the time. Only for the transition time, the time varying BB signal generated by the  $DA_2$  followed by the LPF is connected to the input of the power mixer unit. At  $t = t_0$  for instance, power mixer units which produces the full power ( $PM_{k+1}, PM_{k+2}, \dots, PM_m$ ) should be connected to  $DA_3$ . The units which are turned off ( $PM_1, PM_2, \dots, PM_{k-1}$ ) should be connected to  $DA_1$ . The unit which is at transition ( $PM_k$ , where  $1 < k < m$ ) is connected to the output of the BB circuit which is consisted of  $DA_2$  followed by the LPF. As a result, two BB circuits (a DAC followed by a LPF), and two constant voltages are enough for the BB input signal generation, regardless of the number of the power mixer units. It should be noted that the overlapping technique outline in the previous subsection is utilized in Fig. 9, since two power mixer units ( $PM_0$  and  $PM_k$ ) operate at intermediate power at the same time.

There are three things to be addressed in the actual implementation of the power mixer array. First, the power mixer array is compatible with a CMOS process, since MOS transistors make good switches and are generally suitable for turning the power mixer units on and off. Second, the input of the DAC should be oversampled such that a BB envelope signal can be divided into pulses and a residue correctly. On the one hand, the sampling frequency should be  $m$  times higher than that of a conventional ER system. Also, the control frequency of the analog BB distributor and the digital LO distributor should be  $m$  times higher than the envelope bandwidth. On the other hand, the required dynamic range is relaxed by a factor of  $m$ , which implies required effective number of bits for each DAC is lower by  $\log_2(m)$  bits. This is because the number of the operating power mixer units effectively represents the  $\log_2(m)$  MSB of the BB envelope signal digital-to-analog conversion. Finally, mismatch between the power mixer units should be discussed. Since each power mixer unit represents the LSB side of the dynamic range, the mismatch requirement can be relaxed. Fortunately with a careful layout and routing, the mismatch does not affect the overall system performance.

#### D. Signal Combing at the Output Network

Another advantage of the power mixer array approach is the ease with which signal combining can be performed using a linear signal combination in the current domain, as shown in Fig. 10. To obtain the peak power, the output matching network should be designed such that the output load seen by the power mixer array ( $Z_L$ ) is small enough. Typically,  $Z_L$  is about  $5\Omega$  or smaller for a CMOS watt-level power generation circuit simply based on the reliability issues associated with maximum allowed voltage swing experienced by the output transistors. In contrast, the output impedance of the power mixer array ( $Z_O$ ) should be much larger than  $Z_L$  (typically around  $50\Omega$ ) to guarantee high efficiency. When  $Z_O$  is much higher than  $Z_L$ , the power mixer units act as ideal RF current sources, and the linear current summation is achieved regardless of the number of the activated power mixer unit.

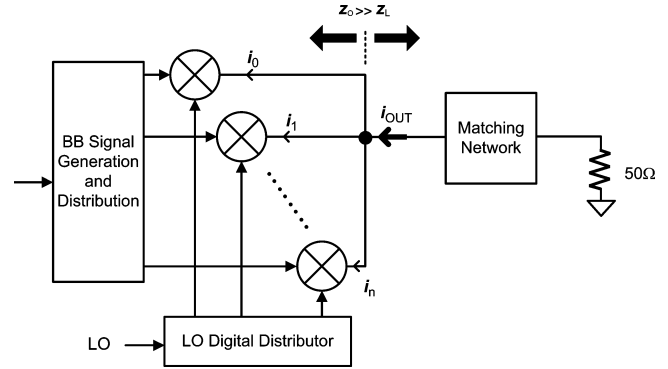


Fig. 10. Current domain signal combination at the output of the power mixer.

### III. IMPLEMENTATION AND CIRCUIT DETAILS

#### A. Architecture Overview

Complete system block diagram is shown in Fig. 11. In this implementation, the output currents of power mixer units are combined at their outputs, where the non-constant envelope RF signal is regenerated. The resultant non-constant envelope differential current is impedance transformed to drive the external single-ended  $50\Omega$  load using an on-chip tuned transformer that maintains the linearity of the current domain signal due to its linear time invariant (LTI) behavior. Sixteen power mixer units are implemented to guarantee that (1) back-off efficiency dependence is almost the same as that of a class-B amplifier, (2) required oversampling ratio is not very high, and (3) overhead in the layout to maintain the matching and minimizing the skew is negligible. The differential phase-modulated LO signal is buffered and selectively applied to the desired number of power mixer units by the digital LO distributor. The choice of how many and which power mixer units receive the digital LO is controlled by an on-chip digital controller. The differential BB envelope signal is applied to the power mixer units via an analog BB distributor, which connects each power mixer unit to any six of the differential BB input signals. As we will explain later, the BB envelope signal can be linearized by analog BB replica linearizers, while it feeds back the mixer's common mode (CM) information to the analog replica linearizers.

#### B. Power Mixer Unit

The schematic of the power mixer unit is shown in Fig. 12. It is similar to the switched transconductor mixer [21] in the sense that lower-tree common-source transistors ( $M_1$  and  $M_2$ ) are driven by the LO. The power mixer has high peak power efficiency, since the common-source transistors switch between triode and cut-off modes. The BB signals are applied to the middle-tree differential pairs ( $M_3, M_4, M_5$ , and  $M_6$ ), rendering a separate supply modulator unnecessary. The differential pair works as a cascode for the LO signals, and the power mixer utilizes another cascode with thick-gate-oxide top transistors ( $M_7$  and  $M_8$ ) [22] to increase the maximum drain voltage swings without raising reliability issues, and to boost the output impedance.

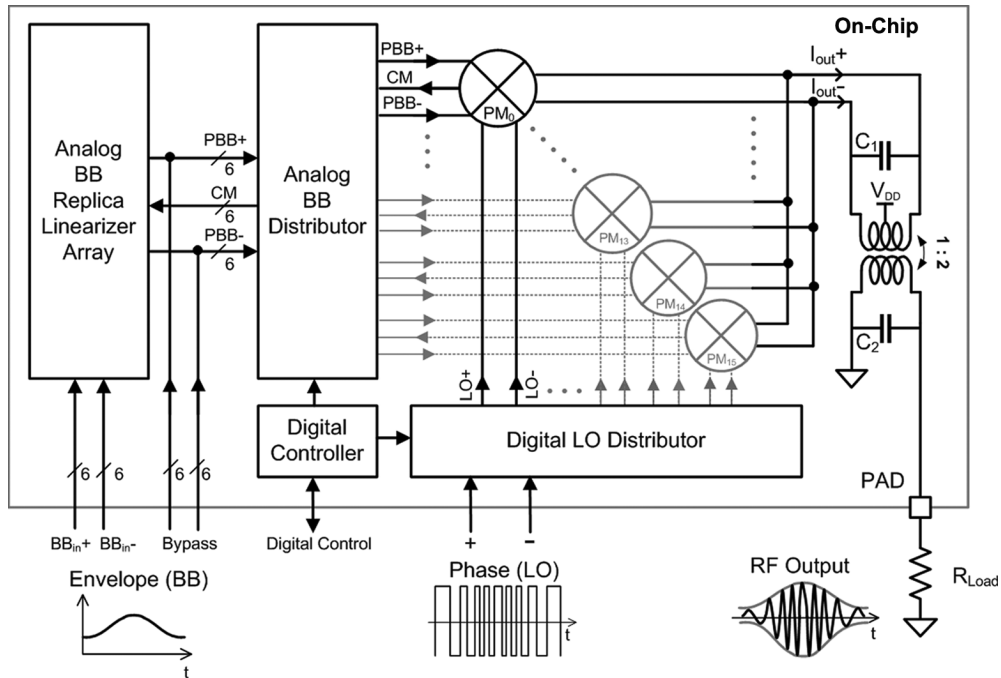


Fig. 11. Complete system block diagram of the implemented power mixer array system.

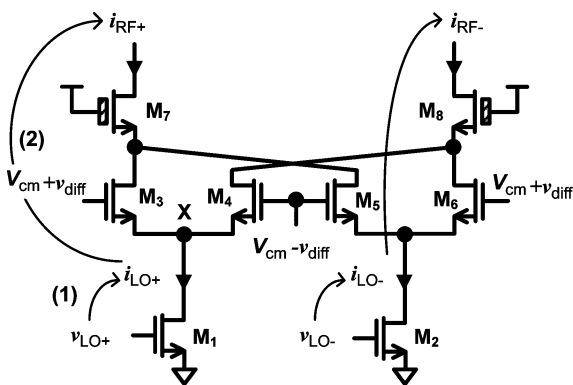


Fig. 12. The schematic of the power mixer unit.

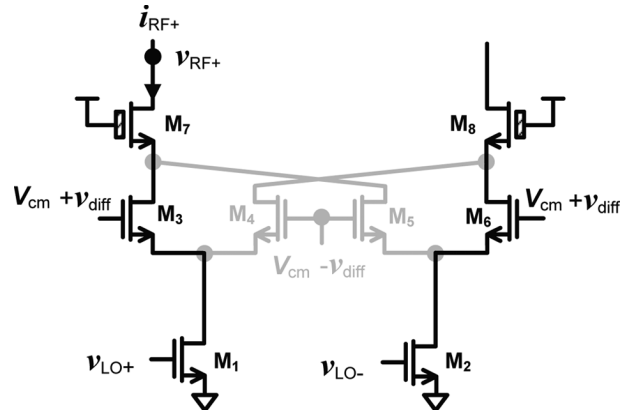


Fig. 13. The schematic of the power mixer unit in the extreme case, with very large  $v_{diff}$ .

To understand the efficient operation of the power mixer, an equivalent circuit in the limiting case, where the  $BB+$  input signals is very large and the  $BB-$  input signal is very low, is shown in Fig. 13. In this limiting case, the cross coupled paths can be neglected and the amplifier is exactly the same as the switching amplifier. The simulated drain voltage and current waveforms of Fig. 14 show switching operation of the power mixer, which enables a peak drain efficiency of 60% with an output power of +32 dBm at 1.8 GHz with sixteen power mixer units. It draws 0.88 A from a 3 V supply in the simulation.

As shown in Fig. 12, the gain of the power mixer is determined by the transconductance of the switching stage and the current gain of the differential pair. The transconductance of the switching stage is basically proportional to the DC voltage of node X in Fig. 12, as the equivalent DC model of the power mixer is shown in Fig. 15. The simulated LO current at the drains of  $M_1$  and  $M_2$  ( $i_{LO}$ ) is shown in Fig. 16. The small signal

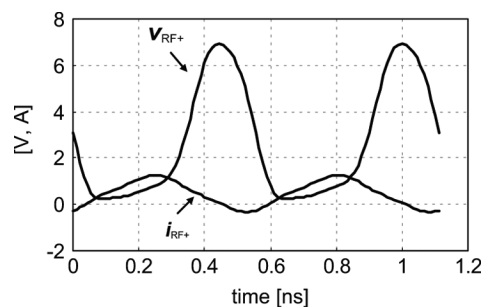


Fig. 14. The simulated drain voltage and total current of the power mixer array in the extreme case.

transconductance is determined by the common-mode input of the BB signal ( $v_{cm}$ ). However, as the differential input voltage ( $v_{diff}$ ) increases,  $i_{LO}$  starts to track the higher voltage side of

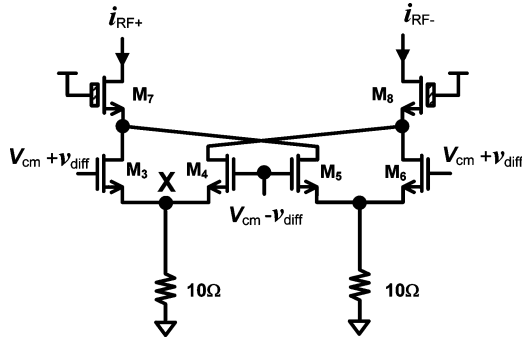
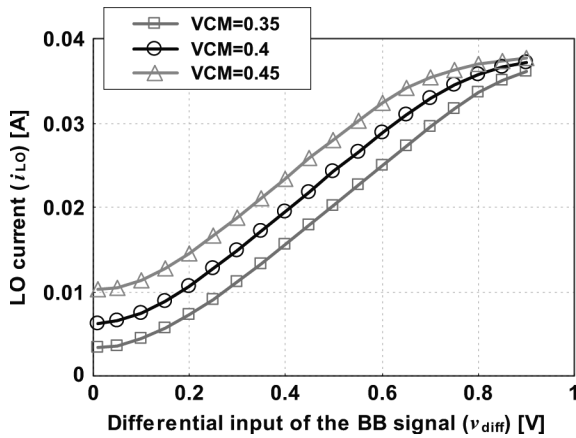
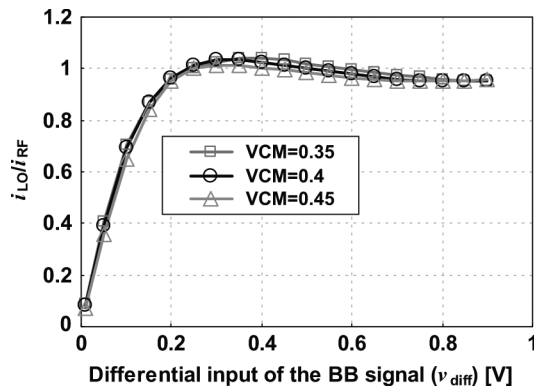


Fig. 15. Equivalent DC circuit for the power mixer unit.


 Fig. 16. Simulated  $i_{LO}$  dependence on the differential input voltage  $v_{diff}$ .

 Fig. 17. Simulated  $i_{LO}$  to  $i_{RF}$  gain.

the differential pair due to the nonlinear nature of the transconductance. At large  $v_{diff}$ ,  $i_{LO}$  saturates due to the limited drivability and the capacitance of node X. Output current,  $i_{RF}$ , is then determined by the current gain of the differential pair.  $i_{RF}$  is linearly related to  $v_{diff}$  with small  $v_{diff}$ . However  $i_{RF}$  gradually saturates as it approaches  $i_{LO}$ , as shown in Fig. 17.

We can take advantage of the positive nonlinearity of the transconductance and the negative nonlinearity of the differential pair. The nonlinearity can cancel each other by adjusting  $v_{cm}$ , and similar to a class-AB amplifier, back-off efficiency is also improved. Fig. 18 shows simulated conversion gain dependence on  $v_{cm}$  in this example where  $v_{cm}$  is 400 mV, power mixer is highly linear as the positive and the negative

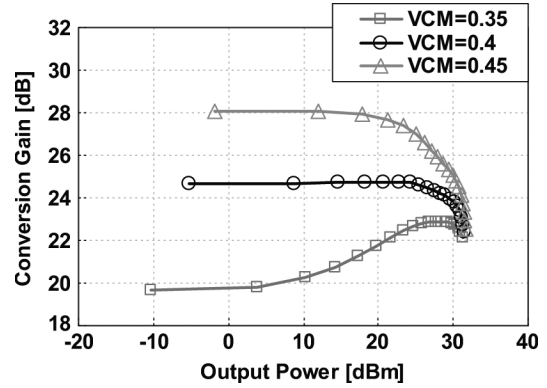


Fig. 18. Simulated conversion gain of the power mixer.

nonlinearity cancel out to the first order. DC power consumption, which is proportional to  $i_{LO}$ , is smaller when the output power is smaller.

### C. Analog Feedback Linearizer

Based on the analysis of Section III-B, we arrive at another type of linearization technique, where the transconductance of the switching stage and the current gain of the differential pair are linearized separately. The transconductance can be linearized by fixing the DC voltage of the drains of the switching stage. This is done by a replica linearizer using common-mode feedback (CMFB) circuit, as shown in Fig. 19. To linearize the current gain of the differential pair, a replica differential pair is used to model the nonlinearity. The BB replica amplifier is placed inside of a resistive feedback loop with the CMFB amplifier. The feedback linearizes the transfer function from the  $BB_{in}$  inputs to the  $BB_{out}$  outputs and in the process a differential pre-distorted signal  $PBB$  is generated at the input of the replica, which produces an output signal ( $i_{RF}$ ) linearly related to the  $BB_{in}$  signal. This  $PBB$  signal is then applied to the gates of the middle-tree power mixer units ( $M_3$ ,  $M_4$ ,  $M_5$ , and  $M_6$ ). Each linearizer draws 6 mA from a 3 V supply, with a loop bandwidth of 1 MHz.

### D. Output Matching Network

An Output matching network is designed using a transformer and a capacitor, as illustrated in Fig. 20(a). Transformer is suitable for a watt-level power generation circuit, since it is broadband and can have smaller loss than  $LC$  matching network especially when the output network is implemented on chip, where the Q of on-chip inductors can not be very large [23]. It also converts a differential input signal to a single-ended output signal. In our design, the numbers of the primary turn and secondary turn are one and two, respectively. In the ideal case, 50  $\Omega$  load is transformed to 12.5  $\Omega$  differential load, and single-ended power mixer array sees a small load of 6.25  $\Omega$ . The differential and single-ended version of complete equivalent output networks are shown in Figs. 20(b) and 20(c), respectively. Taking into account the drain capacitance ( $C_d$ ), bonding wire inductance ( $L_{bond}$ ), leakage inductance and parasitic capacitance of the transformer ( $T_1$ ), single-ended power mixer array sees a 3.6  $\Omega$  purely resistive load at 2.0 GHz. In the transformer layout, the



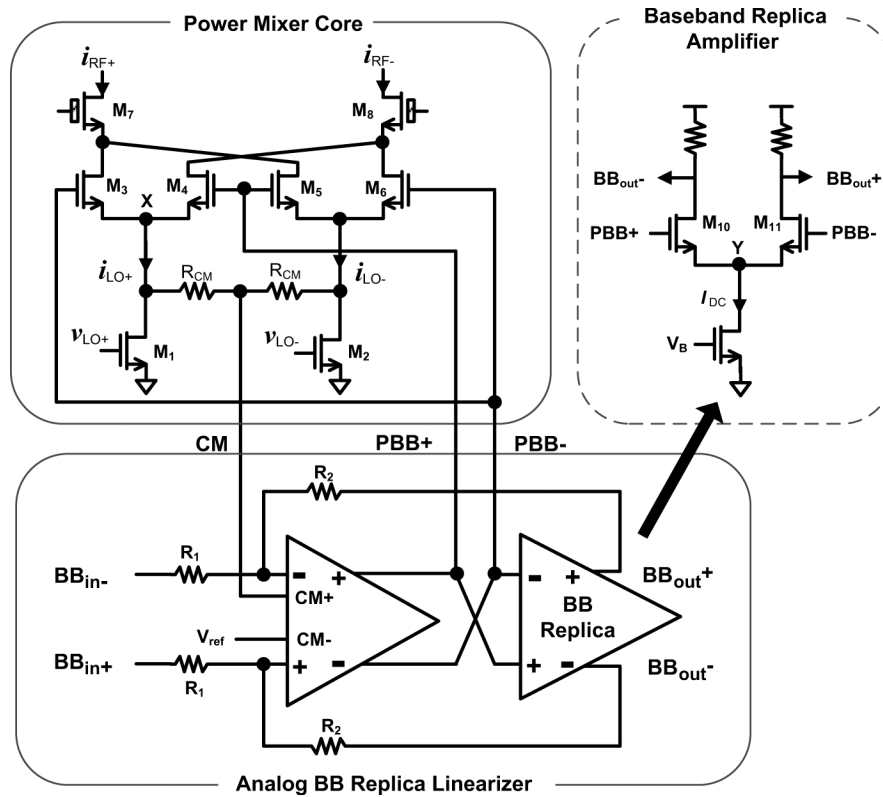


Fig. 19. Linearization by the analog BB replica linearizer.

length of the wires from each power mixer unit to the transformer is equal to match the delay between each unit. Simulated passive efficiency of this output network is about 80%.

### E. Digital LO Distributor

Fig. 21 shows the single-ended version of the digital LO distributor, which has a tree structure to match the delay for each path. The NOR gates drive the common-source transistors of the power mixer core ( $M_1$  and  $M_2$  in Fig. 12) with a 1.2 V square wave. To guarantee the differential balance, buffers are implemented by inverters and nor-gates with cross-coupled inverters. The NOR gates are used to improve the back-off efficiency of the power mixer array, as well as the digital LO distributor, since the output of a NOR-gate can be pulled down to corresponding power mixer unit, individually and dynamically. 1.2 V digital gates enable the small and power efficient digital LO distributor.

### F. Analog BB Distributor

The analog BB distributor is consisted of 48 one-to-six analog multiplexers. One of the six differential BB inputs is applied to the power mixer unit, and the CM of the power mixer unit is fed back to the feedback linearizer via the analog BB distributor. Thick gate oxide devices are used and 3 V control signals are applied to achieve a large on/off resistance ratio. Level shifters are placed to generate the 3 V control signals from a 1.2 V input signals.

### G. Controller

Six 16-bit shift registers are implemented to control the state of the analog BB distributor and the digital LO distributor. The

same number of latches as registers is also implemented so that the output of the on-chip controller is updated all at once. A 1.2 V supply is used for the controller.

## IV. OPERATION MODES AND TEST SETUP

Our power mixer array incorporates one system level and two circuit level linearization and back-off efficiency improvement techniques. In this section, we will explain three operation modes, which correspond to the three proposed linearization and back-off efficiency improvement techniques applied in different configurations. First mode of operation is *baseline analog* (BA) mode. In the BA mode, all inputs of the power mixer unit are connected to one baseband input signal, as shown in Fig. 22(a), where the entire power mixer array is used as a giant power mixer. The BB envelope signal is generated by an external ADC and an LPF. Linearization and back-off efficiency improvement are done by class-AB operation explained in Section III-B. Second mode of operation is *linearized analog* (LA) mode, in which the linearization is done by the analog BB replica linearizer, as depicted in Fig. 22(b). Similar to the BA mode, all inputs of the power mixer unit are connected to one BB signal, which is the output of the analog BB replica linearizer. In addition, common mode signal of the power mixer unit is fed to the replica linearizer. In the LA mode, linearization is done by the feedback linearizer. However, there is no back-off efficiency improvement, as it consumes almost the same current irrespective of the output amplitude. Fig. 22(c) explains another mode of operation, which is *efficient segmented* (ES) mode. The ES mode uses the segmented power generation scheme, described in the Section II-B. The digital LO distributor turns off and turns

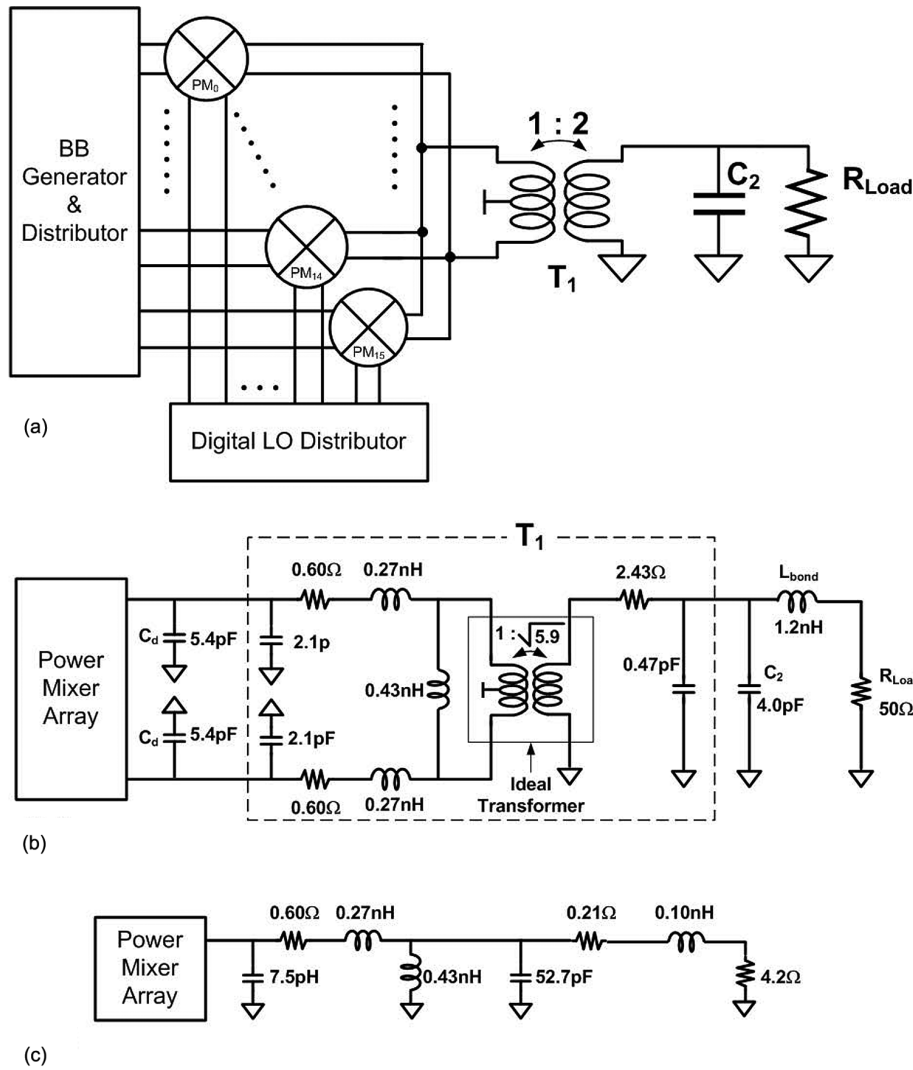


Fig. 20. (a) Output matching network implementation using a transformer and a capacitor, (b) equivalent circuit of (a), and (c) single-ended version of the equivalent circuit.

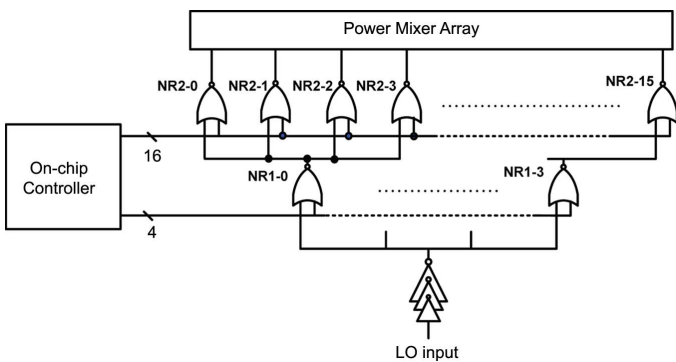


Fig. 21. The LO digital distributor.

on the power mixer units dynamically and individually to improve the back-off efficiency and linearity. The BB inputs of the power mixer units are connected to one of four BB input signals via the analog BB distributor. In this measurement setup, we use four external ADC and LPF to generate the four BB input signals. Two power mixer units, which represent the analog residue

part of the BB envelope, are always connected to the same BB signal. The remaining fourteen power mixer units are connected to one of three baseband input signals, which correspond to the turned off, turned on, or transition state. The BB distributor dynamically changes the connection between fourteen power mixer units and three BB inputs, such that the non-constant envelope signal is regenerated at the output of the power mixer array.

V. MEASUREMENT RESULTS

A prototype was fabricated in a standard 130 nm CMOS process. Fig. 23 shows the die photograph of the prototype. The entire chip occupies a small area of 1.6 mm by 1.6 mm. Fig. 24 shows the measured maximum CW output power and peak PAE of the power mixer array, with an LO input power of +3 dBm. It should be noted that PAE of the power mixer array, which subsumes the frequency up-conversion, includes DC power consumption of all the circuit blocks on-chip as

$$PAE = \frac{\text{Output RF power} - \text{LO input power}}{\text{DC power consumption of the entire chip}} \quad (11)$$

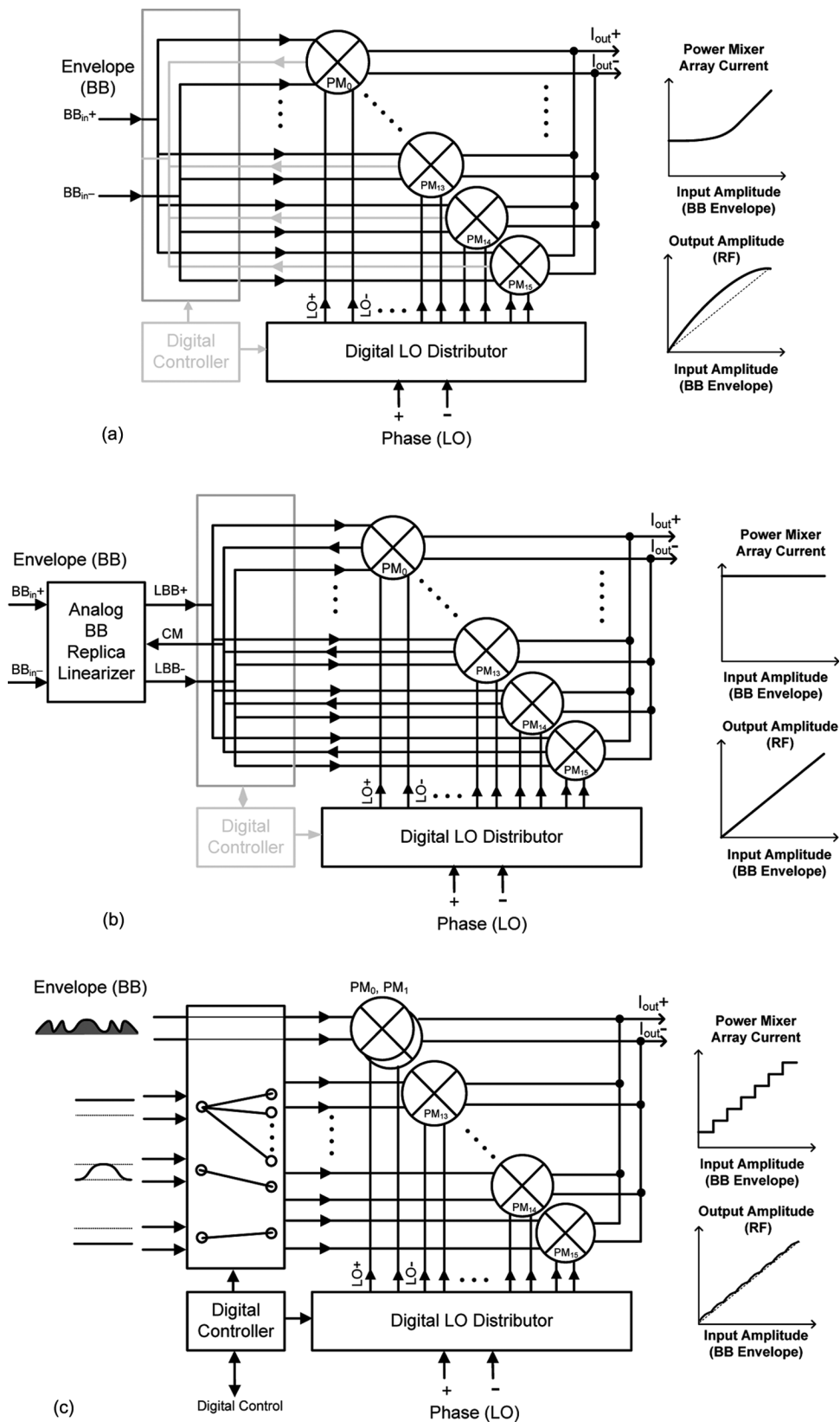


Fig. 22. Three operation mode of (a) Baseline analog (BA) mode, (b) Linearized analog (LA) mode, and (c) Efficient segmented (ES) mode.

The PAE is greater than 40% between 1.6 GHz and 2 GHz with a peak of 43% at 1.6 GHz, and the output power is greater than 1 W over an octave range from 1.2 GHz to 2.4 GHz. This wideband performance can be attributed to the high coupling

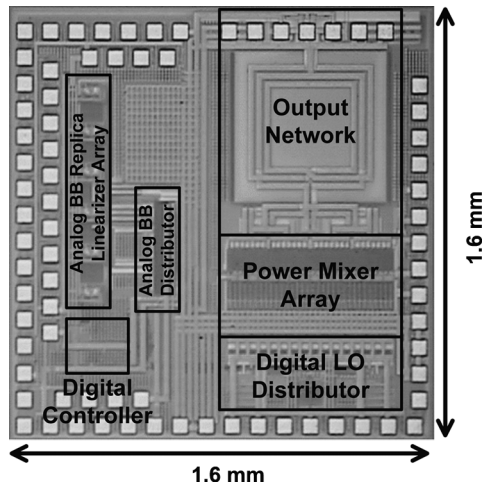


Fig. 23. Die micrograph.

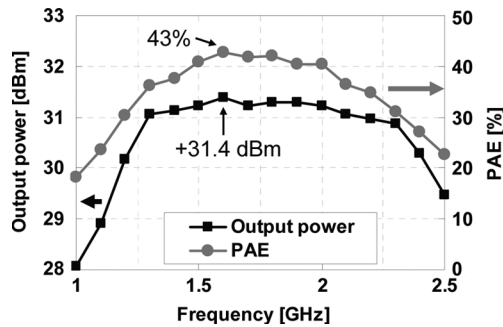


Fig. 24. Measured frequency response of output power and PAE.

coefficient ( $k \sim 0.8$ ) of the on-chip transformer. The peak PAE and drain efficiency at 1.8 GHz is 42% and 46%, respectively. Without the on-chip transformer, the peak drain efficiency is estimated around 62%. This agrees with the simulation result in the Section III-B. The power mixer array has an LO-to-RF power gain of +28.4 dB. It produces the maximum output power of +31.4 dBm with a BB input voltage of 450 mV at 1.6 GHz.

Fig. 25 shows the measured PAE and normalized conversion gain versus the output power at 1.8 GHz for the three operation modes. In the BA mode, the output  $P_{1\text{dB}}$  is +30.2 dBm where the common mode of the BB signal is optimized to obtain good linearity. In the LA mode, gain compression at its maximum output power of +31.3 dBm is only 0.4 dB and output  $P_{1\text{dB}}$  is simply the same as maximum power, i.e., +31.3 dBm. In the ES mode, there are ripples when the output power is small as expected, and the ripple gets smaller with larger output power. The ripple is almost negligible for the output power of greater than +20 dBm where gain flatness is important for a good EVM and output spectrum. Output  $P_{1\text{dB}}$  is about +28 dBm. The ES mode is most efficient for the reduced output power levels, where it clearly demonstrates an improved efficiency as shown in Fig. 25(b).

Linearity robustness to the common mode bias voltages should be discussed, since the bias condition depends on the large PVT variations in a CMOS process. Fig. 26 shows the conversion gains with different common-mode bias voltages

for the three operation modes. In the BA mode, the linearity strongly depends on the bias voltages as is expected of a conventional class-AB amplifier. In the LA mode, the high linearity can be maintained with different bias voltages due to the feedback circuits. In the ES mode, the low-power ripples in the conversion gain have a limited impact to the overall linearity of the system.

The AM-to-PM conversion is measured for the BA mode, by generating a 10 kHz amplitude modulated output signal. Instantaneous amplitude and phase are demodulated using a vector signal analyzer. Output phase dependence on the output amplitude is plotted in Fig. 27. The measured phase error is very small due to the constant RF input amplitude, and about four degrees with  $V_{CM}$  of 0.45 V.

All three modes are tested with 16 QAM modulated signal, which has non-constant envelope signal. Fig. 28 shows the EVM and PAE dependence on the average output power. In this Figure, the modulation symbol rate is 50 kSym/s and the filter used for the BB pulse shaping is root-raised cosine with excess ratio of 0.5. In the BA mode, output power of +27.1 dBm is achieved with an EVM of 4.3% and a PAE of 25%. In the LA mode, higher yet similar output power of +27.6 dBm is achieved with an EVM of 5% and a PAE of 18%. Due to its small gain compression at its full output power, EVM with back-off output power clearly shows improvement in this case. Measured EVM reaches about 1%, when the output power is reduced to +25.2 dBm. In the ES mode, output power of +26.4 dBm is achieved with EVM of 4.5% and a PAE of 26%. Similar to the BA mode, EVM reaches 1% with output power of +21.2 dBm. This indicates the ripple of the conversion gain have negligible impact to overall linearity performance. Although output  $P_{1\text{dB}}$  in the ES mode is smaller than the BA and LA modes by a few dBs, the EVM measurements show the linearity of the ES mode to be comparable. This could be explained by the thermal effects, which is included in the gain compression measurement of Fig. 25. In the BA and LA modes, the thermal effects could be compensated by the class-AB and feedback linearizer, respectively. In addition, the ES mode has the largest temperature change since it has smallest power consumption at the back-off operation. Measured spectrum and constellations for the BA, LA, and ES modes are shown in Fig. 29.

The accurate processing of the baseband pulses and especially analog residue signal described in Fig. 8 is important to avoid the aliasing and quantization noise problems. The wideband output spectrum of the ES mode with the 16 QAM signal is measured and compared with a calculated spectrum without either analog residue signal or baseband filter, as shown in Fig. 30. The clock frequency of a DAC used for the measurement is 10 MHz, and an ideal sample-and-hold DAC output is used for the calculation. While strong aliasing signals with 10 MHz separation are observed with the calculated spectrum, no aliasing signal observed with the measured spectrum. Spurs at 20 MHz offset is maybe due to the test setup, where 20 MHz control signals are applied from a separate board to the on-chip digital controller with noisy unshielded wires. The effect of the analog residue signal on the quantization noise is also measured. Fig. 31 shows the output spectrum of the ES mode

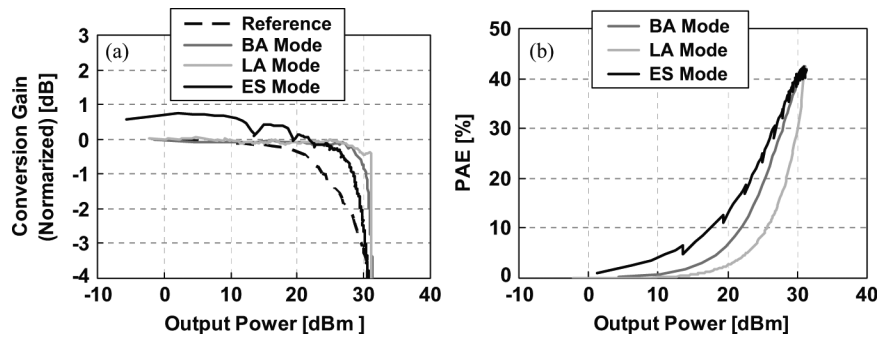


Fig. 25. Measured (a) Conversion gain and (b) PAE for BA, LA, and ES modes.

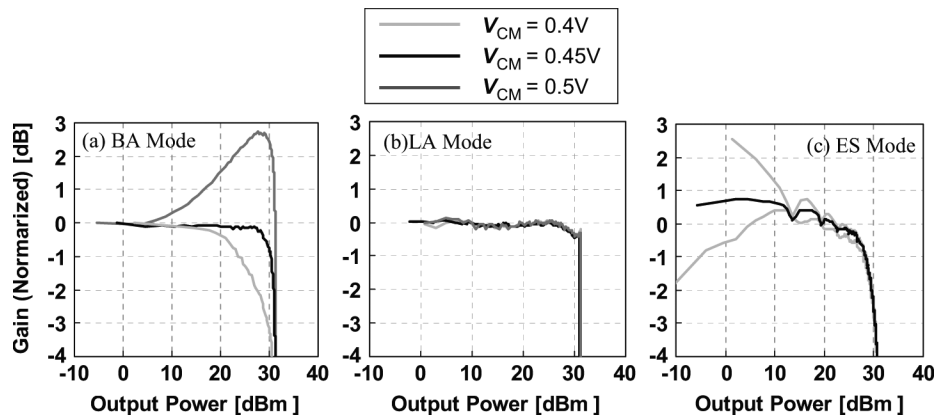


Fig. 26. Measured Conversion gain dependence of the common-mode bias.

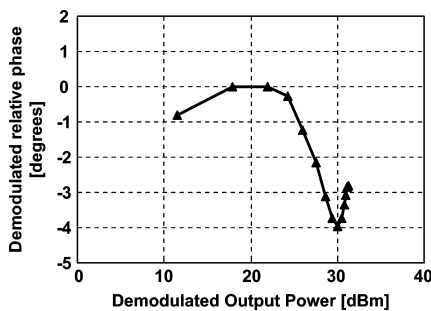


Fig. 27. Measured AM to PM conversion for the BA mode.

with  $\pi/4$ -QPSK modulation. Unwanted quantization noise is avoided by applying analog residue signal of the BB envelope to one unit. In this measurement, the clock frequency of the DAC for the analog baseband signal generation is 2 MHz.

As we discussed in Section I, one of the major challenges in the conventional ER system (i.e., supply modulation and digital PA) is its limited output power range. Even in a conventional IQ transmitter system, expensive and power consuming RF gain control circuit is required to realize large output power range. The power mixer array can have very small output power without any RF gain control, since LO leakage can be very small due to its double-balanced topology. Measured LO leakage is shown in Fig. 32. To reduce the LO leakage, only one power mixer unit is activated and  $v_{cm}$  is set to 200 mV, which substantially reduces the transconductance of the switching stage. The LO leakage is measured at  $-70$  dBm without adjusting the

TABLE I  
BASIC PERFORMANCE SUMMARY

#### Basic Performance

Frequency	1.8 GHz	
Maximum Output Power	+31.3 dBm	
Peak PAE	42 %	
LO Input Power	3 dBm	
Die Area	2.56 mm <sup>2</sup>	
Max. LO to RF Power Gain	28.3 dB	
BB to RF Voltage	Max.	20.2 dB
Conversion Gain	Min.	-18.6 dB
Output Power Range	103 dB	
OP1dB	BA-mode	+30.2 dBm
	LA-mode	+31.3 dBm
	ES-mode	+28.5 dBm

#### Power Consumption

	Supply Voltage	Power Consumption
Power Mixer Array	3 V	2.94 W
Digital LO Distributor	1.2 V	0.27 W
Analog BB Replica Linearizer	3 V	18 mW
Analog BB Distributor	3 V	< 0.1 mW
Digital Controller	1.2 V	< 0.1 mW

#### Basic modulation performance

Modulation	PAPR	Mode	Pout	PAE	EVM
16QAM	5.9 dB	BA	+27.1 dBm	25%	4.3%
		LA	+27.6 dBm	18%	5.0%
		ES	+26.5 dBm	26%	4.5%
$\pi/4$ -QPSK	3.7 dB	LA	+29.0 dBm	25%	3.4%

DC offset of the differential pair. It can further be reduced by input offset cancellation techniques as evident from its reduction to

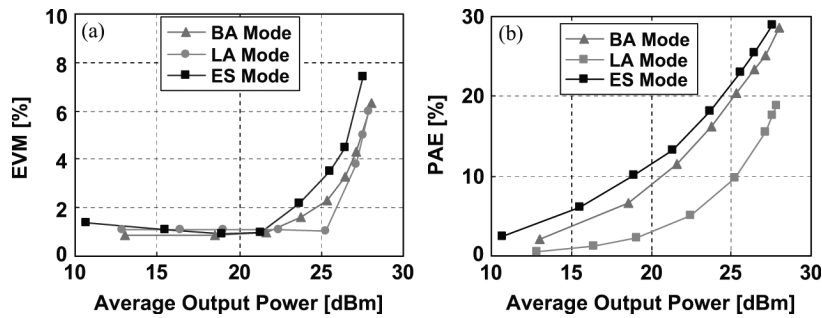


Fig. 28. Measured (a) EVM and (b) PAE with 16 QAM signal.

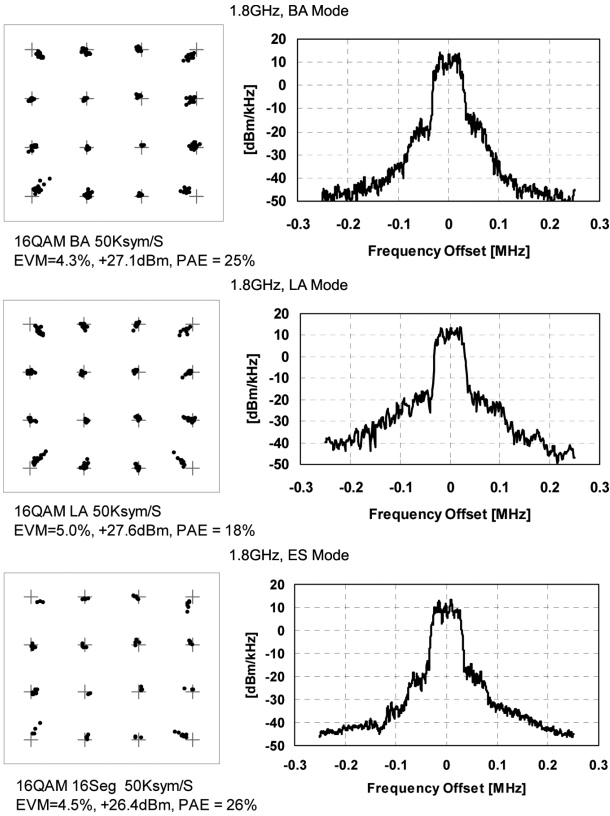


Fig. 29. Measured output spectrum and constellation for BA, LA, and ES modes.

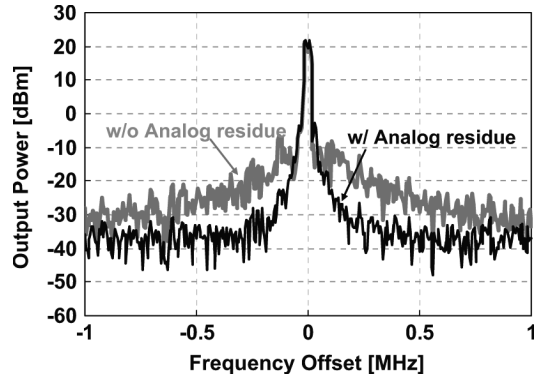


Fig. 31. Measured quantization noise suppression due to the analog residue signal.

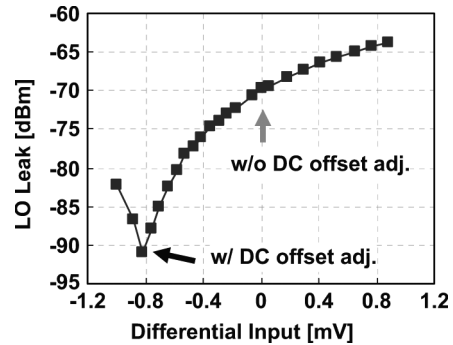


Fig. 32. Measured LO leakage dependence of the input DC offset voltage.

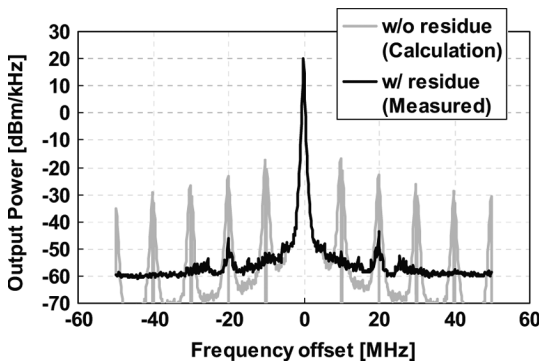


Fig. 30. The wideband spectrum of the ES mode with 16 QAM modulation.

lower than  $-91$  dBm, when  $-0.82$  mV differential DC input is applied to cancel the offset of the differential pair. The EVM with 16 QAM signal is measured with large output power range, as shown in Fig. 33. The EVM is less than 5% for output power levels greater than  $-57.9$  dBm without the adjustment. With

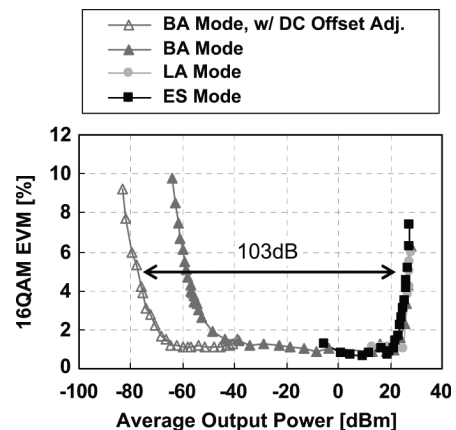


Fig. 33. Measured EVM for small output power, with and without DC offset canceled.

the adjustment, EVM is less than 5% with output power levels greater than  $-76.2$  dBm, and more than 100 dB output power dynamic range is achieved without any RF gain control circuit.

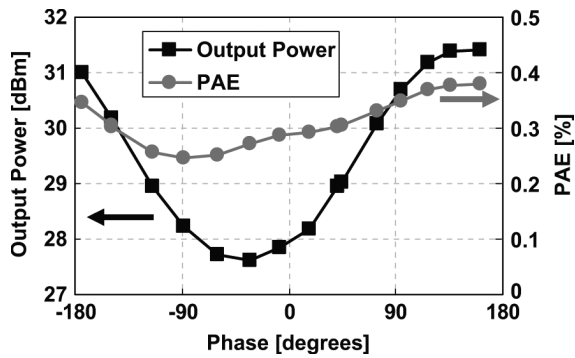


Fig. 34. Measured output power and PAE at a VSWR mismatch of 1:2.6.

The power mixer array with the maximum output power at 1.8 GHz is tested for a VSWR mismatch. The output power and PAE for a VSWR mismatch of about 1:2.6 is shown in Fig. 34. The output power and PAE are degraded to +27.6 dBm and 26% at worst, respectively. In terms of reliability, the power mixer array survives VSWR mismatch test of up to 1:5.5, which is the most severe condition for our test setup, with no output power degradation.

Table I summarizes basic performances. From the summary, we can discuss the use of the three operation modes. In the LA mode, the current consumption is almost constant regardless of its output power. Therefore, the use of the LA mode might be limited to when the power mixer array generates its highest output power and non-constant envelope modulations, where the EVM is better than BA and ES modes. In the 16 QAM case for instance, LA mode should be used to generate output powers greater than +26.0 dBm. When the output power is close to its saturation output power, PAE can be comparable to those of BA and ES modes. For example, a PAE of 25% is achieved with an output power of +29.0 dBm and an EVM of 3.4%, when the modulation signal is  $\pi/4$ -OQPSK. The ES mode has the best PAE for the same output power, and thus this mode should be used when it offers an acceptable EVM. In the 16 QAM case for example, an output power of less than +26.0 dBm can be produced by using the ES mode. As we discussed in Section II-C, in the ES mode, the operating frequency of the analog BB and digital LO distributors should be fast enough to represent the envelope frequency. In this implementation, the operating frequency of the analog BB distributor is limited to 1 MHz due to the test setups (serial interface of the on-chip controller). The maximum modulation bandwidth is 100 kSym/s, without sacrificing power efficiency.

The BA mode has the highest modulation bandwidth, and it is tested with some wideband standard signals such as WCDMA and mobile WiMAX. Fig. 35(a) shows the output spectrum and constellation for WCDMA output signal with a PAPR of 3.5 dB at 1.75 GHz. Measured output power is +28.3 dBm with a PAE of 30% and an EVM of 2.9%. Fig. 35(b) shows the output spectrum and constellation for the multi-code modulation, where the PAPR is as high as 5.2 dB. An output power of +25.5 dBm is measured with a PAE of 21% and an EVM of 3.1%. WCDMA spectra are also measured for different frequencies of 1.83 GHz and 1.95 GHz. The EVM, spectrum mask and ACLR of all measurements satisfy the 3GPP specification, as the result is

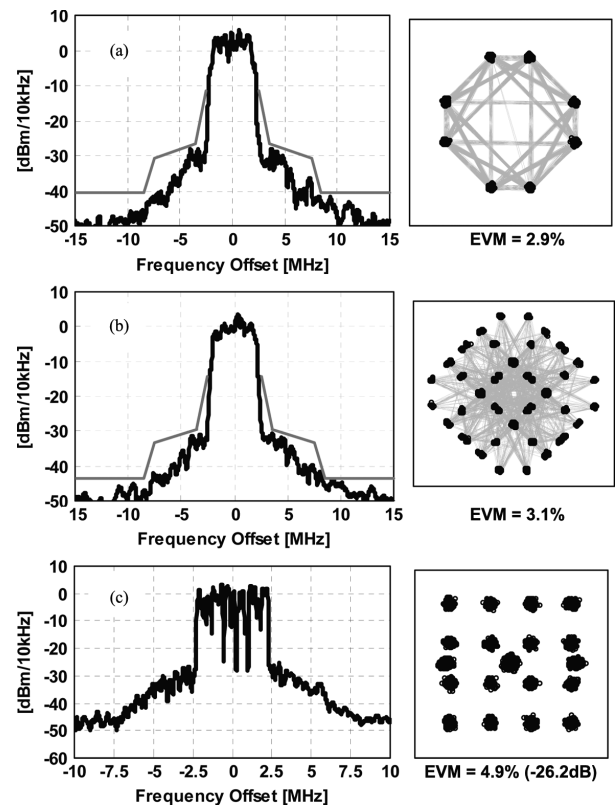


Fig. 35. Measured output spectrum and constellation for (a) WCDMA signal with a PAPR of 3.5 dB, (b) WCDMA signal with a PAPR of 5.2 dB, and (c) WiMAX signal.

TABLE II  
MODULATION PERFORMANCE SUMMARY FOR (A) WCDMA AND (B) WiMAX  
(99.9% PAPR = 8.5 dB) SIGNALS

		PAPR = 3.5dB			PAPR = 5.2dB		
		Band I	Band II	Band III	Band I	Band II	Band III
Frequency [GHz]		1.95	1.83	1.75	1.95	1.83	1.75
Power [dBm]		28.4	28.3	28.3	25.1	25.3	25.5
PAE		28%	28%	30%	19%	20%	21%
EVM	PEAK	10.6%	10.1%	7.7%	12.7%	11.1%	11.1%
	RMS	3.7%	3.5%	2.9%	3.4%	3.0%	3.1%
ACLR [dB]	Lower 10M	-48.8	-47.2	-50.2	-43.6	-44.1	-50.5
	Lower 5M	-36.6	-36.3	-36.1	-35.4	-33.2	-38.4
	Upper 5M	-36.1	-35.5	-35.4	-34.0	-33.4	-37.2
	Upper 10M	-46.1	-45.5	-47.3	-45.9	-47.7	-48.4

		1.75	1.75
Frequency [GHz]		1.75	1.75
Signal Bandwidth		5	10
Power [dBm]		25.0	25.0
PAE		20%	20%
EVM		4.9%	4.8%

summarized in Table II. Fig. 35(c) shows the output spectrum and constellation for mobile WiMAX at 1.75 GHz with a signal bandwidth of 5 MHz. An output power of +25 dBm is obtained with a PAE of 20% and an EVM of 4.9%. Similar performance is obtained with the BB signal bandwidth of 10 MHz, as the result is summarized in Table II.

TABLE III  
PERFORMANCE COMPARISON WITH RECENTLY REPORTED MONOLITHIC POWER AMPLIFIERS FOR MOBILE APPLICATION

Ref.	Technology and PA system	freq	$V_{DD}$	Die area	Ext. comp.	$OP_{1dB}$	WiMAX/WLAN			WCDMA		
							$P_{OUT}$	PAE	EVM	$P_{OUT}$	PAE	AC LR
	Unit	GHz	V	$mm^2$		dBm	dBm	%	dBc	dBm	%	dBc
This work	CMOS, ER (power mixer)	1.8	3	2.6	No	30	25	20	-26	28.3	30	-36
[1]	CMOS, Class-AB	2.4	3.3	1.7	No	24.5	19	16	-27	-		
[2]	CMOS, Class-AB	2.4	3.3	0.7	Yes	25.1	18.8	14	-26	-		
[3]	CMOS, Class-AB	2.3	3.3	4	No	27.7	22.3	12	-25	-		
[5]	CMOS, Doherty	3.7	1.6	2.7	Yes	25.4	21	13	-25	-		
[6]	CMOS, Outphasing	0.9	1.2	-	Yes	-	-			13	30	-
[10]	CMOS, ER (digital PA)	1.6	1.7	1.8	Yes	-	13.6	7	-27	-		
[8]	LDMOS, ER (supply mod.)	1.9	3.6	1.1	Yes	-	-			27	46	-39
[19]	SiGe-HBT, ET	2.4	3.3	4	Yes	-	20	28	-26	-		
[24]	GaAs-HBT, Doherty	5.2	3.3	1.6	No	-	22.5	21	-26	-		
[25]	GaAs-HBT, Class-AB	-	3.4	0.5	Yes	-	-			28	54	-33
[26]	GaAs-HBT, Class-AB	2.5	6	2.5	Yes	-	30	20	-26	-		

## VI. CONCLUSION

A new system and circuits for a watt-level power generation of a non-constant envelope signal in a CMOS process was presented. The power mixer array achieves +31.3 dBm output power with PAE of 42% at 1.8 GHz. In the LA mode, which uses proposed feedback circuit, the gain compression at its full output power is only 0.4 dB. In the ES mode, which exploits the novel segmented power generation, power mixer array can transmit a +26.5 dBm 16 QAM signal with a PAE of 26% and an EVM of 4.5%. In the BA mode, which utilizes the class-AB operation, it is capable of transmitting +28.3 dBm WCDMA spectrum and +25.0 dBm WiMax spectrum with PAE of 30% and 20%, respectively. It can also produce down to -70 dBm output with EVM of less than 5%, without any RF gain control circuit. The chip also includes wideband 50  $\Omega$  output matching and occupies only 2.6  $mm^2$ , which is attributed mainly on the nonlinear amplification of the LO signal. This is the first reported fully integrated CMOS power generation circuit to achieve over 1 W output  $P_{1dB}$ , in gigahertz range and the performance is comparable to a recently reported fully integrated GaAs PA [24], as can be seen in Table III, summarizing previous work of monolithic PA for mobile application [25], [26].

## ACKNOWLEDGMENT

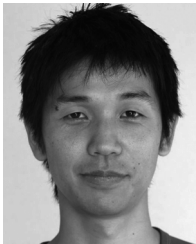
The authors would like to thank the members of the CHIC group at Caltech, particularly Y. Wang and H. Wang for many helpful discussions, Hamdi Mani of Caltech, and Toshiba Corporation.

## REFERENCES

- [1] J. Kang, A. Hajimiri, and B. Kim, "A single-chip linear CMOS power amplifier for 2.4 GHz WLAN," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2006, pp. 208–209.
- [2] R. D. Singh and K. Yu, "A linear mode CMOS power amplifier with self-linearizing bias," in *Proc. A-SSCC*, 2006, pp. 251–254.
- [3] D. Chowdhury, C. D. Hull, O. B. Degani, P. Goyal, Y. Wang, and A. M. Niknejad, "A single-chip highly linear 2.4 GHz 30 dBm power amplifier in 90 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2009, pp. 378–379.
- [4] N. Wongkomet, L. Tee, and P. R. Gray, "A +31.5dBm CMOS RF Doherty power amplifier for wireless communications," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2852–2559, Dec. 2006.
- [5] M. Elmala, J. Parmesh, and K. Soumyanath, "A 90-nm CMOS Doherty power amplifier with minimum AM-PM distortion," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1323–1332, Jun. 2006.
- [6] S. Moloudi, K. Takinami, M. Youssef, M. Mikhemar, and A. Abidi, "An outphasing power amplifier for a software-defined radio transmitter," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2008, pp. 568–569.
- [7] P. Reynaert and M. S. J. Steyaert, "A 1.75-GHz polar modulated CMOS RF power amplifier for GSM-EDGE," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2598–2608, Dec. 2005.
- [8] V. Pinon, F. Hasbani, A. Giry, D. Pache, and C. Garnier, "A single-chip WCDMA envelope reconstruction LDMOS PA with 130 MHz switched-mode power supply," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2008, pp. 564–565.
- [9] P. Cruise, C.-M. Hung, R. Staszewski, O. Eliezer, S. Rezeq, K. Maggio, and D. Leipold, "A digital-to-RF amplitude converter for GSM/GPRS/EDGE in 90-nm digital CMOS," in *Proc. IEEE RFIC Symp.*, Oct. 2005, pp. 21–24.
- [10] A. Kavousian, D. Su, and B. Wooley, "A digitally modulated polar CMOS power amplifier with 20 MHz signal BW," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2251–2258, Oct. 2008.
- [11] C. D. Presti, F. Carrara, and G. P. A. Scuderi, "A high-resolution 24-dBm digitally-controlled CMOS PA for multi-standard RF polar transmitters," in *Proc. 34th ESSCIRC Conf.*, 2008, pp. 482–485.
- [12] F. H. Raab, "Efficiency of outphasing RF power-amplifier systems," *IEEE Trans. Commun.*, vol. COM-33, no. 10, pp. 1094–1099, 1985.
- [13] A. Pham and C. G. Sodini, "A 5.8 GHz, 47% efficiency, linear outphase power amplifier with fully integrated power combiner," in *Proc. IEEE RFIC Symp.*, 2006, pp. 160–163.
- [14] L. Kahn, "Single-sided transmission by envelope elimination and restoration," in *Proc. IRE*, Jul. 1952, pp. 803–806.
- [15] W. Chu, B. Bakkaloglu, and S. Kiaei, "A 10 MHz bandwidth, 2 mV ripple PA regulator for CDMA transmitters," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2809–2819, Dec. 2008.
- [16] S. Hietakangas, T. Rautio, and T. Rahkonen, "Feedthrough cancellation in a class E amplified polar transmitter," in *Proc. European Conf. Circuit Theory Design*, 2007, pp. 591–594.
- [17] J. D. Kitchen, I. Deligoz, S. Kiaei, and B. Bakkaloglu, "Linear RF polar modulated SiGe class E and F power amplifiers," in *Proc. IEEE RFIC Symp.*, 2006, pp. 4–7.



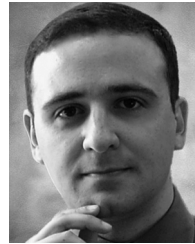
- [18] F. Wang, A. Yang, D. Kimball, L. Larson, and P. Asbeck, "Design of wide-bandwidth envelope-tracking power amplifiers for OFDM applications," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 4, pp. 1244–1255, Apr. 2005.
- [19] F. Wang, D. Kimball, D. Lie, P. Asbeck, and L. Larson, "A monolithic high-efficiency 2.4-GHz 20-dBm SiGe BiCMOS envelope-tracking OFDM power amplifier," *IEEE J. Solid-State Circuits*, vol. 42, no. 6, pp. 1271–1281, Jun. 2007.
- [20] S. Kang, B. Choi, and B. Kim, "Linearity analysis of CMOS for RF application," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 972–977, Mar. 2003.
- [21] E. Klumperink, S. Louwsma, G. Wienk, and B. Nauta, "A CMOS switched transistor mixer," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1231–1240, Aug. 2004.
- [22] T. Kuo and B. Lusignan, "A 1.5 W class-F RF power amplifier in 0.2 $\mu$ m CMOS technology," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2001, pp. 154–155.
- [23] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Fully-integrated CMOS power amplifier design using the distributed active transformer architecture," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 371–83, Mar. 2002.
- [24] D. Yu, Y. Kim, K. Han, J. Shin, and B. Kim, "Fully integrated Doherty power amplifiers for 5 GHz wireless-LANs," in *Proc. IEEE RFIC Symp.*, 2006, pp. 4–7.
- [25] Y. S. Noh and C. S. Park, "An intelligent power amplifier MMIC using a new adaptive bias control circuit for W-CDMA applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 967–970, Jun. 2004.
- [26] M. Miyashita, T. Okuda, H. Kurusu, S. Shimamura, S. Konishi, J. Udamoto, R. Matsushita, Y. Sasaki, S. Suzuki, T. Miura, M. Komaru, and K. Yamamoto, "Fully integrated GaAs HBT MMIC power amplifier modules for 2.5/3.5-GHz-Band WiMAX applications," in *Proc. IEEE Compound Semiconductor Integrated Circuits Symp. (CSICS)*, 2007, pp. 1–4.



**Shouhei Kousai** (M'08) received the B.S. and M.S. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1996 and 1998, respectively.

In 1998, he joined Toshiba Corporation, Kanagawa, Japan. Since then he has been engaged in the design of analog and RF circuits for wireless communications. From 2007 to 2009, he was a visiting scholar at the California Institute of Technology. He is also a part-time Ph.D. student at Tokyo Institute of Technology.

Mr. Kousai is a member of the technical program committee of A-SSCC.



**Ali Hajimiri** (M'99) received the B.S. degree in electronics engineering from Sharif University of Technology, Tehran, Iran, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1996 and 1998, respectively.

He was a Design Engineer with Philips Semiconductors, where he worked on a BiCMOS chipset for GSM and cellular units from 1993 to 1994. In 1995, he was with Sun Microsystems, where he worked on the UltraSPARC microprocessor's cache RAM design methodology. During the summer of 1997, he was with Lucent Technologies-Bell Labs, Murray Hill, NJ, where he investigated low-phase-noise integrated oscillators. In 1998, he joined the Faculty of the California Institute of Technology, Pasadena, where he is a Professor of electrical engineering and the director of Microelectronics Laboratory. He co-founded Axiom Microdevices Inc. in 2002, which has shipped more than fifty million fully-integrated CMOS PAs, and was acquired by Skyworks Inc. in 2009. His research interests are high-speed and RF integrated circuits for applications in sensors, biomedical devices, and communication systems. He is the author of *The Design of Low Noise Oscillators* (Springer, 1999) and has authored and coauthored more than 100 refereed journal and conference technical articles. He holds more than 24 U.S. and European patents.

Dr. Hajimiri has served on the Technical Program Committee of the International Solid-State Circuits Conference (ISSCC), as an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC), as an Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS (TCAS) II, a member of the Technical Program Committees of the International Conference on Computer Aided Design (ICCAD), Guest Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, and Guest Editorial Board of the *Transactions of Institute of Electronics, Information and Communication Engineers of Japan* (IEICE). Dr. Hajimiri was selected as one of the top 100 innovators (TR100) list in 2004 and is a Fellow of the Okawa Foundation. He has served as a Distinguished Lecturer of the IEEE Solid-State and Microwave Societies. He is the recipient of Caltech's Graduate Students Council Teaching and Mentoring award as well as the Associated Students of Caltech Undergraduate Excellence in Teaching Award. He was the Gold medal winner of the National Physics Competition and the Bronze Medal winner of the 21st International Physics Olympiad, Groningen, The Netherlands. He was a co-recipient of the IEEE JSSC Best Paper Award of 2004, the International Solid-State Circuits Conference (ISSCC) Jack Kilby Outstanding Paper Award, a two-time co-recipient of CICC Best Paper Award, and a three-time winner of the IBM Faculty Partnership Award as well as National Science Foundation CAREER Award.