Self-Reconfigurable Analog Arrays: Off-The Shelf Adaptive Electronics for Space Applications

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Abstract

Development of analog electronic solutions for space avionics is expensive and lengthy. Lack of flexible analog devices, counterparts to digital Field Programmable Gate Arrays (FPGA), prevents analog designers from benefits of rapid prototyping. This forces them to expensive and lengthy custom design, fabrication, and qualification of application specific integrated circuits (ASIC). The limitations come from two directions: commercial Field Programmable Analog Arrays (FPAA) have limited variability in the components offered on-chip; and they are only qualified for best case scenarios for military grade (- 55C to +125C). In order to avoid huge overheads, there is a growing trend towards avoiding thermal and radiation protection by developing extreme environment electronics, which maintain correct operation while exposed to temperature extremes (- 180°C to +125°C). This paper describes a recent FPAA design, the Self-Reconfigurable Analog Array (SRAA) developed at JPL. It overcomes both limitations, offering a variety of analog cells inside the array together with the possibility of self-correction at extreme temperatures.

1. Introduction

Contrasting to fixed circuit solutions such as application specific integrated circuits (ASICs), field programmable gate and analog arrays (FPGAs and FPAAs) are advantageous for space applications due to their flexibility of being programmed after launch. While FPGAs are already being utilized in space applications, their analog counterparts have yet to be tested in space.

Planetary exploration and long-term satellite missions require radiation and extreme-temperature hardened electronics to survive the harsh environments beyond Earth's atmosphere. Failure to take appropriate precautions in this area could lead to disastrous consequences, potentially jeopardizing the vehicle, the mission and, in fact, future missions as well. Thus for long-term missions it is essential that all electronics can somehow deal with faults.

There are two main approaches possible to achieve the needed survivability of electronics in extreme environments. The first is to use materials/devices that are less affected by environmental conditions such as temperature. National Aeronautics and Space Administration (NASA) has invested in SiGe solutions, which have shown a good response and stability all the way to very low temperatures (–230° C and below) [1]. The second approach is to allow variations of devices with temperature, but to compensate for them at the circuit and sub-system level. This is the approach of the Self-Reconfigurable Electronics for Extreme Environments project. Reconfigurability at a fine level includes programming current and voltage sources injecting compensation signals to the circuits (tunability is a more appropriate term at this level). On the other hand reconfigurability at a coarser (block) level allows encapsulation of high-performance circuits in cells and a good number of resources that can be interconnected as needed to form a number of circuits and subsystems.

The limitation of current FPAA in terms of reduced type or small number of cells is overcome by employing a larger number of cells/building blocks (BB) with a larger diversity. Thus, compared to commercial solutions this has the advantages in terms of (1) larger variability of the cells, (2) total number of cells, and (3) extended temperature operational range (from –180C to 125C). While in our prior work, BBs were of very fine granularity (as in field programmable transistor arrays, FPTA, and most refined to transistor level in FPTA-0 [2]) the SRAA uses buildings blocks of common encapsulated granularity, with advantages in frequency response because of fewer parasitic losses. Compared to our FPTA architecture [3], [4] that would only map circuits operating in the ~ 100 kHz range, the SRAA is expected to operate beyond ~5MHz.

Second NASA/ESA Conference on Adaptive Hardware and Systems(AHS 2007)
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We have implemented a number of test chips as operational transconductance amplifiers (OTA) and have demonstrated that OTA can be compensated algorithmically. These tests were conducted using appropriate equipment for temperature control (-196°C to 130°C range) [5]. Higuchi [6] has demonstrated working of OTA cells for design of filters by exploiting programmable current biases to tune circuits using evolutionary algorithms to compensate for fabrication variations. In our case of circuits implemented with OTA, the tuning successfully compensated not for parameter variation due to mismatch but for temperature-induced deviations within -180C and 120C range.

The most recent Self-Reconfigurable Analog Array (SRAA) designed at JPL specifically provides the capability of temperature compensation combined with the availability of a variety of elementary cells. This offers sufficient flexibility to map a number of specific circuits for which mission-oriented ASICs were designed in the past. The SRAA cells were designed with built-in tunable knobs offering degrees of tuning and programmability for compensation for effects that come from temperature variations. A special characteristic of the architecture is that the on-line normal operation can continue uninterrupted while optimal compensation is determined on a set of reference cells. The result of compensation is then transferred to the main array. This is the first field-programmable architecture that allows on-line real-time adaptation while its main function is performed, providing a means of adaptation with hardware in the loop that does not jeopardize system safety. Currently, the algorithmic control for adaptation and reconfiguration is on a separate digital ASIC, which in future could be integrated into selected SRAA versions.

The paper is organized as follows. Section 2 presents an analysis of NASA-designed ASICs implementing functions for sensing and actuation. The analysis results in a selection of a common set of BBs that has been incorporated in multiple designs. Section 3 presents the SRAA architecture incorporating the selected set of BBs in an array of operational cells. For each group of cells of one type there is also a reference/test cell of the same type, on which adjustments and calibration can be performed even during run-time. It also describes the digital controls that permit multiple functions and hierarchical adaptation. Section 4 illustrates examples of mapping a circuit using SRAA cells and shows various simulation results.

2. Analog circuits for sensing and actuation in space avionics

An analysis of NASA-designed ASICs implementing functions for sensing and actuation reveals that a number of BBs is common to multiple designs.

The Table 1 below is a part of a larger table that reviews circuit BBs utilized in a variety of NASA designed sensors and power control chips.

Based on the analysis of a number of ASICs, the following types of BBs (and their numbers in circuits) were selected for the first generation SRAA:

1. Operational Amplifiers (OpAmps)
2. Low-Offset OpAmps
3. Current Sources
4. High Voltage OpAmps
5. Comparators
6. High Speed Comparators

Table 1. A reduced table summarizing the function of the ASIC (horizontal rows) and the main building blocks used (columns).

ASIC/Application	OpAmp	Low-Offset OpAmp	Current Source	HV OpAmp	High-speed Comparators	Passive Components	Digital Interface	Bandgap Reference
Pulse Width Modulator (PWM)			1		2	x	x	2
Power Switch Control		1		1		x		
Shaft Encoder	4	4			4	x		
Instrumentation Amplifier	3	3						1

Different implementations of the same building block were selected as needed for the functions. For instance, two kinds of OpAmps were implemented, conventional OpAmp and Low Offset (or Ping-Pong) OpAmp. The later presents an input offset voltage below 100uV. The comparator has a conventional and also a high-speed (more than 5MHz) implementation.

Based on the requirements of each application, a building block is replicated 4 times, resulting in a 4x6 analog array. In addition, an extra copy of each cell will serve as reference for adjustment, as explained in the next sections.

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3. Self-Reconfigurable Analog Array

This section presents the SRAA architecture incorporating the selected set of BBs in an array of operational cells. As mentioned earlier, for each group of cells of one type there is a reference/test cell of the same type for adjustments and calibration during run-time.

3.1 SRAA architecture

Main components of the SRAA architecture are the analog cell arrays (divided into reference and functional array), the switch box and the test fixture (Figure 1). The SRAA is externally controlled by an FPGA and a digital ASIC. These are described below.

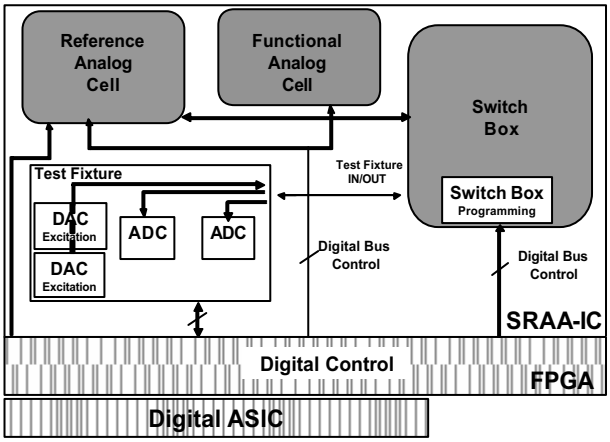

Figure 1. SRAA block diagram. Digital controls now implemented in FPGA/ASIC may be included on-chip in next version of the SRAA

3.2 Analog Array

The analog array is divided into the functional and the reference analog arrays. The reference analog cells are individually excited/probed through the test fixture to check for degradation. The functional array is configured to implement the system functions described in Section 2.

Figures 2 and 3 show block diagrams of the reference and functional cells. Both types of cells include Digital-to-Analog Converters (DACs) used to provide bias voltages or currents to tune the analog cell response (see Section 3.4). In current implementation, these *reconfiguration DACs* are programmed by external controls originating in an FPGA. While the I/O of the reference analog cells are provided/read by the test fixture, they are routed to other functional cells or to I/O pads in the case of the functional analog cell.

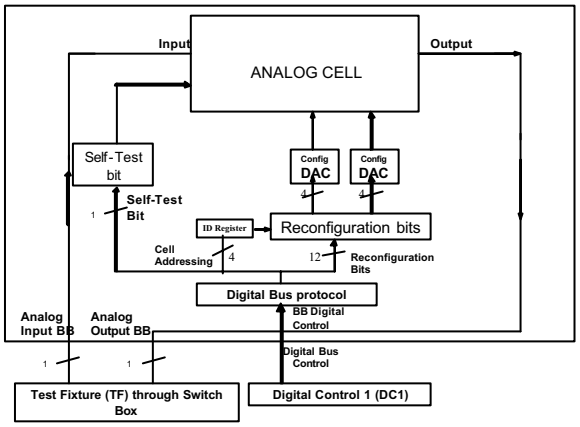

Figure 2: Reference Analog Cell

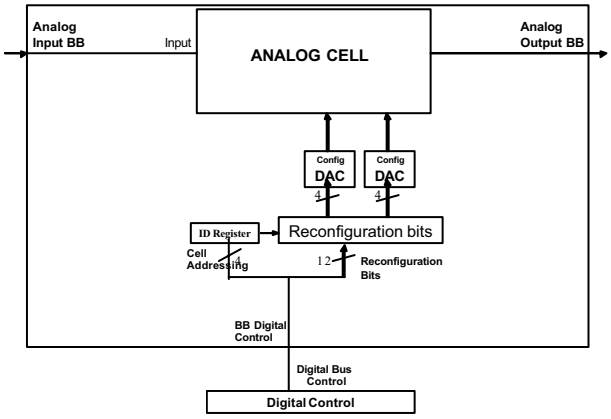

Figure 3: Functional Analog Cell

3.3 Reconfiguring circuit topologies by Signal Switch Box (on-chip controls)

The switch box allows for the configuration of different functions in the functional analog array, as well as providing an interface between the reference analog cells and the test fixture. The signal switch box is logically divided into 8 sub-blocks or chains, each of them associated with the configuration of a system level function. Figure 4 shows a block diagram representation of an individual chain, as well as the control signals. Each chain is implemented as a shift register structure, in which each flip-flop controls the state of a transmission-gate switch. A *select* signal enables 1 out of 8 chains; the *clock* signal shifts the data, which is latched at the end of the configuration.

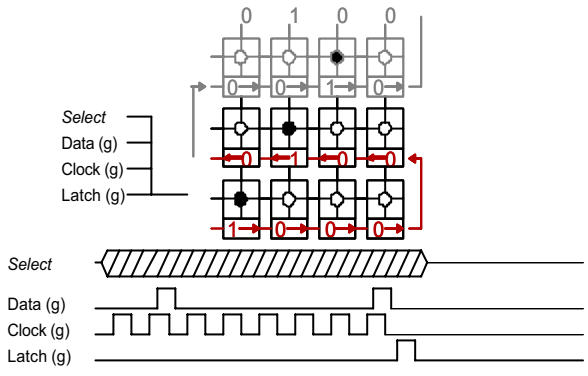

Figure 4. Configuration of a switch box chain

3.4 Tuning cells by programmable controls

All analog cells have one or more extra input points that allow circuit calibration for extreme temperature recovery. As an example, a ping-pong OpAmp circuit was designed which has two current mode calibration points that are used to bias the pre-amps. Other cells use voltage mode calibration points. The biases are obtained from DACs, as shown in Figures 2 and 3.

3.5 Digital programmable controls for function select and SRAA operation

The SRAA is initialized through the configuration of one or more system applications in the functional array. In the current implementation the switch box interface signals shown in Figure 4 are obtained from an external FPGA. The associated DACs of the functional cells (Figure 3) being utilized are programmed to provide the default (room temperature) calibrating voltages/currents for the functional cells. These DACs are also programmed by the FPGA (Figure 5).

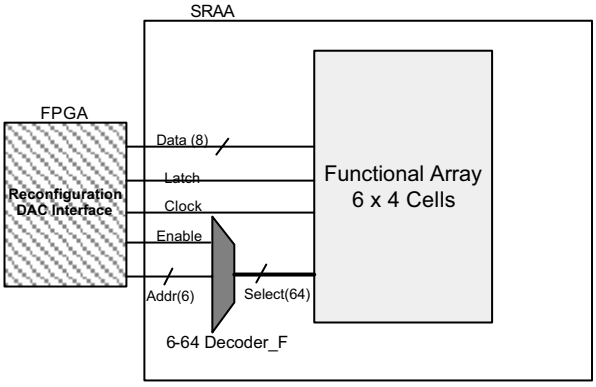

Figure 5. Functional Array DAC Interface.

Each cell of the functional array includes 1 or 2 reconfiguration DACs. There are a total of 40 reconfiguration DACs for the 6x4 functional array. These reconfiguration DACs are programmed sequentially and selected through the decoder shown in the figure above. Each DAC will share a data bus and the other control signals (Latch and Clock in the figure above). The reconfiguration DACs of the reference cells are programmed using a similar interface with the default (room temperature) calibration values for the analog cells.

Once the functional and reference array are programmed, the reference cells are sequentially monitored to check for behavior degradation, particularly when the chip is exposed to extreme temperatures or radiation. The reference cells are tested using the test fixture, which consists of two (excitation) DACs and two ADCs as shown in Figure 1. These data converters are also controlled through the FPGA, the interface being shown in Figure 6. As an example, the slew-rate of an OpAmp cell can be monitored by the application of a step voltage through the excitation DAC and evaluating the response coming from the excitation ADC.

Figure 6 shows the excitation DAC/ADCs, each with its own 8-bit data bus. The FPGA also provides the control signals for the DAC (clock, latch and select) and ADC (RST and clock). Two excitation DACs are needed to provide up to 2 inputs to the reference cells; one ADC to probe the cell output and the second to probe one of the inputs.

Once an analog cell response goes out of specification, possibly due to temperature or radiation effects, the FPGA will recalibrate the corresponding reference cell by reprogramming its respective reconfiguration DACs. This involves a search process over the possible calibrating voltage/currents at the particular analog cells. The search process will be controlled by a third digital ASIC chip that implements a search algorithm. Once new values are found that recover the behavior of the reference cell, the same are used to re-program the configuration DACs of the associated functional cells.

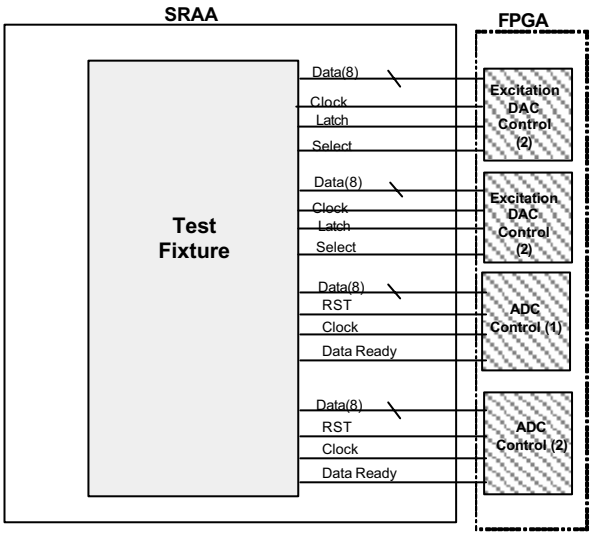

Figure 6. Test Fixture/FPGA interface

This tuning process assumes that for each type of cell, its functional and reference versions will display the same behavior. This assumption may usually hold when the SRAA chip is exposed to extreme temperatures; nevertheless, it will probably not hold when the chip is exposed to transient radiation effects (SEU – single event upset), since its effect is not uniform across the chip. In this case the functional cells will also have to be probed individually for correction. Since the chip is fabricated in a rad-hard process (Honeywell), the SRAA will tolerate permanent radiation effects (Total Ionization Dose -TID) up to 300Krad.

Finally, the data converters are also assumed to be temperature insensitive based on simulations. However, due to limitations in the simulation models, the actual behavior may present variations. Small temperature variations (such as offset or small decrease in resolution) in the data converters can possibly be compensated by the inherent feedback control performed by the search algorithm.

4. Mapping a variety of circuits by selective interconnect of SRAA cells

4.1 Mapping circuits into SRAA

This section illustrates examples of circuit implementations using the SRAA cells. This is shown in Figure 7 for the instrumentation amplifier. This circuit uses two types of functional cells, conventional and Ping-Pong OpAmps. The cells and external I/Os are interconnected through 18 switches controlled by the switch box chain assigned to the Instrumentation Amplifier function. Different circuit implementations can be selected depending on the switch configuration.

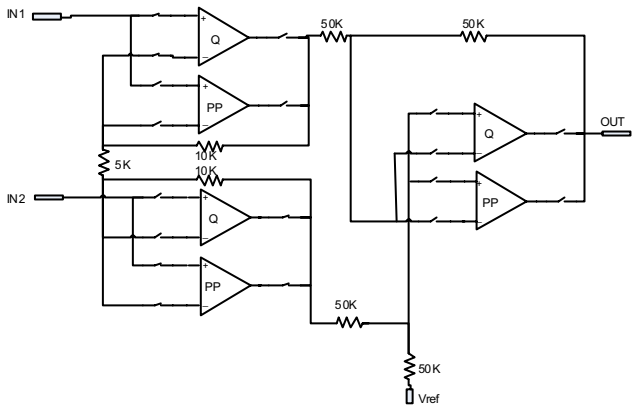

Figure 7. Instrumentation Amplifier implementation. Q is Quad (regular) OpAmp and PP is Ping-Pong OpAmp.

Figure 8 illustrates the implementation of a pulse width modulator (PWM) circuit, which uses two functional analog cells, the high speed (HS) comparator and conventional comparator. This circuit can be used to control a switched power supply. The switch chain configuration allows the selection of one or other comparator to implement the circuit. It should be noticed that the analog cells are reused in other applications, i.e., different switch box chains usually share the analog cells.

4.2 Functional simulations

This section shows simulation results of circuits mapped into the SRAA cells. Figure 9 depicts the transient simulation results of the instrumentation amplifier shown in Figure 7.

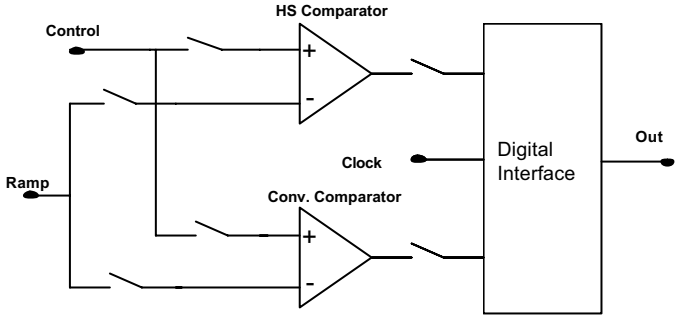

Figure 8. Comparators in Pulse-Width Modulator (PWM) circuit

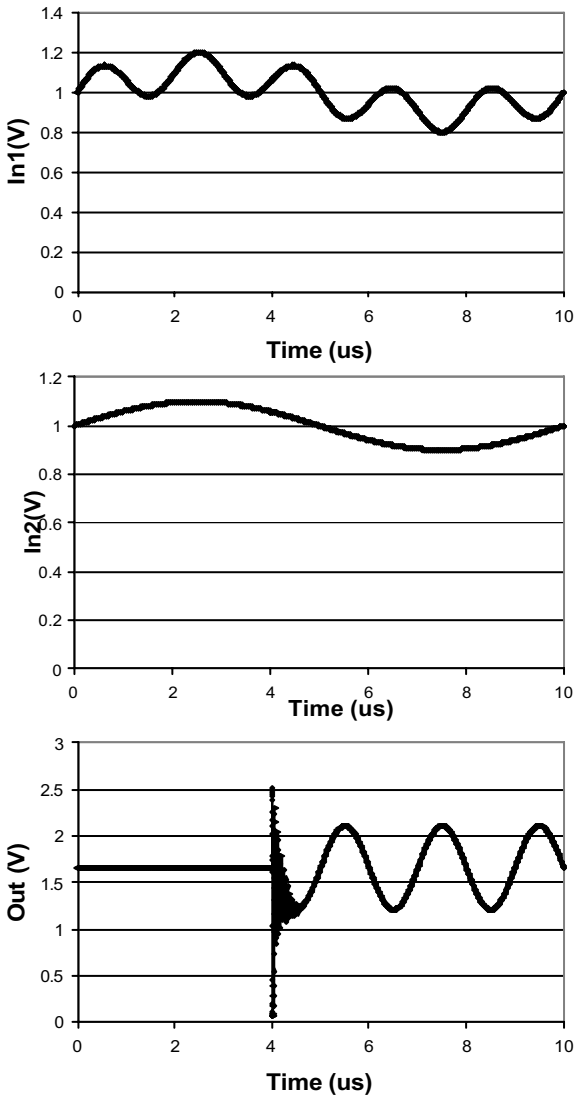

Figure 9. Differential and common-mode signals (top); common-mode signal (middle); and circuit output (bottom)

All the switches are opened until 4μs after, when the switch chain is programmed. The instrumentation amplifier amplifies the differential input (higher frequency in this case) and rejects the common mode signal (lower frequency).

Figure 10 shows the simulation results of the PWM circuit shown in Figure 8. This circuit takes three inputs (ramp, clock, and control) and produces one output. The pulse width at the output increases with the control input as shown in Figure 10.

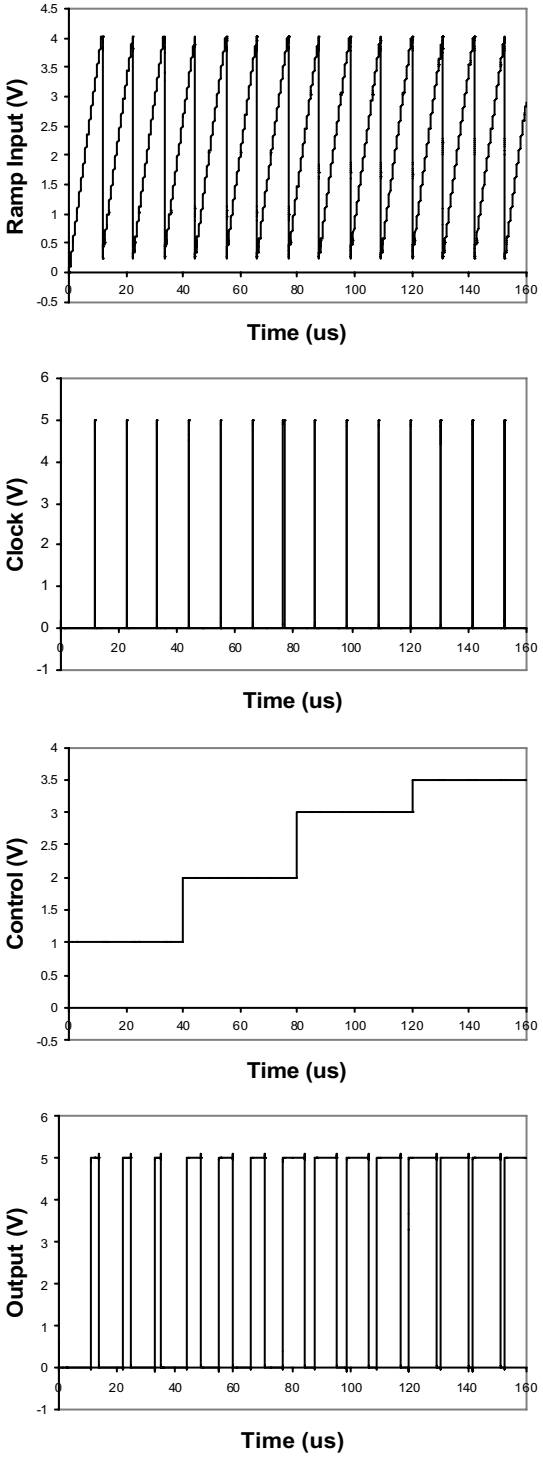

Figure 10. PWM circuit response

4.3 Adaptation to environment

A hierarchical approach to calibration/compensation has been adopted. A first

level compensation involves mapping corrections that were predetermined, either through model-based computation or tests with the devices in the actual environment. A second level involves finding solutions through gradient-descent searches that are less computationally expensive and hence faster. Finally, a third level is employed in case that previous levels did not succeed, and a global search, using evolutionary algorithms, is employed.

5. Conclusions

The SRAA offers a solution to the need for flexible, survivable extreme environment electronics. The flexibility offered by the presence of a wide variety of cells allows the implementation of a number of functions for sensing and actuation applications. Simulations show that the chosen architecture is capable of implementing in the same chip, by consequent configuration/ reconfiguration, a variety of topologies that previously were implemented with specialized ASICs.

The SRAA is designed to maintain a stable operation over a wide temperature range of more than 300C, from –180C to 125C. Over this range, parameters of interest may vary with less than 1-5 % deviation from their 27C value, depending on the circuit. This is achieved by temperature-oriented designs and exploitation of tuning points additionally included in the circuits and which allow algorithmic driven digital programmable compensation through programmable current/voltage signals/biases. The availability of the SRAA as an off-the-shelf component for space avionics designs would greatly reduce the development cost and development and integration/ validation time.

Special innovations contributed with this SRAA include:

- A solution for on-line adaptation by the use of functional cells and reference cells. While the functional cells are actively involved in the mapped function, the reference cells are monitored and calibrations are determined in the case of deviations. The calibration/tuning is then transferred to the functional cells without stopping the operation.
- A hierarchical approach to calibration/ compensation is used. A first level involves mapping corrections that were predetermined, either through model-based computation or test with the devices in the actual environment. A second level involves finding solutions through gradient descent searches that are less computationally expensive and hence faster. Finally, a third level is employed in case that previous levels did not succeed, when a global search, using evolutionary algorithms, is employed.

Acknowledgements

The research described in this (publication or paper) was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

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