

A 2.7-kW, 29-MHz Class-E/ F_{odd} Amplifier with a Distributed Active Transformer

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Abstract — A Class-E/ F_{odd} high power amplifier (PA) using the distributed active transformer (DAT) is demonstrated at 29MHz. The DAT combines the output power from four VDMOS push-pull pairs. The zero voltage switching (ZVS) condition is investigated and modified for the Class-E/ F_{odd} amplifier with a non-ideal output transformer. All lumped elements including the DAT and the transistor package are modeled and optimized to achieve the ZVS condition and the high drain efficiency. The PA exhibits 2.7kW output power with 79% drain efficiency and 18dB gain at 29MHz.

Index Terms — Class-E/F, Distributed active transformer, Power amplifiers, Switching amplifiers, Zero voltage switching.

I. INTRODUCTION

The high-efficiency power amplifier (PA) is a key component for various applications in the HF and VHF bands. The applications include plasma generation, RF heating, semiconductor processing, and medical imaging at industrial, scientific, and medical (ISM) frequencies such as 13.56, 27.12, and 40.68MHz [1], [2]. FM transmitters for broadcasting also need high-efficiency PAs. The output power level required for these applications is typically 1 - 50kW, and solid-state PAs are replacing vacuum-tube PAs up to the 5kW level as the transistor technology progresses. However, it is hard to achieve such an output power from a single transistor, and thus the PA needs a power-combining structure.

The distributed active transformer (DAT) has been proposed as an efficient way to combine the output power of several push-pull amplifiers by connecting the secondary circuit of magnetically-coupled 1:1 transformers in series [3]. It also provides each transistor with the output impedance transformation in order to boost the available power from the given device. The DAT was originally demonstrated for a CMOS integrated PA. The PA fabricated by a 0.35- μm CMOS process combined eight transistors using the DAT, and achieved 1.9W output power with 41% power-added efficiency at 2.4GHz [4].

In this work, the DAT is applied to a discrete amplifier with kilowatt-level output power, and implemented by lumped elements as shown in Fig. 1. Four push-pull VDMOS pairs independently operated in Class-E/ F_{odd} mode are combined by the DAT built of two stacked copper slabs, which are thick enough to handle high current through them. The Class-E/ F family has been proposed to take full advantage of both Class-

E and Class-F¹ characteristics [5]. A 1.1-kW Class-E/ $F_{2\text{odd}}$ PA was demonstrated at 7MHz with a drain efficiency of 85% [6].

This paper demonstrates a Class-E/ F_{odd} PA using the DAT structure at 29MHz with an output power of 2.7kW, a drain efficiency of 79%, and a gain of 18dB. The DAT of the stacked copper slabs is modeled by a magnetically coupled equivalent circuit. The parameters of the circuit are extracted as functions of the slab length, and optimized for satisfying the zero voltage switching (ZVS) condition.

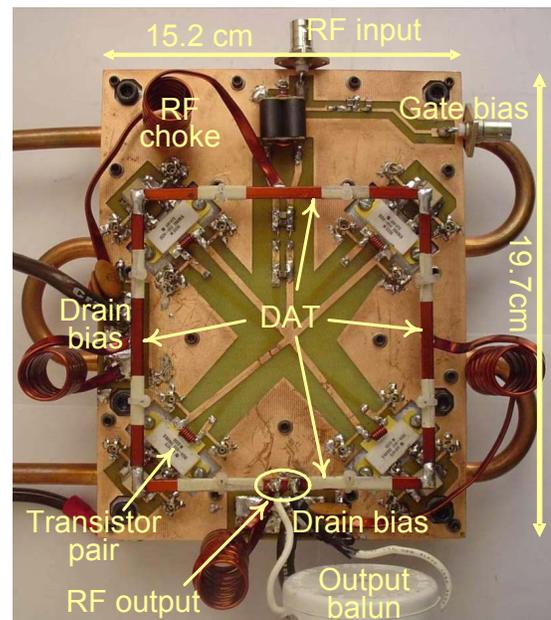


Fig. 1. Photo of the constructed amplifier with the DAT: The transistors are mounted on a water-cooled heatsink with dimensions of 15.2cm x 19.7cm. An output power of 2.7kW with 79% drain efficiency and 18dB gain is achieved at 29MHz.

II. CLASS-E/ F_{odd} OPERATION OF PA WITH DAT

Due to the distributed nature of the DAT and the symmetry formed between two adjacent pairs, the complete amplifier can be divided into four independent push-pull amplifiers for analysis convenience. The equivalent circuit of the push-pull amplifier is shown in Fig. 2 with a transistor modeled as an ideal switch in parallel with a capacitance C_s . L_m and L_{ll} represent a magnetizing and a leakage inductance of the

output transformer with a finite coupling coefficient k , respectively. The leakage inductance of the secondary winding is absorbed in the detuning reactance X_L .

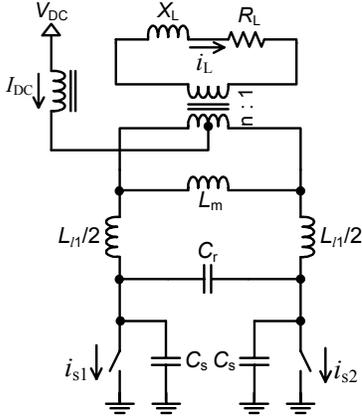


Fig. 2. A Class-E/F_{odd} push-pull amplifier with a non-ideal output transformer.

We can extend the analysis of Kee, *et al.* [5] to Fig. 2 to find the condition of the fundamental load admittance required for satisfying the ZVS condition:

$$Y_L = \frac{1}{R_L + jX_L} = G_L + jB_L$$

$$= \frac{2n^2 I_{DC}}{\pi^2 [1 - \omega_0^2 (C_s + C_r) L_{r1}] V_{DC}} - jn^2 \left[\frac{\omega_0 (C_s + C_r)}{1 - \omega_0^2 (C_s + C_r) L_{r1}} - \frac{1}{\omega_0 L_m} \right]. \quad (1)$$

Several important observations can be made about the load condition. Both G_L and B_L are functions of different circuit parameters: the leakage inductance, the capacitance in the resonant tank, as well as the transistor output capacitance. In a Class-E/F_{odd} amplifier with an ideal output transformer, however, B_L is a function of a single parameter, that is, the transistor output capacitance [5]. The load susceptance in (1) compensates not only for the transistor output capacitance, but also for a deviated reactance in the resonant tank. The deviation from the ideal parallel resonance at the operating frequency ω_0 is caused by the leakage inductance. The required load susceptance may even be capacitive depending on the coupling coefficient of the transformer, while it is always inductive in an amplifier with an ideal transformer.

The fact that the load resistance should be positive in any case imposes a condition on the operating frequency as follows:

$$\omega_0 < \sqrt{\frac{1}{(C_s + C_r) L_{r1}}}. \quad (2)$$

From (2), it is clear that the coupling coefficient of the output transformer should be maximized in order to increase

the operating frequency for a given active device and a given Q -factor of the resonant tank. Note that (1) will be equal to the load condition for the ZVS in [5] and no frequency limitation will be presented by (2), if the transformer is ideal ($k = 1$).

III. DESIGN OF CLASS-E/F_{odd} PA WITH DAT

The DAT is implemented by two copper slabs with a cross section of 4.8mm x 1.3mm, stacked up together 10mm above the ground plane as shown in Fig. 3(a). The copper slabs are isolated from each other by an enamel coating on the surface. The lower slab behaves as the primary circuit of a 1:1 transformer. The two ends of the slab are connected to each drain of the transistors in a push-pull pair. The upper slabs of four push-pull pairs, serving as the secondary circuits, are connected in series. They present a 1:8 impedance transformation of load impedance to each transistor. The DAT also combines the output power of 8 transistors by adding up AC voltages, magnetically coupled to the secondary circuits.

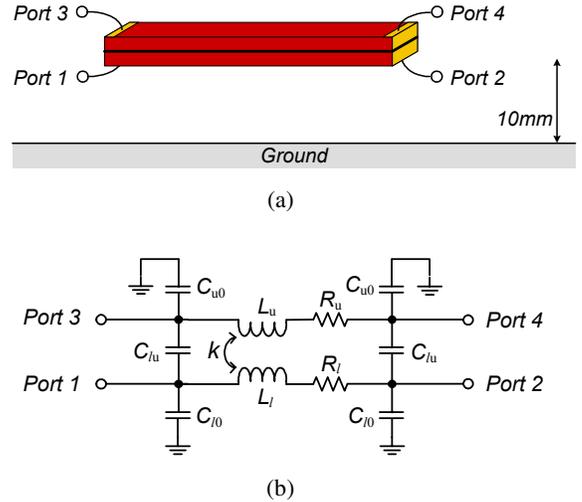


Fig. 3. The structure(a) and the equivalent circuit model(b) for the slab transformer.

Since the output transformer gives the required inductances for resonance and detuning as well, it is imperative to model the transformer accurately for simulation. Fig. 3(b) shows the equivalent circuit model of a quarter of the DAT, which corresponds to the output slab transformer of one push-pull pair in Fig. 2. 4-port S-parameter measurements were performed for slab transformers of different lengths with a network analyzer. The circuit parameters are then extracted as functions of the slab length by fitting the measured S-parameters to the simulated ones, shown in Fig. 4. As expected, all circuit parameters are linearly proportional to the length except the coupling coefficient of 0.84. The parasitic capacitances between the slab and the ground are negligibly small. It also should be noted that the Q -factor of the copper

slab is 600, so that the ohmic loss and the resulting heat problem can be drastically reduced, especially under the condition of the high current flow in this PA.

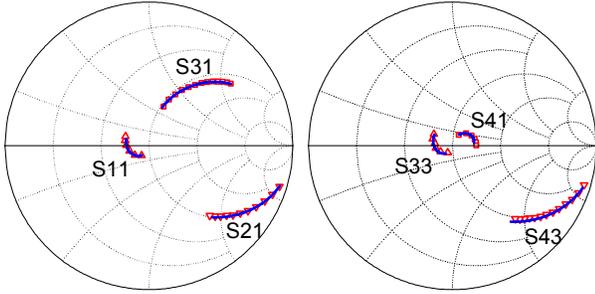


Fig. 4. Measured (symbol) and simulated (line) S-parameters of the slab transformer: slab length of 7.5cm, 50-200MHz. Only six S-parameters need to be fitted due to the reciprocity and the symmetry of the slab transformer.

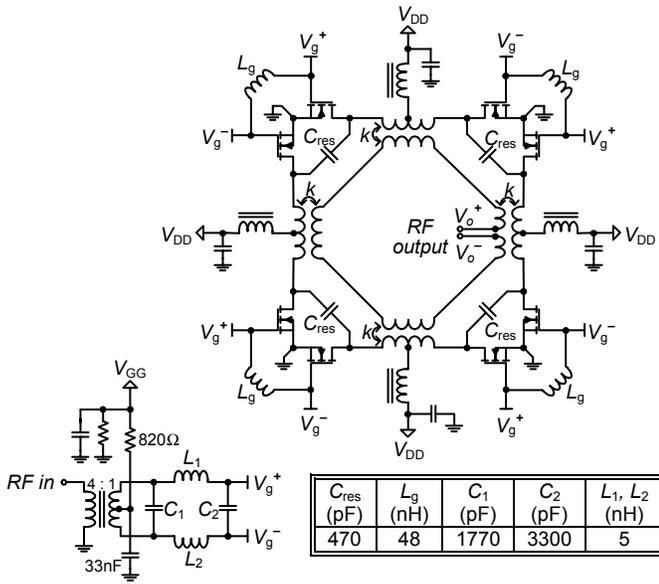


Fig. 5. Complete schematic of the Class-E/ F_{odd} PA with the DAT: Four push-pull pairs are combined by the DAT.

The complete schematic of the PA with the DAT is shown in Fig. 5. The active device used in this PA is the ARF473 VDMOS from Advanced Power Technology. It is a pair of matched power transistors in a common source configuration with 500V of maximum drain-to-source voltage and 10A of continuous drain current each transistor. The transistor is modeled by a simple switch in series with its on-resistance of 0.45 Ω , and a parallel nonlinear capacitance as a function of drain bias. The parasitic inductance of 3nH from the package is included in order to take into account a transient ringing in the simulation [7].

The capacitor C_{res} in Fig. 5 is connected between the drains belonging to adjacent push-pull pairs. Since the voltage across the capacitor is identical to the voltage between the drains of

the same push-pull pair, C_{res} can be regarded as being connected in parallel with the output transformer. The PA becomes a combination of four simple Class-E/ F_{odd} push-pull amplifiers of Fig. 2 with this connection.

The input matching network consists of lumped capacitors C_1 and C_2 , inductors L_1 and L_2 , and a 4:1 ferrite-core transformer. The input transformer also serves as a balun to drive the transistors in push-pull.

In the simulation, the value of C_{res} and the length of the output slab transformer are optimized to provide not only a parallel resonant tank at the operating frequency but also the appropriate susceptance given in (1) for the ZVS condition.

The simulation predicts a drain efficiency of 83% at an output power of 2.7kW. This includes a transistor loss of 13%, a capacitor loss of 2%, and an inductor loss in the slab transformers and the RF chokes of 2%. In addition, an external output balun has a measured loss of 7%, which means that the predicted overall drain efficiency will be 76%.

The amplifier is constructed on a FR-4 circuit board, shown in Fig. 1. The transistor packages are mounted on a water-cooled heatsink. For the capacitor C_{res} in the resonant tank, ATC 100E porcelain capacitor with a maximum working voltage of 2500V and Q of 450 at 29MHz is used. Since the DAT presents a balanced RF output, an external 1:1 output balun, B1-5K Plus from Radioworks, is employed for driving a conventional unbalanced load. The balun has a bandwidth of 2 - 50MHz, a loss of 0.3dB at 29MHz, and a power rating of 5kW at 3.5MHz.

IV. EXPERIMENTAL RESULTS

The RF input drive was applied by a Yaesu FT-840 transceiver. The output power of the amplifier was measured by a Bird 4024 power sensor and a 4421 power meter. The output spectrum was taken using an Agilent E4407B spectrum analyzer. The DC power supply was built by connecting several 12V sealed lead-acid batteries in series.

The measured drain voltage waveforms of the eight transistors for 2.7kW output power are shown in Fig. 6, where the simulated waveforms of two transistors are superimposed. Good agreement can be seen between them. The visible good balance among the measured waveforms leads to high drain efficiency. The transient ringing observed in the waveforms results from the parasitic resonance among the transistor package inductance, the transistor output capacitance, and the capacitance in the resonant tank.

Fig. 7 shows the gain and the drain efficiency versus the output power at 29MHz. The drain efficiency stays above 80% up to 2kW output power. The gain increases with the output power, as expected in a switching amplifier. At a drain voltage of 83V, an output power of 2.7kW is obtained with 79% drain efficiency and 18dB gain. This compares with 76% predicted drain efficiency. The input drive is 37W and the input VSWR is 1.3.

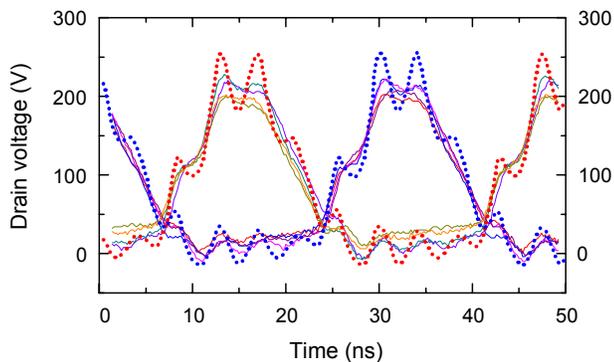


Fig. 6. Measured (solid lines) drain voltage waveforms of eight transistors for 2.7kW output power. Simulated (dotted lines) waveforms of two transistors are superimposed: The well-balanced half-sinusoidal waveforms confirm the proper Class-E/ F_{odd} operation with high drain efficiency. The transient ringing caused by the transistor package inductance can be observed.

The measured output power and input VSWR at a drain voltage of 72V are shown as a function of input frequency in Fig. 8. The output power exhibits a peak at the center frequency (29MHz), and the VSWR is better than 2:1 over a bandwidth of 1MHz.

The measured harmonic levels of the amplifier are shown in Table I. The largest harmonic is the 5th, at 34dB below the fundamental. Even harmonics are much lower than odd harmonics due to the push-pull operation of the amplifier.

V. CONCLUSION

A Class-E/ F_{odd} PA was simulated and built with four VDMOS push-pull pairs. The DAT was used in the PA both as an output impedance transformer and as a power combiner for the eight transistors. The amplifier exhibits an output power of 2.7kW with 79% drain efficiency and 18dB gain at 29MHz.

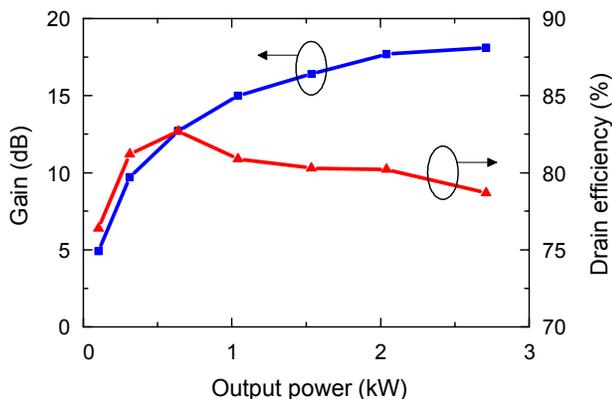


Fig. 7. Measured gain and drain efficiency vs. output power at 29MHz: The output power is varied by changing the drain bias voltage. At 2.7kW output power, the gain is 18dB and the drain efficiency is 79%.

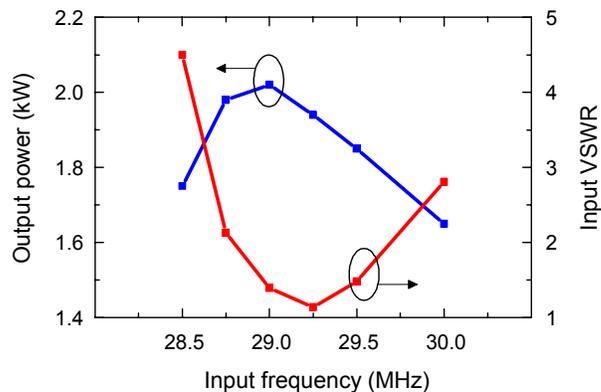


Fig. 8. Measured output power and input VSWR vs. input frequency for a drain voltage of 72V. The input bandwidth for 2:1 VSWR is 1MHz.

Table I. Harmonic levels of the amplifier (measured)

Harmonic no.	2nd	3rd	4th	5th	6th	7th
Harmonic level	-54dBc	-35dBc	-70dBc	-34dBc	-51dBc	-37dBc

ACKNOWLEDGEMENT

The authors appreciate the support of the Lee Center for Advanced Networking. We also would like to thank S. Weinreb, K. Potter, and F. Wang for their helpful advice.

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