Role of film conformality in charging damage during plasma-assisted interlevel dielectric deposition

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While observations of charging damage during plasma-assisted deposition have been erratic thus far, concern abounds that it may worsen as aspect ratios increase and high-density plasmas are used more frequently. Simulations of pattern-dependent charging during interlevel dielectric deposition reveal that the initial conformality of the dielectric film plays a crucial role in metal line charge up and the subsequent degradation to the buried gate oxide, to which the metal line is connected. For moderate aspect ratios, significant charging damage occurs for nonconformal step coverage.
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Charging damage is a serious problem in high-density plasma (HDP) etching of gate electrodes and metal interconnect lines.[1] It manifests itself as degradation or breakdown of thin gate oxides by tunneling currents that flow at the onset of and/or during the overetching step.[2,3] Concern over its adverse impact on reliability and yield at smaller critical dimensions has spurred widespread interest on charging damage, as evidenced in the increasing numbers of related publications.[4]

Most studies have focused on metal or polysilicon etching and resist ashing, where large aspect ratio features worsen electron shading, the origin of pattern-dependent charging.[4] Observations of charging damage during plasma-assisted deposition have been erratic; the few published reports have centered on interlevel dielectric (ILD) deposition in both conventional plasmas and HDPs. Cheung and Pai[5] reported serious charging damage during plasma-enhanced tetraethylorthosilicate (PETEOS) deposition of interlayer oxide at the metal-1 level which, surprisingly, increased with dielectric film thickness. Since the dielectric film should prevent the metal line from directly collecting charge, the latter trend was attributed to photoconduction, caused by vacuum ultraviolet photons from the plasma, which allows continued charging of the metal line through the oxide. Stamper, Lasky, and Adkisson[6] observed significant charging only during PETEOS of doped oxide; ''no measurable charging occurred during silane-based or undoped TEOS depositions.'' It was speculated that the introduction of dopant gas (trimethyl-phosphine) adversely affected plasma nonuniformity and oxide properties so that more charging ensued. Sporadic charging during undoped oxide deposition in conventional plasmas has been reported by Hook, Stamper, and Armbrust.[7] The inconsistent charging from run-to-run and between nominally identical plasma tools led these authors to conclude that their ''wafers were experiencing sporadic arcing events caused by virtually immeasurable differences in the individual tools at different times.'' They also used an HDP deposition process (at unspecified conditions) and found no evidence of charging damage. Earlier, Bothra *et al.*[8] compared conventional plasma-enhanced versus HDP oxide deposition and reported significant charging damage only for unoptimized HDP deposition performed at high plasma power. Interestingly, they also found that the damage in the unoptimized HDP could be prevented when a thin oxide layer was deposited first by the nondamaging PETEOS process.

The conflicting nature of the aforementioned observations suggests that charging damage during plasma-enhanced deposition may be more complex than that occuring during plasma etching. The migration towards HDP intermetal dielectric deposition, to improve gap-fill capabilities of higher aspect ratio trenches at lower temperature,[9] bears the risk of increased charging damage and warrants a theoretical study to understand how charging is brought about; only then can possible pitfalls and limitations of HDP tools and processes be uncovered in a timely manner.

Modeling of charging during ILD deposition requires coupling of various phenomena that occur simultaneously across disparate time- and length-scales, including surface charging,[10] charged particle dynamics in local electric fields,[10] electron tunneling,[11] and surface charge dissipation.[12] These phenomena are also coupled to film growth; for simplicity, we shall assume two extreme cases, schematically shown in Fig. 1: (a) neutral-flux-limited oxide growth, where the film thickness increases proportionally to the flux of the impinging neutral precursors (nonconformal step coverage), and (b) reaction-rate-limited oxide growth, where the film thickness is independent of the neutral precursor flux and the same on all surfaces at all times (conformal step coverage). In the former case, the oxide is thicker on top of the metal lines than at the bottom of the trench or at the sidewalls, a consequence of geometric shadowing of the isotropic neutral precursors by the topography. The realistic deposition process should be in-between the two extreme cases.[9] The detailed mechanism of the oxide growth is neglected. We also assume that electron tunneling through the bulk of the dielectric occurs as in very good quality oxide;[11] however, surface charge dissipation is controlled by

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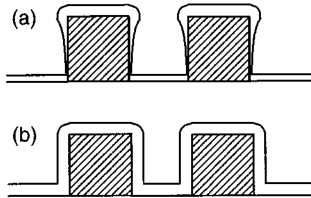

FIG. 1. Profiles of the deposited oxide by the two models considered: (a) neutral-flux-limited growth (nonconformal), and (b) reaction-rate-limited growth (conformal). Most of the charging damage occurs before the oxide grows to the thickness shown.

a threshold electric field, $\tilde{E}_s$, for subsurface conduction or surface discharging,[12] which depends on dielectric quality and surface adsorbates.[13] Photoconduction is neglected.

A cross-section of the structure to be simulated is depicted in Fig. 2. Metal lines of square cross-section (0.3×0.3 μm^2) extend in the direction perpendicular to the figure to a length such that the ratio of the area of the metal line (footprint) to the area of the gate oxide is 20 000:1 (antenna area ratio). The trenches are 0.3 μm wide (aspect ratio=1.0). The gate oxide thickness is taken to be 4.0 nm. The substrate is assumed to be grounded. Typical parameters for HDP are considered: low pressure (<10 mTorr), electron temperature=4 V, ion temperature=0.5 V, no applied radio frequency bias. Since we are interested in revealing the mechanism of charging damage, we shall assume a relatively high electron density of $5\times10^{12}\,cm^{-3}$; the results will be approximately valid for lower plasma densities (e.g., $5\times10^{11}\,cm^{-3}$), provided the antenna area ratio is increased by the same factor (e.g., 200 000:1). The surface discharge threshold is set at 1.0 MV/cm;[14] charge is allowed to dissipate freely along the surface in the direction of decreasing potential whenever the surface electric field exceeds the threshold value. As the deposition time is increased, the dielectric film thickness on the top surface and the sidewalls changes according to the two simple models described earlier. Monte Carlo based charging calculations, described in detail elsewhere,[10] are performed anew for each thickness considered.

The steady-state charging potential distribution around each metal line reveals the perturbation in the local ion dynamics occurring because of surface charging. Gradients on this potential surface are a measure of the electric field that influences ion motion. Figure 3 compares such distributions for nonconformal and conformal deposition, when the top film is 15 nm thick. For nonconformal step coverage [Fig. 3(a)], the potential of the metal line is positive at 6.4 V; the potential distribution peaks *near* the sidewall foot at about 10 V while a negative potential (−2 V) is visible at the upper sidewalls. For conformal step coverage [Fig. 3(b)], the metal line potential is almost zero; the potential distribution peaks *at* the sidewall foot at about 12 V while a slightly negative potential is apparent (as dips) at the upper sidewalls. The metal line potential develops as a result of a complex balance between tunneling currents through the film at the top and the sidewalls, surface currents along the sidewall and the bottom surface, and electron tunneling through the buried gate oxide. Electron shading is responsible for the negative charge at the upper sidewalls.[4] The negative potential deflects incident ions towards the sidewall, leading to positive charging along the lower sidewall, where the nonconformal film is thinner. Thus, tunneling currents may still flow to the metal line through that location, even when the top oxide is thick enough to stop tunneling through the top. The resulting potential increase is limited by electron tunneling from the substrate through the gate oxide. When the dielectric film is uniform (at 15 nm), tunneling at the lower part of the sidewalls ceases and the metal line potential is no longer affected. Note that charging along the oxide surface is now controlled solely by surface currents.

The variation in the metal line potentials during interlevel oxide deposition is shown in Fig. 4(a) for both conformal and nonconformal step coverage. The results are plotted as a

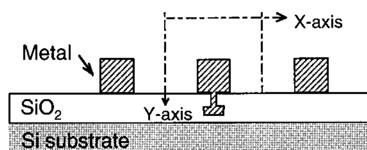

FIG. 2. Schematic of the structure considered and the simulation domain.

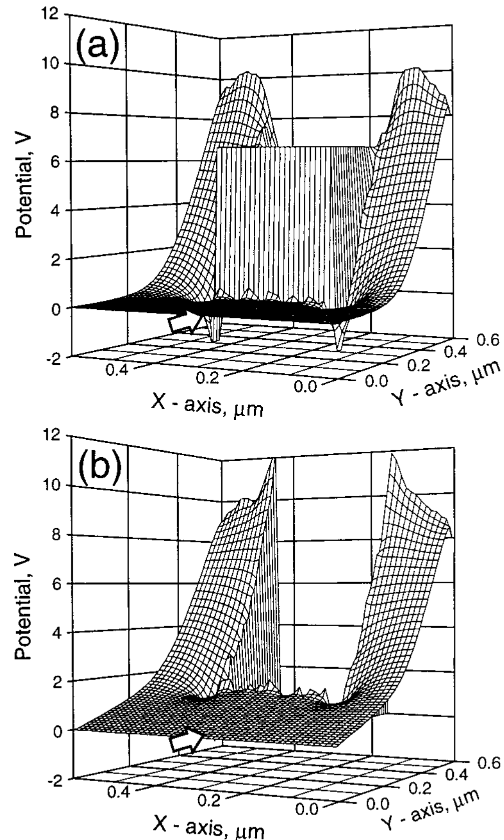

FIG. 3. Three-dimensional charging potential distributions around the metal line for oxide growth with (a) nonconformal and (b) conformal step coverage, when the top oxide thickness is 15.0 nm. The arrows show the direction of ions as they approach the potential surface. The axes are defined in Fig. 2.

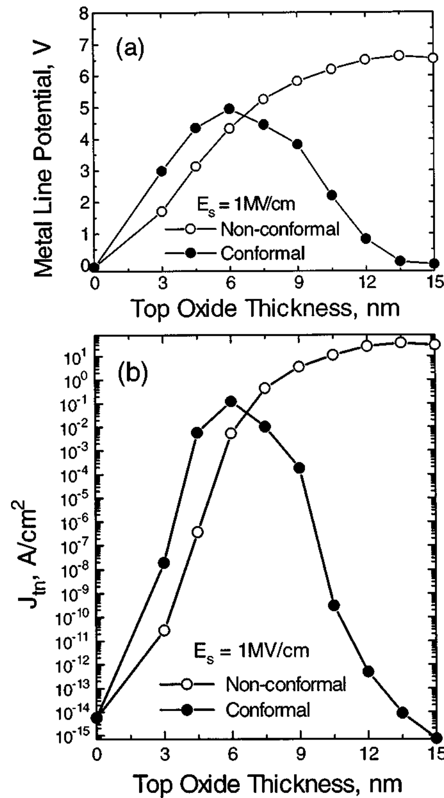

FIG. 4. (a) Charging potential of the metal line and (b) tunneling current density through the underlying gate oxide, as a function of the top oxide thickness (a measure of deposition time) for conformal (filled circles) and nonconformal (open circles) oxide growth.

function of top oxide thickness (a measure of deposition time). In both cases, the line potential first increases with oxide thickness, reaches a maximum, and then decreases. However, two important differences exist: (1) the magnitude of the potential maximum is larger in the case of nonuniform thickness oxide, and (2) the potential decreases a lot faster in the case of conformal oxide. When the oxide deposited on the metal surfaces is very thin, tunneling currents flow readily from all sides maintaining a low line potential. As the oxide thickness increases, tunneling becomes more difficult requiring larger potential differences to commence. Such differences build up at the lower part of the sidewall (positive potential) because electron shading prevents neutralization; the top surface is readily accessible by electrons which help maintain a low potential there. Thus, tunneling can still take place through the sidewalls but not through the top surface; as a result, the metal line potential increases until enough electrons are supplied from the substrate to establish current balance to the metal line. In nonconformal deposition, the oxide film is thinner at the lower part of the sidewalls, permitting larger tunneling currents to the metal line, which cause the line potential to increase until electron tunneling from the substrate forces a new dynamic current balance. The increased thickness of the oxide at the upper part of the sidewalls allows formation of a more negative potential there, which is responsible for the increase in the positive potential near the sidewall foot, as more ions are deflected. Since the oxide deposition rate is smaller at the lower part of the sidewalls, tunneling currents will flow longer there; thus, the metal line potential will decrease much slower than when the oxide is growing conformally.

Since the tunneling current through the 4.0 nm gate oxide depends exponentially on the metal line voltage, these observations suggest that the probability for oxide degradation due to large tunneling currents sustained over a longer period of time will be dramatically increased for nonconformal films. The steady-state tunneling current (J_{in}) through the gate oxide is plotted in Fig. 4(b) as a function of the top oxide thickness. Not only are the tunneling currents larger for the nonconformal deposition, but they also reach values suggestive of catastrophic failure,[15] e.g., 36 A/cm^2 when the top oxide is 13.5 nm thick! Moreover, the tunneling current decreases very slowly for thicker oxides, an indication that cumulative damage will be severe. When the film is deposited conformally, the calculated peak tunneling current occurs for a 6-nm-thick top oxide and is orders of magnitude smaller at 0.12 A/cm^2! The current decreases exponentially for thicker oxides; thus, the reduction in charging damage should be impressive. These results reveal the importance of achieving conformal step coverage in the initial stages of the deposition.

Charging damage is also affected by the quality of the deposited oxide. The assumption that its bulk dielectric properties are identical to those of perfect thermal oxide is rather simplistic. Defects in the oxide could allow bulk conduction at lower surface potentials; then, thicker oxides would be required to observe a behavior similar to that described. Even in this case, a nonconformal oxide will result in more charging damage as the oxide will still be thinner at the lower part of the sidewall near the potential maximum. The dielectric quality also influences the ability to sustain electric fields along the surface and, thus, charge buildup and dissipation. If surface discharging contributes to charge dissipation, it may be influenced by plasma radiation and/or surface adsorbates,[13] which depend on plasma parameters, chamber condition, and feedstock. Such dependencies may account for variability in charging damage from run-to-run or in otherwise identical tools.[7]

In summary, simulations of pattern-dependent charging during ILD deposition in HDPs predict significant damage to underlying gate oxides, brought about by an imbalance in tunneling currents to the metal line when the dielectric film grows nonconformally. Conformal step coverage during the early stages of dielectric deposition was found to be crucial for reduced charging potentials. The increase in trench aspect ratio, as the metal lines are brought closer together for denser integrated circuits, is expected to worsen ILD conformality and charging damage. The results suggest that charging from dielectric deposition may become a more serious problem than charging from etching. From this perspective, future materials proposed for ILD replacement must meet film conformality and charge leakage requirements more stringent than previously thought.

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[14]In the absence of experimental measurements of thresholds for surface charge dissipation (by surface discharging, subsurface conduction, or other mechanisms) at length scales of relevance (submicrometers), the choice of 1.0 MV/cm is arbitrary, albeit a reasonable guess; see also the discussion section in G. S. Hwang and K. P. Giapis, J. Appl. Phys. **84**, 683 (1998).
[15]The calculation of tunneling currents assumes that the gate oxide preserves its integrity irrespective of the magnitude of the current.