IMPLANTABLE RF-COILED CHIP PACKAGING

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ABSTRACT

In this paper, we present an embedded chip integration technology that utilizes silicon housings and flexible parylene radio frequency (RF) coils. As a demonstration of this technology, a flexible parylene RF coil has been integrated with an RF identification (RFID) chip. The coil has an inductance of 16 μH, with two layers of metal completely encapsulated in parylene-C. The functionality of the embedded chip is verified using an RFID reader module. Accelerated-lifetime soak testing has been performed in saline, and the results show that the silicon chip is well protected and the lifetime of our parylene-encapsulated RF coil at 37 °C is more than 20 years.

1. INTRODUCTION

Wireless retinal prostheses employ electronic systems to restore lost visual function due to such diseases as retinitis pigmentosa (RP) and age-related macular degeneration (AMD), and therefore demand high-resolution chip integration and packaging technologies without compromising flexibility and biocompatibility [1]. Traditional packaging technologies which use wire-bonding, flip chip, and tape automated bonding cannot meet these requirements due to their low reliability, non-biocompatibility, and high fabrication costs. A MicroFlex interconnection (MFI) technology has been developed [2], in which flexible polyimide substrates are fabricated as carriers, and individual devices are mounted to the polymer substrates using bump-bonding method. While devices packaged with this technology are flexible enough, their long term biocompatibility is not fully proved. Its tedious and low yield process also makes it difficult and costly to integrate high electrode density devices.

To overcome the challenges encountered in these traditional technologies, we developed a chip-level integrated interconnect (CL-I^2) packaging technology [3], and have now extended it to incorporate silicon housings and functional parylene-based devices. This new technology uses micro-electro-mechanical system (MEMS) techniques that enable the integration of complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) chips and prosthetic electrodes [4] so as to achieve high-level functionality. The chip-to-packaging interconnections are forged using standard microfabrication techniques including photolithography and metal etching; therefore, no wire-bonding, bump-bonding, or soldering are needed. Another advantage of our approach over traditional methods is that the density of interconnections is limited only by photolithography resolution, which offers the possibility to achieve high-lead-count (>1,000) integration. Finally, the favorable mechanical and chemical properties of parylene C [5] allow our final devices to be highly flexible and biocompatible for implantation.

2. DESIGN

Figure 1 depicts a conceptual schematic of our approach, in which individual prefabricated chips and passive components can be embedded in a carrier silicon wafer and sealed with parylene. After that, the fabrication of other surface MEMS components, such as electrode arrays and coils, can be performed on the same substrate using a parylene-based skin technology [6]. In our design, an EM4100 read-only RFID chip is used to demonstrate the integration technology, as shown in Figure 2(a). This chip is a CMOS integrated circuit, which can be powered up using an external coil through an electromagnetic field. By turning the modulation current on and off, the chip sends back a 64-bit sequence stored in the memory array. The operation frequency of the chip is between 100 kHz and 150 kHz, with 125 kHz being typical. In order to define the size of the chip housings where the chips are embedded, the chip dimension is measured using a WYKO interferometer, as shown in Figure 2(b). The chips have average dimensions of 1 mm in length, 0.98 mm in width, and 182 μm in thickness.

A square planar coil is designed for wireless power and data transmission. The coil consists of two metal layers with 22 turns on each layer. The overall coil size is 2 cm by 2 cm. During the fabrication, the two coil terminals are interconnected to Pad_1 and Pad_2 on the chip (Figure 2(a)). Due to the low power consumption of the wireless chip, only the coil is needed to power the circuit, and no extra capacitor is required.

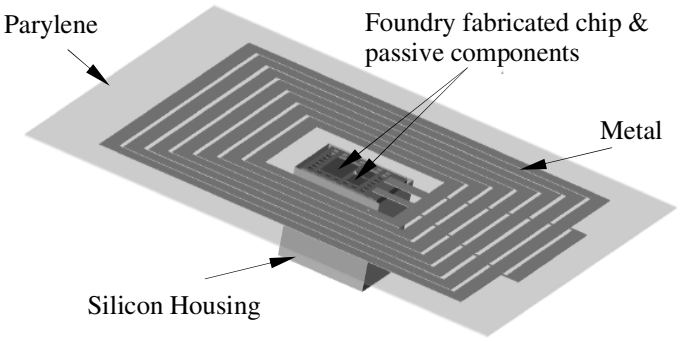

Figure 1: Concept of embedded chip integration.

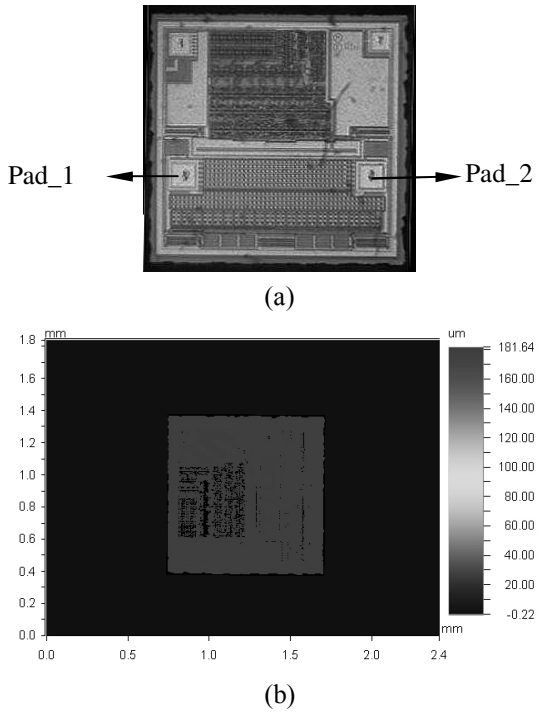

Figure 2: (a) EM 4100 RFID chip used to demonstrate the integration technology; (b) WYKO image of a typical chip.

3. FABRICATION

Figure 3 shows the detailed process flow, which starts with a standard 4 inch wafer coated with a layer of sacrificial photoresist. A 5 μm layer of parylene C is deposited on top of the photoresist. To secure parylene on the substrate, parylene anchors surrounding the chip housings are etched into the substrate using deep reactive-ion etching (DRIE) [7]. After parylene deposition, a 500 nm layer of gold is deposited using an E-beam evaporator, and patterned to form the first layer of coil wires. Next, cavities matching the chip dimensions are etched into the parylene and silicon using oxygen plasma reactive-ion etching (RIE) and Bosch process, and the chips are then dropped into the cavities to self-align with lateral displacements less than 10 μm. During this procedure, some epoxy is applied to the bottom of the cavities as needed in order to compensate for cavity depth inaccuracy and to fill the gaps surrounding the chips. A metal pole with a flat silicon piece attached on one end is used to push the chips into the cavities and to level the surface. The surface heights of the chips are measured using a profilometer, as given in Figure 4. The overall vertical displacements from the wafer surface are within 6μm, providing sufficient flatness for subsequent photolithography and metallization steps.

After the chips are fitted into the cavities, parylene deposition is performed again to seal the chips and to form an insulation layer between two metal layers, followed by oxygen plasma etching to properly open interconnection vias. A second 500 nm layer of gold is then deposited and patterned to form the top layer of coil wires and interconnects. Another 5 μm layer of parylene C is coated on top and patterned using oxygen plasma in the RIE to define the profile of devices. Through-wafer trenches surrounding the chips are then etched from the backside using Bosch process, and the flexible skin is released from the substrate, carrying the chips encapsulated in silicon housings. Lastly, the entire device can be sealed with parylene as a protection layer.

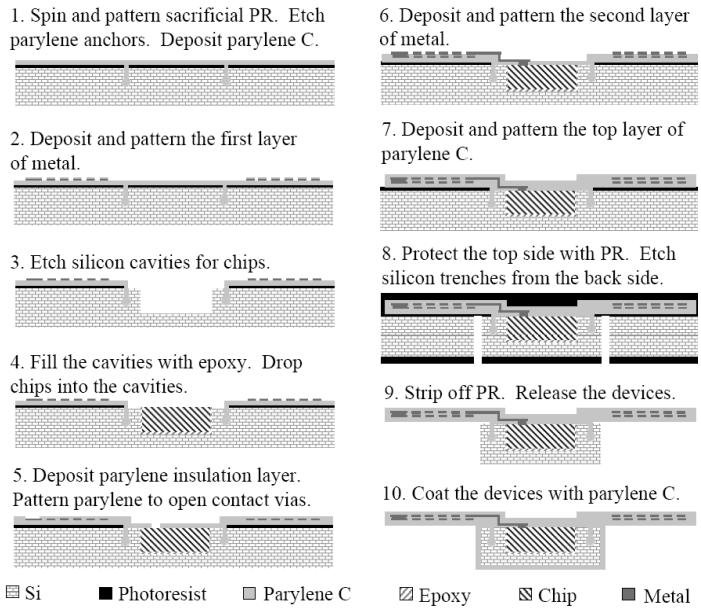

Figure 3: Detailed process flow for embedded chip integration.

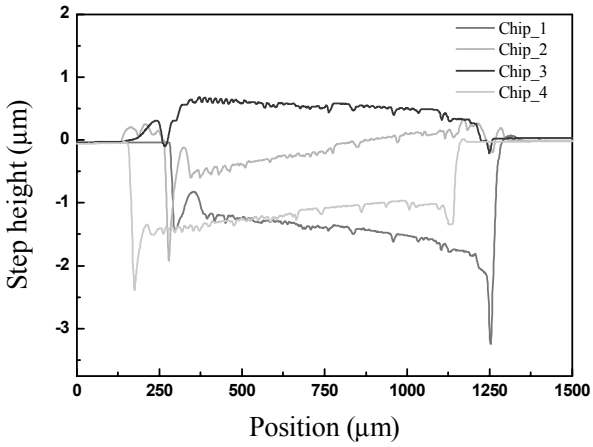

Figure 4: Vertical displacements of chips: 0μm step height indicates wafer level.

Figure 5 shows a fabricated device, in which the coil has an inductance of 16 μH measured with an HP 4192 impedance analyzer. The DC resistance of the coil is around 275 Ω measured with an Agilent 34401 multimeter. Figure 6 gives an example of an interconnection via after parylene patterning, which shows a lateral chip misalignment of approximately 10μm. With more precise chip-alignment lithography, this alignment deviation can be improved in the future to achieve high-lead-count integration. The total thickness of the

parylene-metal-parylene thin film is around 20 μm. Figure 7 demonstrates its flexibility, which allows the device to be placed in direct contact with delicate tissues during implantation.

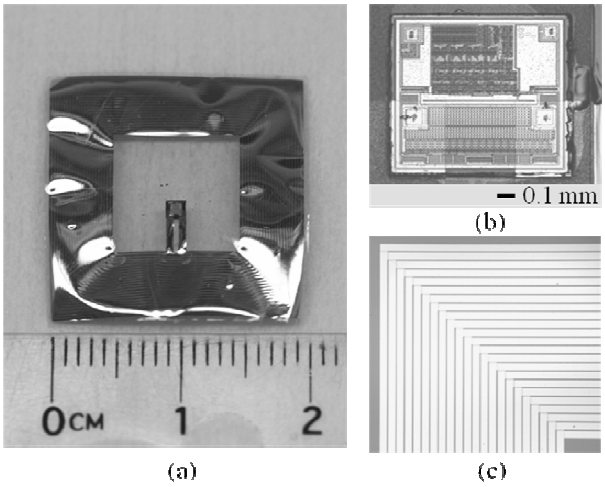

Figure 5: Fabricated parylene skin with an embedded RFID chip in a silicon housing: (a) Overall view of the device. (b) Close-up view of the embedded chip. (c) Close-up view of the coil wires.

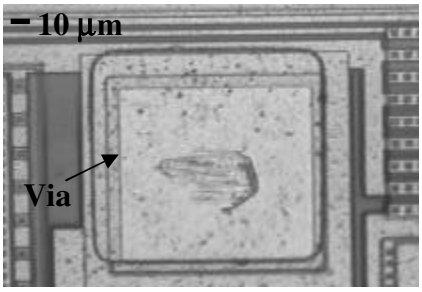

Figure 6: Example of ~10 μm lateral misalignment of the chip.

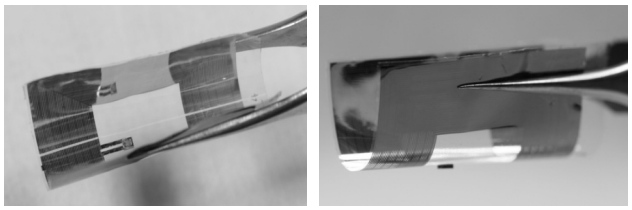

Figure 7: Flexibility of the parylene-packaged RFID chip.

4. TESTS AND RESULTS

The embedded RFID chip is tested using a commercial RFID reader module driven by a 5 volt DC voltage power supply, as shown in Figure 8(a). The reader module contains an integrated coil to transmit RF energy, as well as to receive the data from the chip. This transmission coil has dimensions of 60 mm by 66 mm. The output port of the reader is connected to an oscilloscope to monitor the signal readout. When the coil-integrated RFID chip is placed within reading distance of the reader, the information stored in the chip will be detected by the reader, and an 8-bit transistor-transistor logic (TTL) signal sequence can be observed on the oscilloscope. Figure 7(b) gives a typical square waveform of the output signal. The spatial separation between the device and the reader is varied during measurements, and a maximal detectable range of 3 mm to 4 mm is found. This short reading distance is mainly due to the small inductance of the receiver coil, which results in low power transmission through the electromagnetic field. For applications that require higher power and greater operating ranges, further improvements can be made to enhance the power transfer efficiency by modifying the coil geometry, such as increasing the number of turns or metal layers.

Accelerated-lifetime soak testing is also performed to evaluate the lifetime of the parylene packaging. RFID chips and coils are separately coated with 10 μm of parylene-C, and then annealed at 200 °C for 2 days in a vacuum oven. Unpowered testing is performed in hot saline, and the samples are monitored optically at distinct time intervals. No major physical damage or delamination is observed under the microscope after the chip has been soaked at 77 °C for over 90 days. For the parylene encapsulated coils, tests are done at two different temperatures, and a lifetime at body temperature of 37°C can be extrapolated using a Arrhenius relationship, which shows the parylene package can remain intact at 37 ºC for over 20 years [8].

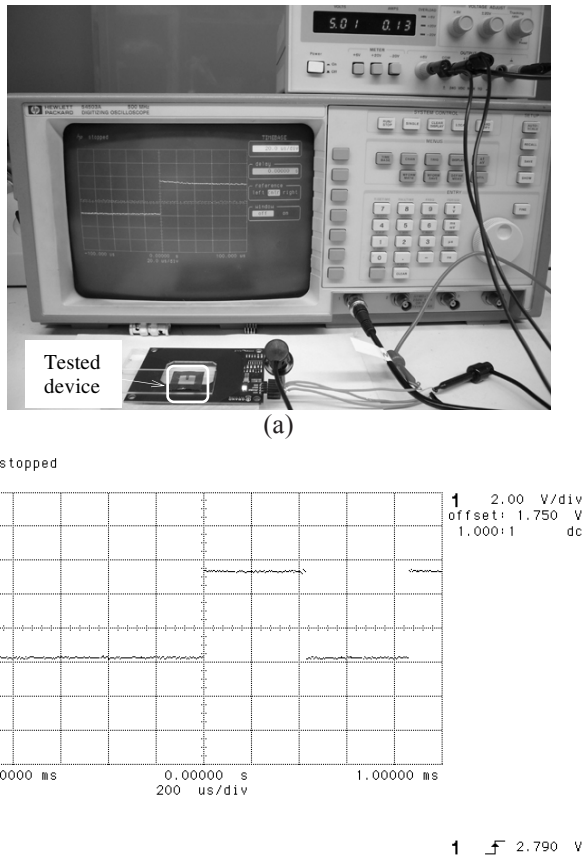

Figure 8: (a) Test setup to verify the function of embedded RFID chips. (b) Signal readout.

5. CONCLUSIONS

An embedded chip integration technology has been developed and successfully demonstrated by integrating a flexible parylene RF coil with a commercially available read-only RFID chip. The functionality of the embedded chip is tested using an RFID reader module. Preliminary accelerated-lifetime passive soak testing has also been done in hot saline, which shows positive results for bioimplant packaging using parylene. Although specifically tailored to the needs of retinal prostheses, this technology can also be used for other biomedical or IC applications by varying the circuitry and passive components to achieve different system functions. We are expecting to carry out long-term active soak testing to further characterize the parylene packaging performance.

6. ACKNOWLEDGMENTS

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7. REFERENCES

[1] J.D. Weiland, W. Liu, M.S. Humayun, "Retinal Prosthesis," *Annual Review of Biomedical Engineering*, vol. 7, pp. 361-401, 2005.

[2] J.-U. Meyer, T. Stieglitz, O. Scholz, W. Haberer, H. Beutel, "High Density Interconnects and Flexible Hybrid Assemblies for Active Biomedical Implants," *IEEE Transactions on Advanced Packaging*, vol. 24(3), pp. 366-374, 2001.

[3] D.C. Rodger, J.D. Weiland, M.S. Humayun, Y.C. Tai, "Scalable High Lead-count Parylene Package for Retinal Prostheses," *Sensors and Actuators B: Chemical*, vol. 117, pp. 107-114, 2006.

[4] D.C. Rodger, W. Li, H. Ameri, A. Ray, J.D. Weiland, M.S. Humayun, Y.C. Tai, "Flexible Parylene-based Microelectrode Technology for Intraocular Retinal Prostheses", in *Proc. IEEE-NEMS 2006,* Zhuhai, China, January 18-21, 2006.

[5] L. Wolgemuth, "Assessing the Performance and Suitability of Parylene Coating," *Medical Device & Diagnostic Industry*, vol. 22, pp. 42-49, 2000.

[6] Y.C. Tai, F. Jiang, Y. Xu, M. Liger, S. Ho, C.M. Ho, "Flexible MEMS Skins: Technologies and Applications," in *Proc. Pacific Rim MEMS Workshop,* Xiamen, China, 2002.

[7] M. Liger, D.C. Rodger, Y.C. Tai, "Robust Parylene-to-silicon Mechanical Anchoring," in *Proc. 16th IEEE Int. Conf. on Micro Electro Mechanical Systems*, Kyoto, Japan, January 19-23, 2003, pp. 602-605.

[8] W. Li, D.C. Rodger, E. Meng, J.D. Weiland, M.S. Humayun, Y.C. Tai, "Flexible Parylene Packaged Intraocular Coil for Retinal Prostheses," in *Proc. 4th International IEEE-EMBS Special Topic Conference on Microtechnologies in Medicine and Biology*, Okinawa, Japan, May 9-12, 2006, pp. 105-108.