Platinum diffusion into silicon from PtSi

A. Prabhakar, T. C. McGill, and M-A. Nicolet
California Institute of Technology, Pasadena, California 91125

(Received 4 August 1983; accepted for publication 26 September 1983)

We have observed platinum diffusion into the silicon underlying a PtSi film. Silicon substrates covered with platinum films were annealed at temperatures from 300 to 800 °C to form the silicide. Backscattering spectrometry spectra show no degradation of the silicide in the samples treated below 700 °C. Deep level transient spectroscopy (DLTS) was used to measure diffused platinum electron traps. Electron trap concentrations in samples treated below 700 °C are below the DLTS detection limit of $5\times10^{11}/cm^3$. Trap concentration profiles for the samples annealed at higher temperatures were obtained. These profiles cannot in general be explained by simple diffusion from an infinite source of platinum at the surface.

PACS numbers: 66.30.Jt, 71.55.Fr, 61.70.Wp, 81.40.Ef

Transition metal silicides have received a great deal of attention recently due to their applications in a number of devices.[1,2] One example is platinum silicide which has application in large scale integrated circuits[1] and in infrared detection schemes.[3] A difficulty with using transition metals in silicon systems is the possibility of poisoning the silicon with metal impurities during processing, since a large number of transition metals form deep traps in silicon. Platinum traps in silicon in particular have been studied because of their application as lifetime killers.[4] Thus, a knowledge of the effects of annealing on the metal diffusion into silicon is important in considering any silicide for use in a device.

In this letter we describe the observation of diffusion of platinum and its related deep levels into silicon from PtSi on the surface. Deep level transient spectroscopy (DLTS) and backscattering spectrometry (BS) were used to measure metal contaminants. DLTS observes traps in the depletion region of the reverse-biased Schottky barrier formed by the silicide-silicon structure, i.e., ~0.5–$7\,\mu$m from the interface. For our samples, trap concentrations above $5\times10^{11}/cm^3$ can be detected by DLTS. BS can detect *atom* impurity concentrations greater than about 0.1 at. % (5×10^{19} atoms/cm^3 in silicon) within $\sim0.3\,\mu$m of the interface of the structure. The two techniques measure what may be physically different configurations of platinum impurities, since BS measures total atomic concentration and DLTS measures only the electron traps, and the regions of the structure in which the measurements are made are different. Both these experiments offer little spatial resolution in the plane of the interface.

The samples used in this study were fabricated from 7–10-Ω cm n-type (100) silicon wafers which were cleaned and dipped in an HF solution before loading into an ion-pumped vacuum system. A 500-Å-thick platinum film was electron beam evaporated onto each wafer at a pressure less than 3×10^{-7} Torr. Regions of each wafer were masked to make 0.75-mm-diam diodes for the DLTS studies. The wafers were diced, and diodes as well as pieces with broad-area platinum coverage were annealed together at pressures less than 10^{-6} Torr at temperatures ranging from 300 to 800 °C. The pieces which were completely covered with the silicide were used for the backscattering analysis. The diodes, with In-Ga ohmic contacts on the backs, were mounted on headers and wire bonded to prepare them for DLTS profiling.

Backscattering spectrometry using 2-MeV $^4He^+$ ions was carried out on these samples. Figure 1 shows three of the resulting spectra. Analysis of the spectra using the ratio of the Pt signal leading-edge height to the Si signal leading-edge height yields compositions consistent with Pt_2Si for the 300 °C sample and PtSi for all higher temperature samples. The film thickness for each of the PtSi samples is approximately 1000 Å. The solid line in Fig. 1 shows the spectrum for the PtSi sample which was annealed at 600 °C for 30 min. This and all samples treated at lower temperatures exhibit Pt signals which fall off sharply on the low energy end, indicating abrupt silicide-silicon interfaces and smooth silicide surfaces. These Pt signals fall off as sharply as do Pt signals in the case of unannealed samples (Pt on Si).

Samples annealed at 700 and 750 °C (not shown in the figure) exhibit very small tails at the low energy end of the Pt signal. However, a significant platinum tail is seen in the 800 °C samples. Inspection of the surface with an optical microscope reveals a smooth topology, while scanning elec-

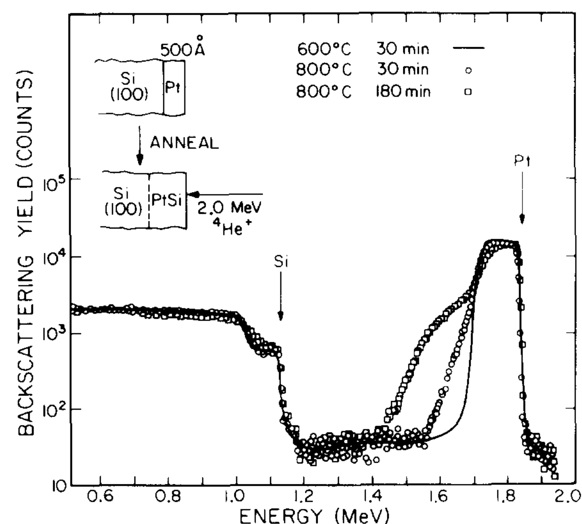

FIG. 1. BS spectra for PtSi-Si structures. These spectra were taken with the beam of 2-MeV $^4He^+$ ions incident normal to the sample and with the detector at 170° from the normal.

 © 1983 American Institute of Physics

Downloaded 22 Dec 2005 to 131.215.225.9. Redistribution subject to AIP license or copyright, see http://apl.aip.org/apl/copyright.jsp

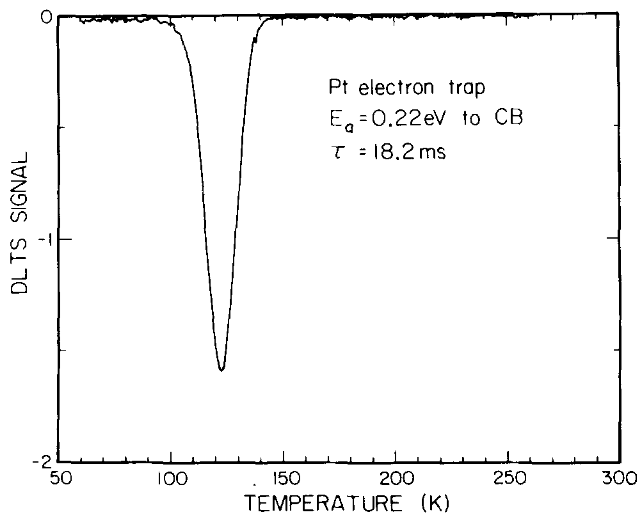

FIG. 2. Platinum electron trap seen in DLTS spectrum taken with time constant of 18.2 ms. E_a is the trap activation energy measured relative to the conduction band (CB).

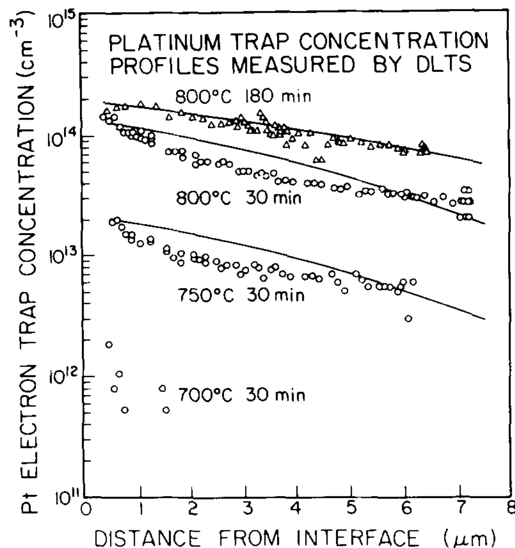

FIG. 3. Platinum electron trap concentration profiles obtained by DLTS. The solid lines are representative erfc's.

tron microscopy images reveal features approximately one micron wide. Thus the tail could correspond to a nonabrupt interface between the silicide layer and the substrate, or it could be a result of the surface roughness. The circles in Fig. 1 show the BS spectrum for PtSi annealed at 800 °C for 30 min. The tail at the low energy end of the Pt signal for this case is almost a straight line on this semilog plot. If we assume that it results from a nonabrupt interface, the slope of the tail corresponds to a decrease in the Pt atomic concentration of approximately one order of magnitude for every 0.2 μm from the interface, with a Pt concentration of $\sim 3\%$ at a distance of 500 Å from the interface. The squares in Fig. 1 show the spectrum for the sample treated at 800 °C for 180 min. In this final case, the low energy end of the platinum signal exhibits a large tail which is not a straight line. Here, the onset of the disintegration of the PtSi film is evident, as the number of counts at the peak of the platinum signal is approximately 10% less than in the samples which were treated for a shorter time.

The DLTS trap measurements were made using a Boonton model 72 BD capacitance meter. A double boxcar gating scheme[5] was used to analyze the capacitance transients of the Schottky barrier diode, which were caused by the emission of electrons by deep levels. A typical DLTS spectrum for a sample with a detectable concentration of platinum traps is shown in Fig. 2. For a scanning time constant of 18.2 ms, no other traps were observed in the samples up to 350 K. The trap observed was found to have an activation energy of 0.22 ± 0.015 eV, which is in good agreement with the value given by Brotherton *et al.*[6] for the platinum electron trap in silicon.

By applying reverse bias voltages from 2 to 25 V and changing the amplitude of the trap-filling pulses, we are able to observe electron emission from platinum traps in a region from 0.5–7 μm from the interface. The trap concentration profiles obtained by this method are shown in Fig. 3 for the samples which had detectable platinum trap concentrations. In the sample annealed at 700 °C for 30 min, we measure trap concentrations of $\sim 5 \times 10^{11}/\text{cm}^3$ which are just within our detection limit. Trap concentrations are approximately 10^{13} and 10^{14} for samples treated at 750 and 800 °C, respectively. The concentration profile for the sample which was annealed at 800 °C for 180 min falls off more slowly with distance from the interface than that for the sample annealed at the same temperature for 30 min, but the concentrations 0.5 μm from the interface are relatively close.

For simple diffusion of platinum from an infinite source at the surface, the concentration distribution at any temperature would be described by a complementary error function (erfc). The profiles we have measured are not in general described by complementary error functions, as our DLTS profiles bend in the opposite direction from erfc's. Thus, the distribution of platinum traps which we have observed is not due to simple diffusion. However, our profiles are similar in shape to the diffusion profile of gold in silicon, measured in Ref. 7 by radiotracer experiments. The profile in that case is thought to be a result of the interaction among Au atoms in substitutional sites, and silicon self-interstitials.[8] A similar theory could explain our platinum trap diffusion profiles.

To date, few attempts have been made to measure transition metal diffusion into silicon from a silicide at the surface. Ishiwara *et al.*[9] have reported the observation of platinum diffusion by backscattering spectrometry for PtSi on (100) and (111) oriented silicon wafers. Our BS spectra for (100) wafers show significantly less motion of the platinum atoms than theirs. In our sample which was annealed at 800 °C for 3 h, we measure 22% platinum diffusion in contrast to 53% for a 2-h 800 °C treatment reported by Ishiwara. Here, the percentage of diffused metal atoms is defined as the ratio of the area under the Pt tail to the total area under the Pt signal, and we have assumed, as they did, that the tails correspond to diffusion of platinum. Their samples were prepared in a manner very similar to ours, except that their evaporations were carried out at pressures about an order of mgnitude lower. The doping level in their substrates may also have been different, as the only information given about their substrates is the orientation. These differ-

Downloaded 22 Dec 2005 to 131.215.225.9. Redistribution subject to AIP license or copyright, see http://apl.aip.org/apl/copyright.jsp

ences may account for the disparity in the results.

Our DLTS studies of platinum diffusion into (100) silicon substrates from PtSi have shown that there is no observable diffusion at temperatures below 700 °C for our samples. BS spectra show that the PtSi phase is maintained at the surface at 800 °C for annealing times less than 3 h. The electron trap concentration measured by DLTS ranges from $2.0–0.5\times10^{13}/cm^3$ in the region from 0.5–7 μm from the interface for the sample treated at 750 °C for 30 min. In the 800 °C samples, the concentration range is $1.8–0.3\times10^{14}/cm^3$. Thus, we conclude that 700 °C is a safe temperature below which the silicon is not poisoned by the diffusion of platinum electron traps.

We would like to thank M. Finetti for her assistance. This work was supported in part by the Office of Naval Research under contract No. N00014-81-C-0285.

[1] F. Mohammadi, Solid State Technol. **24**, 65 (1981).
[2] M-A. Nicolet and S. S. Lau, in *VLSI Electronics: Microstructure Science*, edited by N. Einspruch (Academic, New York, 1983), Vol. 6, Chap. 6.
[3] W. F. Kosonocky, H. G. Erhardt, G. Meray, F. V. Shallcross, H. Elabd, M. J. Cantella, J. Klein, L. H. Skolnik, B. R. Capone, R. W. Taylor, W. Ewing, F. D. Shepherd, and S. A. Roosild, Soc. Photo-Opt. Instrum. Eng. **225**, 69 (1980).
[4] M. D. Miller, H. Schade, and C. J. Nuese, J. Appl. Phys. **47**, 2569 (1976).
[5] D. V. Lang, J. Appl. Phys. **45**, 3023 (1974).
[6] S. D. Brotherton, P. Bradley, and J. Bicknell, J. Appl. Phys. **50**, 3396 (1979).
[7] W. R. Wilcox and T. J. LaChapelle, J. Appl. Phys. **35**, 240 (1964).
[8] U. Gösele, F. Morehead, W. Frank, and A. Seeger, Appl. Phys. Lett. **38**, 157 (1981).
[9] H. Ishiwara, K. Hikosaka, and S. Furukawa, J. Appl. Phys. **50**, 5302 (1979).

Local oxidation induced dislocation generation near [100] Si_3N_4 film edges

J. Vanhellemont, J. Van Landuyt, and S. Amelinckx
Universiteit Antwerpen, R.U.C.A., Groenenborgerlaan 171, B-2020 Antwerp, Belgium

C. Claeys, G. Declerck, and R. Van Overstraeten
K.U. Leuven, E.S.A.T., Kardinaal Mercierlaan 94, B-3030 Heverlee, Belgium

(Received 8 July 1983; accepted for publication 26 September 1983)

The generation of dislocations at [100] nitride film edges on (001)Czochralski silicon wafers is studied by means of high voltage electron microscopy. After local oxidation 90° (edge) dislocations forming triangular half-loops with sides lying in $[21\bar{1}]$ and $[2\bar{1}1]$ directions in a (011) plane are found. It is observed that the shape of the surface stacking faults is also influenced by the mask orientation and that a denuded zone free from bulk defects is formed at the silicon surface. A novel model to explain the dislocation generation and movement under the influence of the stresses near the Si_3N_4 film edges is discussed.

PACS numbers: 61.70.Ga, 61.70.Jc, 81.60.Dq, 81.40. – z

Thin low-pressure chemical vapor deposited (LPCVD) Si_3N_4 films are widely used as masks to protect the active regions of integrated circuits during oxidation steps. The high intrinsic stresses at the nitride film edge can activate several dislocation sources caused by, e.g., surface damage, trapping of dislocations from external sources and subsequent multiplication, precipitates induced by metal contamination, and unfaulting of stacking faults. Above 950 °C viscoelastic flow of a thin silicon oxide layer (pad oxide) between the nitride mask and the silicon substrate, decreases the high stresses and prevents dislocation generation. A large number of papers have been devoted to a detailed study of the influence of the different parameters on the defect generation: the nitride layer thickness, the nitride/pad oxide thickness ratio, the oxidation temperature and time, the oxygen pressure and the ambient.[1–9] Most of these investigations are performed on (001) silicon wafers with nitride mask edges lying along [110] directions. Only little attention is given to the influence of the nitride edge direction on the defect generation.[6]

In this letter results on n-type, 15–30-Ω cm, 50-mm-diam, 350-μm-thick, (001) oriented Czochralski silicon wafers are reported. The mask pattern, consisting of 16-μm-wide parallel nitride bands with a 10-μm spacing, is defined by wet etching of the 120-nm-thick LPCVD Si_3N_4 layer in hot H_3PO_4 acid. The nitride bands are aligned in a [100] direction, making an angle of 45° with the wafer flat. The wafers are oxidized for 10 h in wet oxygen at 975 °C. After etching the field oxide and part of the nitride layer, plan-view transmission electron microscopy (TEM) specimens are prepared by backside chemical thinning. The TEM investigation is performed in a high voltage electron microscope operated at an acceleration voltage of 1250 kV.

Over the whole wafer surface a low density of dislocations in the shape of a triangular half-loop (THL) is observed lying in (011) planes that cut the (001) surface along the [100] nitride edges. The THL's consist of two 90° (edge) dislocation segments with 1/2[011] Burgers vector; these lie, respectively, in the $[21\bar{1}]$ and the $[2\bar{1}1]$ directions [Fig. 1(a)]. All the THL's show the remarkable property that after tilting the

 © 1983 American Institute of Physics

Downloaded 22 Dec 2005 to 131.215.225.9. Redistribution subject to AIP license or copyright, see http://apl.aip.org/apl/copyright.jsp