Piezoelectrically enhanced capacitive strain sensors using GaN metal-insulator-semiconductor diodes

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We report on the use of metal-insulator-semiconductor (MIS) diodes, formed on *n*-GaN with SiO_2, for capacitive strain sensing. These diodes, when subjected to static strain, were found to exhibit a steady-state change in capacitance. As a result, they can be used to detect strain with frequencies all the way down to dc. We formulate a model to explain the action of piezoelectricity in the diode and obtain excellent agreement with measurements. The model is then used to develop design criteria which optimize the sensitivity of the diode to detect strain. The sensitivity of the devices tested here rivals that of the best silicon piezoresistive sensors, but could attain nearly tenfold improvement with only minor design changes. Finally, we consider the effects of interface states on sensor performance and demonstrate how static strain sensing in GaN MIS diodes is enabled by the high quality of the oxide interface. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1611267]

I. INTRODUCTION

Piezoelectric effects lie at the heart of many existing III–V nitride devices, most notably the well-studied AlGaN/GaN heterojunction field-effect transistor (HFET) which has marked its place for high power and high frequency electronics.[1] These transistors are but one example of a broader class of *piezoelectronic* devices in the nitrides, devices which exploit the unique combination of large piezoelectricity with conventional semiconductor properties.[2] A natural, but somewhat neglected, extension of this class would be GaN semiconductor strain sensors.[3] The development of sensors of this type is especially germane given the broad range of suspended micro- and nanomechanical structures that can now be fashioned in GaN.[4] Highly sensitive strain detectors, integrated on these platforms, would open the door for an entire family of diverse and flexible sensors using GaN.

Recently, we demonstrated how the large piezoelectric effect in GaN can be exploited to create highly sensitive strain detectors using Schottky diodes.[5] Strain is measured through the voltage which develops across the diode due to its high intrinsic blocking resistance. Because this voltage is transient, GaN Schottky diodes, like other piezoelectric sensors, are only sensitive to dynamic strain, with a practical lower cutoff frequency of ~10 Hz. However, many applications, such as in pressure, force, or displacement sensing, call for the measurement of a strain which is either slowly varying or completely static. Sensing at dc would seem to present a serious challenge for GaN owing to the relatively high density of free carriers which will move, if given sufficient time, to negate any piezoelectric bound charge. In the following, we will show that static strain sensing in GaN is not only possible, but highly practical, using a simple MIS diode. Due to the piezoelectric bound charge which forms at the oxide interface, a dc strain will lead to a steady-state shift in the electrostatic surface potential inside the MIS diode. This shift, in turn, will cause a change in the diode capacitance. In this way, GaN MIS diodes can be operated like conventional capacitive strain sensors, but with a sensitivity that is orders of magnitude larger.

We present a study on the use of GaN MIS diodes as piezoelectrically enhanced capacitive strain sensors. Section II reports on the fabrication and interface quality of these diodes, as well as the experimental setup used to measure their response to static strain. In Sec. III A, a model is presented to predict the change in capacitance with strain for the case of an ideal diode without interface states. This theory gives excellent agreement with the measurements, in particular, with regard to: (i) the dependence of the capacitance change on the dc bias applied to the diode, and (ii) the linearity of this change with strain magnitude. In Sec. III B, the model is exploited to infer operational and design rules which optimize the sensitivity, or gauge factor; of the GaN MIS sensor. In the course of this discussion, we find that the devices tested here compare favorably with conventional semiconductor strain gauges, but could readily attain an order of magnitude improvement in sensitivity with only minor design changes. In Sec. III C, the detrimental role of interface states is considered. To illustrate their effects, we provide data on MIS diodes that were deliberately prepared to have a low quality oxide interface. By modifying the theory to include surface charging, we develop an objective criterion to gauge the effects of interface states on sensor performance. A notable consequence of this analysis is that static strain sensing in GaN is enabled not only by the large piezoelectric constants, but also by the low surface state densities which are attainable with this semiconductor.

II. EXPERIMENT

The GaN sample used in this experiment was grown by metalorganic chemical vapor deposition (MOCVD) on a

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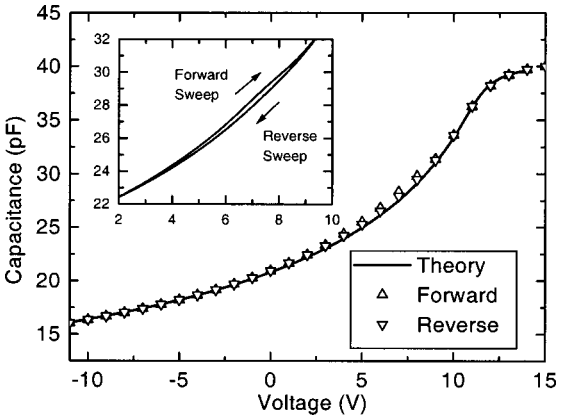

FIG. 1. Room-temperature $C-V$ characteristics for a 0.12 mm^2 GaN MIS diode showing both forward and reverse sweeps. The data were taken at a ramp rate of 0.01 V/s and a spot frequency of 100 kHz. The solid line represents a theoretical fit for an ideal diode. The inset shows an expanded view of a small hysteresis likely caused by interface states.

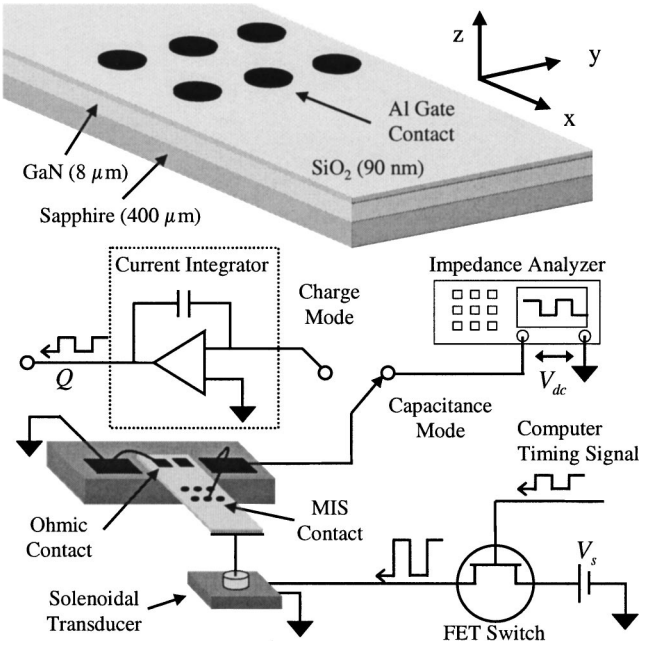

FIG. 2. Experimental setup used to measure the capacitance change and charge flow of GaN MIS diodes in response to strain.

c-plane sapphire substrate. The growth consists of three epitaxial layers: (i) a 40 nm AlN buffer layer; (ii) a 5.0 μm n^+-GaN base layer which was doped with Si at a level of $5\times10^{18}/cm^3$; and (iii) a 3.0 μm *n*-GaN surface layer doped at $7\times10^{16}/cm^3$. The growth resulted in Ga-polar (0001) film with a sheet resistance of 40 Ω/square.

To form the MIS diodes, a 90 nm SiO_2 layer was deposited on the GaN surface by plasma-enhanced chemical vapor deposition (PECVD) at a temperature of 350 °C. A 100 nm Al layer was then sputter deposited on the insulator and subsequently patterned into 390 μm diameter circular gate electrodes by etching down in phosphoric acid. The ohmic contacts, consisting of an Al–Ni–Au (50 nm–30 nm–50 nm) stack, were sputter deposited on the GaN surface in windows etched out of the insulator layer using hydroflouric acid. These contacts were ohmic as deposited.

The room temperature capacitance–voltage ($C-V$) characteristics of a typical MIS diode are shown in Fig. 1. The forward and reverse sweeps shown here were measured in the dark at a frequency of 100 kHz and a voltage sweep rate of 10 mV/s. The solid line shows a theoretical fit to the data using the exact solution for the high-frequency capacitance of an ideal MIS diode without interface states.[6] Due to the prohibitively low minority carrier generation rate in GaN at room temperature,[7] this analytical solution was modified to exclude the effect of any minority carrier holes. As a result, the capacitance exhibits a deep depletion characteristic for large reverse biases. The fit shown corresponds to a flat band voltage of $V_{fb}=12.0$ V and an oxide dielectric constant of $\epsilon_i=3.5\,\epsilon_0$.

A small capacitance hysteresis is evident in the expanded view inset of Fig. 1. The clockwise orientation of this hysteresis, as well as the slight ''ledge'' seen on the forward sweep,[8] are both consistent with the effects of interface states. Using the Terman technique,[9] we found a mean interface state density of 3.2×10^{11} $cm^{-2}\,eV^{-1}$ over the range of 0.3–0.65 eV below the conduction band edge. On the basis of measured time constants for electron emission from interface traps,[10] this narrow range in energy was deemed to be the limit of validity for the Terman method given our measurement conditions. The interface state density found here agrees well with previous measurements for PECVD SiO_2 on *n*-GaN,[11] but is significantly higher than the value of $<5.0\times10^{10}$ $cm^{-2}\,eV^{-1}$ quoted for optimized oxide/nitride/oxide insulator stacks.[10]

Figure 2 shows the experimental setup used to study the effects of strain on these MIS diodes. GaN samples, with dimensions 5×30 mm, were anchored at one end to a rigid support fixture to form a suspended cantilever. A wire, affixed at the free end of the cantilever, conveyed a mechanical line force to the sample from a solenoidal transducer below. Referring to the coordinate axes in Fig. 2, the resulting deformation of the GaN epilayer is a mixture of longitudinal strain in x (S_1) and in z (S_3). Using standard reduced notation,[12] these components of strain are related by:

$$S_3=-\frac{C_{31}}{C_{33}}S_1, \tag{1}$$

where C_{ij} are the components of the GaN elastic tensor. Given the relative thickness of the GaN epilayer (8 μm) to the sapphire substrate (400 μm), these strain conditions are approximately uniform in z across the film thickness, but vary in x along the length of the cantilever.

As seen in Fig. 2, the force supplied by the transducer was computer controlled by way of a digital timing signal sent to the gate of a high-power analog switch. The magnitude of this force could be adjusted by varying the supply voltage V_s of the switch circuit. Synchronously, an HP4192A Impedance Analyzer measured the capacitance of the MIS diode at a particular dc bias level. A representative trace of the resulting capacitance data is shown in Fig. 3(a); the corresponding timing signal is shown in Fig. 3(c). Because of the large fractional change in capacitance with strain, a Wheatstone bridge circuit was not necessary.

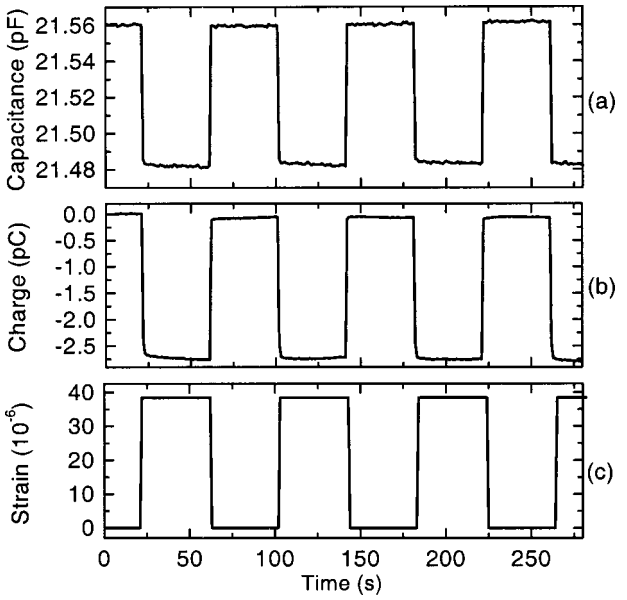

FIG. 3. Representative time series of the (a) capacitance and (b) charge measured from a MIS diode for a (c) strain cycled every 80 s. Traces (a) and (b) were recorded sequentially using identical strain conditions (c) and the same diode bias (0 V). The actual strain magnitude shown in (c) was inferred from the amplitude of the charge swing averaged over many cycles.

To calibrate the mean strain in the GaN epilayer immediately below the MIS diode, the total charge moving from the metal to the semiconductor side of the diode was monitored in time using an ultralow drift Keithley 6517A current integrator. A typical trace of this charge data is shown in Fig. 3(b). As discussed in Sec. III, the change in charge (from peak to trough in the trace) is related in a simple, linear manner to the change in strain of the diode. Charge and capacitance traces where taken sequentially under identical strain conditions, i.e., using the same timing signal and the same force level (V_s) applied by the solenoidal transducer. Using this method, the measured strain levels imposed on the diodes in this experiment were in the range from 10^{-6} to 10^{-4}.

III. RESULTS AND DISCUSSION

In the following section, we set forth a simple model to describe the change in steady-state capacitance of a GaN MIS diode resulting from an applied static strain. In this analysis, we are concerned with the final state of the diode, maintained at constant dc bias, a long time after the initial application of strain. The transient electrical response of the device, however, is the basis for a class of highly sensitive dynamic strain sensors in GaN; sensors of this type, using both MIS and Schottky diodes,[5] are treated elsewhere.

Whether static or dynamic, strain affects the state of a MIS diode by introducing piezoelectric bound charge within the semiconductor. For the coupled strain conditions in this experiment, equal and opposite sheet charge densities will form at the two *c*-plane faces of the epilayer, with a magnitude (σ_b) at the GaN/oxide surface given by:

$$\sigma_b = \left(e_{31} - \frac{C_{31}}{C_{33}} e_{33} \right) S_1 \equiv e'_{31} S_1 . \tag{2}$$

Here, e'_{31} denotes an effective piezoelectric constant having a value of -0.61 C/m^2 derived from reported material constants.[13]

However, the final state of the diode is determined not only by the bound charge, but also by the redistribution of free charge in response to the strain. For a MIS diode with no interface states, the insulating layer prevents the formation of a compensating sheet charge at the semiconductor surface, not because free carriers are unable to reach the surface, but because there are no states for them to occupy there. Thus, free charge cannot cancel the bound charge, but merely screens it at some distance, leading to a net change in the capacitance of the diode.

A. Model for an ideal diode

In the following part, we present a theoretical means to compare the state of the diode before and after strain in terms of the two quantities measured in this experiment: (i) the change in capacitance ΔC, and (ii) the total charge ΔQ which flows from the metal to the semiconductor side of the device. In addition to having no interface states, the diode is assumed to have an insulator layer containing no mobile charge.

Under these assumptions, the state of a GaN MIS diode is determined by the surface potential Φ_s, the electrostatic potential at the semiconductor–insulator surface relative to that in the bulk. In the steady state, this potential is related to the applied dc bias (V) and the imposed strain (S_1) via:

$$V_{bi} - V = \Phi_s + \frac{z_i}{\epsilon_i} \epsilon_s \dot{\Phi}_s + \frac{z_i}{\epsilon_i} e'_{31} S_1 , \tag{3}$$

where ϵ_i and ϵ_s are the insulator and semiconductor dielectric constants, z_i is the oxide thickness, and V_{bi} is the built-in voltage of the MIS junction.[6] In this sign convention, the spatial derivative of the potential is the electric field. The quantity $\dot{\Phi}_s$ appearing in Eq. (3) is the electric field in the semiconductor at the surface; for a fixed doping level, it is a function of Φ_s alone. It is therefore clear from Eq. (3) that if the diode is maintained at a constant bias, the application of strain will cause the surface potential to change.

This shift in Φ_s will be reflected in the capacitance per unit area (C_d) of the diode. The effect of piezoelectric bound charge [r.h.s. of Eq. (3)] is to shift the bias voltage corresponding to the same surface potential by an amount $\Delta V = e'_{31} S_1 / C_i$, where $C_i = \epsilon_i / z_i$ denotes the oxide capacitance per unit area. Since the capacitance is a function of Φ_s alone, strain will therefore simply translate the $C-V$ characteristics to the left by an amount ΔV along the voltage axis. In this regard, the piezoelectric charge is totally analogous to the familiar oxide fixed charge appearing at the surface in MOS diodes.[6] Thus, the change in capacitance per unit area is:

$$\frac{\Delta C}{A} = C_d(V + \Delta V) - C_d(V) \approx \left[\frac{dC_d}{dV} \right] \frac{e'_{31} S_1}{C_i} , \tag{4}$$

where the last equation applies in the limit of small strain.

In addition to the capacitance, the free charge on the metal surface will change as a result of strain. Using boundary conditions for the electric field at the metal–oxide inter-

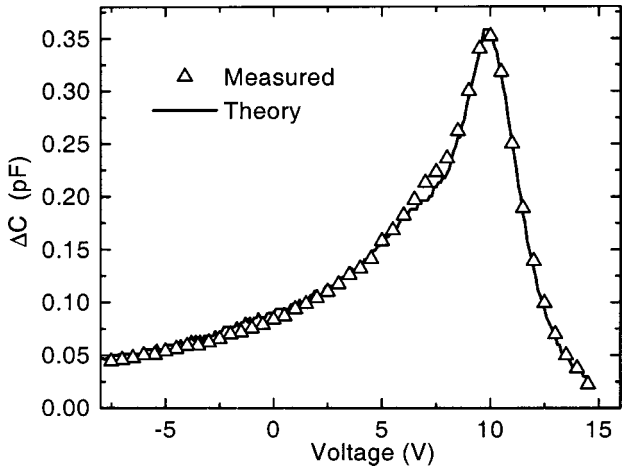

FIG. 4. Measured capacitance change ΔC vs diode bias for a strain magnitude of 7.0×10^{-5}. The solid line shows the theoretical prediction based on the empirical $C-V$ profile.

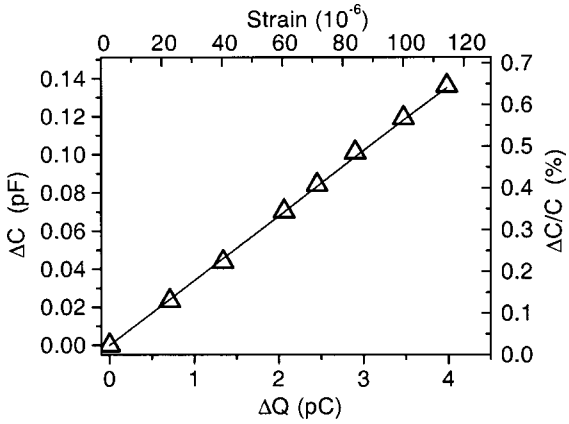

FIG. 5. Linearity of the capacitance change ΔC with the strain magnitude for a fixed bias of 0 V. Solid line represents a fit. For each datum, the strain (top axis) was directly inferred from the charge swing ΔQ (bottom axis) using Eq. (5). The right axis shows fractional change in capacitance.

face, the total charge ΔQ flowing from the metal to the semiconductor as a result of strain is found to be:

$$\Delta Q = A e'_{31} S_1 \left(1 - \frac{C_d}{C_i}\right). \tag{5}$$

The ratio of the diode to the oxide capacitance appearing in Eq. (5) can be precisely inferred from the $C-V$ characteristics (Fig. 1). With this knowledge, a measurement of ΔQ provides a direct determination of the bound charge σ_b at the GaN surface, and an estimate of the actual strain to within the accuracy of the GaN effective piezoelectric constant.

Figure 4 shows a plot of the measured capacitance change as a function of bias. The strain applied during this sweep was $S_1 = 7.0\times10^{-5}$ corresponding to a calibrated charge of $\Delta Q = 2.5$ pC. The voltage shift is therefore $\Delta V = 0.13$ V. The solid line overlaid on the data in Fig. 4 shows the theoretical dependence of capacitance change on bias expressed in Eq. (4). The derivative of the capacitance with respect to voltage was calculated directly from the empirical $C-V$ profile (Fig. 1). Since all other quantities in Eq. (4) were known, no adjustable parameters could be used to fit the theoretical curve to the data.

Note that the capacitance change, and hence the sensitivity of the device as a strain sensor, is strongly dependent on gate bias. For large positive gate voltages, electrons in the semiconductor accumulate at the oxide interface. When the diode is strained, these electrons will screen the surface bound charge at close proximity with a corresponding slight change in surface potential. In this case, the screening process is accomplished by a redistribution of charge inside the semiconductor, with no net flow of charge to the metal [as predicted by Eq. (5) when $C_d = C_i$]. Since the surface potential changes only slightly, the change in capacitance is small and ultimately vanishes as the diode is biased further into accumulation. For reverse biases, an electrostatic barrier prevents the flow of carriers to the surface. Electrons in the semiconductor can screen the surface bound charge at a distance no closer than the depletion width. As the reverse bias becomes larger, the depletion width widens, and charge begins to flow increasingly to the metal surface in order to screen the piezoelectric charge. Here, the change in Φ_s approaches a maximum, but ΔC drops off because the diode capacitance changes more slowly with surface potential.

Figure 5 shows the measured capacitance change as a function of strain magnitude for a fixed bias voltage of 0 V. The capacitance change seen there is linear in strain up to $S_1 = 10^{-4}$. For larger strains, the deviation from linearity can be inferred by comparing the exact expression for ΔC in Eq. (4) with its first-order approximation. For the device tested here, operating at 0 V bias, the deviation is calculated to be less than 10% for strains up to $S_1 = 1.2\times10^{-3}$. If operated at the bias for maximal capacitance change, the diode would have a linearity better than 99% for strain less than 1.5×10^{-4} and 90% for strain less than 4.5×10^{-4}. The linear range of operation for a strain sensor of this type could be greatly extended by introducing a nonuniform doping profile in the GaN epilayer like that used in hyperabrupt varactor diodes.[14]

B. Device optimization

To judge the sensitivity of GaN capacitive strain sensors, a useful figure of merit is the gauge factor G_F, defined as the fractional change in capacitance per unit strain:

$$G_F = \frac{\Delta C}{C} \times \frac{1}{S_1}. \tag{6}$$

For the device discussed in Sec. III A, the maximum G_F is 151, obtained at a gate voltage of 10 V. By comparison, this value is 1 for ordinary capacitive sensors, and 150 for the best silicon piezoresistive sensors.[15]

For MIS sensors, G_F will depend on the gate bias, the doping density, and the oxide capacitance. To derive the optimal design criteria, the gauge factor can be expressed in terms of these parameters by combining Eqs. (4) and (6):

$$G_F = -e'_{31} \frac{z_i}{\epsilon_i} \left[\frac{\partial \ln C_d}{\partial V}\right]. \tag{7}$$

Using the exact analytic solution for the $C-V$ characteristics,[6] and numerically optimizing Eq. (7) over all variables, the rules for maximal device sensitivity emerge. At a given doping density, the ideal oxide capacitance (C_i) will be:

$$C_i \equiv \epsilon_i / z_i = 0.56 \times \epsilon_s / L_d , \tag{8}$$

where $L_d = \sqrt{\epsilon_s kT/q^2 N_d}$ is the Debye length in the semiconductor. For this C_i, the optimum gate bias is such that the surface potential $\Phi_s = 2.08 \times (kT/q)$, or alternatively, such that the overall diode capacitance is half the oxide capacitance: $C_d = 0.5 \times C_i$.

Under these conditions, the gauge factor for the MIS capacitive sensor will be given by:

$$G_F = \frac{e'_{31} L_d}{\epsilon_s (kT/q)} \times (9.77 \times 10^{-2}). \tag{9}$$

It is apparent from Eq. (9) that G_F scales as the Debye length, and hence as $1/\sqrt{N_d}$. Thus, the device sensitivity will improve as the doping density is reduced. For the doping of the sample used in this experiment, a maximum gauge factor of 385 can be obtained. If we take $N_d = 10^{16}$ cm^3, a conservative estimate for the current lower limit of controllable *n*-type doping of GaN, we project a value as great as 1020, nearly 7 times that of silicon sensors.

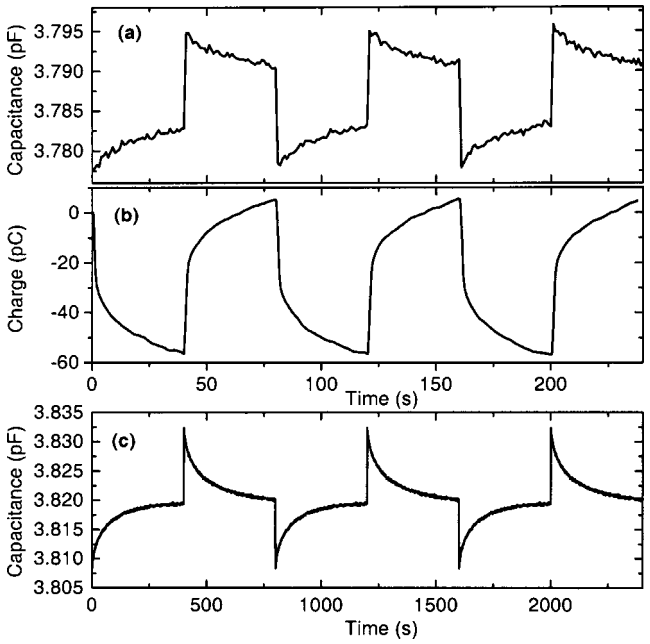

FIG. 6. Typical traces of the (a) capacitance and (b) charge measured on a GaN MIS diode with high interface state density. The time series in (c) represents the capacitance measured on the same device for a much longer (800 s) strain cycle; for clarity, the data shown here were averaged over many cycles.

C. Role of interface states

There are two principal ways in which interface states impair device performance. For one, they can directly cancel the piezoelectric bound charge induced by strain. As a result, the capacitance change (and hence the gauge factor) will be seriously diminished from its ideal value. Perhaps more detrimental is the potentially long time constants for these states to fill and empty in response to strain, leading to a drift in the capacitance until equilibrium is restored.

Both manifestations of surface states are seen quite clearly in Fig. 6. Shown here is the strain response for a GaN MIS diode which was deliberately prepared to have a high density of interface states. This was achieved by exposing the sample to hydrofluoric acid prior to the SiO_2 deposition, thereby removing some of the native passivating oxide on the GaN surface. Furthermore, the oxide was grown thicker, which, for reasons to be discussed shortly, exaggerates the role of the interface states. The effects on the capacitance and charge traces [Figs. 6(a) and 6(b)] are dramatic compared with the same traces for the high quality diode (Fig. 3). When strain is applied to the diode, the capacitance changes but then decays in time toward its original value. During this decay, free charge continues to exchange between the GaN surface and the metal gate. Figure 6(c) shows the capacitance trace of the same diode for a strain cycle with a much longer period. Within 400 s after the initial application of strain, the diode capacitance has returned almost completely to its unstrained value.

The final, steady-state capacitance change, when compared to its initial value, represents a loss in the sensitivity to detect static strain. This reduction of ΔC is directly related to the specific density of interface states D_{ss} at the surface Fermi energy; the decay rate is related to the time constant for emission from these same states. The loss in sensitivity can be quantified by considering the change in surface potential resulting from a small strain in the presence of interface states:

$$\Delta \Phi_s = -e'_{31} S_1 \left(C_i + \epsilon_s \frac{d\dot{\Phi}_s}{d\Phi_s} + q^2 D_{ss} \right)^{-1}, \tag{10}$$

where D_{ss} has units of cm^{-2} eV^{-1}. Note that Eq. (10) applies when equilibrium has been restored long after the initial strain. Because $\Delta \Phi_s$ is reduced when compared to an ideal diode ($D_{ss} = 0$), the capacitance change is smaller as well. Using Eq. (10), and assuming the diode is biased for optimal response ($C_d = 0.5 \times C_i$), the gauge factor with interface states (G_F^{ss}) will be diminished from its ideal value (G_F^{id}) by:

$$G_F^{ss} = \left[1 + \frac{q^2 D_{ss}}{2C_i} \right]^{-1} G_F^{id} . \tag{11}$$

For the sensitivity loss to be small, the specific density at the surface Fermi energy must be small in comparison to the oxide capacitance: $q^2 D_{ss} \ll 2C_i$. Using the optimum oxide capacitance for the doping of our samples, D_{ss} should be much less than 4.1×10^{12} eV^{-1} cm^{-2}. In our case, the measured density for the high quality diodes was more than a factor of ten smaller, leading to less than a 10% reduction of the static gauge factor. If we had matched the lowest reported values to date, $D_{ss} < 5 \times 10^{10}$ eV^{-1} cm^{-2},[10] the reduction would be neglible. For a surface this close to ideal, the sensor could be doped as low as 10^{15} cm^{-3} and would yield a gauge factor in excess of 3200 with less than 10% loss from interface states.

No matter the specific density of interface states, if the diode is designed and biased for an optimal gauge factor $[\Phi_s = 2.08 \times (kT/q)]$, the drift caused by charging of the surface will seem immediate on timescales longer than ~1 ms. This applies for all attainable doping levels of the semiconductor. If drift is deemed intolerable for a particular sensing application, the diode can always be biased deep into depletion (with an associated penalty in G_F). When the surface Fermi energy exceeds 1 eV from the conduction band edge, the time constant for charging surface states becomes so large ($>10^7$ s) that drift would not be practically observable.

IV. CONCLUSIONS

In summary, we have tested GaN MIS diodes for use as piezoelectrically enhanced capacitive strain sensors. The devices exhibit excellent sensitivity to static strain, with a gauge factor of 151 and a linearity better than 99% for strains less than 1.5×10^{-4}. By changing the oxide capacitance and the doping density, sensors of this type could readily achieve gauge factors in excess of 1000. Finally, we developed an objective criterion to weigh the effects of interface states, and show that, for the high quality surfaces attainable in GaN, these states do not limit sensor performance.

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