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Monolithic High-Aspect-Ratio Embedded Parylene Channel Technology: Fabrication, Integration, and Applications

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***Abstract*—This paper presents a novel channel fabrication technology of monolithic bulk-micromachined embedded channels. Based upon implementing two-step complementary dry etching technique and conformal parylene C layer deposition, high-aspect-ratio (internal channel height/internal channel width, greater than 20) polymer channels with uniform quasi-rectangular sidewalls have been successfully fabricated in one silicon wafer. The fabrication is completely compatible with further lithographic CMOS/MEMS process, which enables its total integration with on-chip micro sensors/actuators/structures for lab-on-a-chip applications. An exemplary process has been successfully demonstrated to verify the possibility of combining bulk micromachining and surface micromachining. This proposed formation of channels can be extensively used as beam elements in micromechanical devices or microcolumns for high-performance/high-throughput chip-based separation analysis. A spiral parylene column longer than 1.1 m embedded in a 3.3 mm x 3.3 mm chip has been presented as a prospective element in micro gas-chromatography (μGC).**

Keyword- embedded channel; high-aspect-ratio; monolithic; parylene

I. INTRODUCTION

Micromachined channels/columns have been widely incorporated in microfluidics field in the sense of delivering sample fluids among micro devices for separation/detection or even directly interacting with them by channel wall/fluid contact during delivery. Conventionally, based on target material of channel, microfabrication of on-chip channels can be sorted in two categories: (1) Surface-micromachined channels (Fig. 1.a) [1], in which the process has stripping (long process time) and cleaning (biochemical contamination) concerns of sacrificial materials; (2) Wafer-bonded bulk-micromachined channels (Fig. 1.b) [2], in which the process has challenges of bonding alignment/strength and on-chip integration with other components. Beside the above two fabrication processes, consequently, a buried channel micromachining technology (Fig. 1.c) [3] has been presented to avoid the use of sacrificial materials while remaining its fabrication flexibility. However, the fabricated channels have difficulties to obtain high performance due to their limited geometrical profile. In order to provide a total solution to all the mentioned issues in existing fabricated channels, a novel formation of channels, embedded (one-side buried) channel technology (Fig. 1.d), is therefore proposed in this paper. Its process with versatile designs has been demonstrated and reported [4][5]. Different channel cross-section profiles can be realized accommodate functions including long-channel, high-pressure, or high-flow-rate operations. Using a polymer structural material in silicon micromachining processes, cleaner, more flexible, and more robust microchannels can be implemented to prospective chip-based systems to show their capabilities in microfluidic and lab-on-a-chip devices. Moreover, the fabrication is completely compatible with further lithographic CMOS/MEMS processes, which facilitates integration with other on-chip devices. Specifically in this work, monolithic quasi-rectangular high-aspect-ratio (HAR) embedded channels are fabricated to investigate their capability regarding process integration and applications such as high-performance/high-throughput separation analysis.

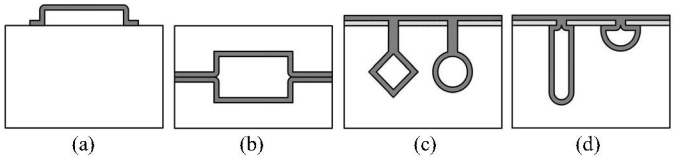

Figure 1. Schematics of channel fabrication technologies: (a) Surface-micromachined channel; (b) Wafer-bonded channel; (c) Buried channel; (d) Embedded channel

II. DESIGN

The design of embedded channels is fairly straightforward. Illustrated in Fig. 2, a thin film layer is first deposited and patterned on substrate to serve as a hard etch mask. At this step the layout of channels is also determined with a small characteristic opening width $2t$. From those exposed regions on surface, HAR trenches or cavities can be created by bulk etching of the substrate. Due to the etching selectivity of materials the etch mask is hardly etched, which results in mask overhang on top of trenches/cavities. Sequentially, by controlling the process of bulk etching, trenches/cavities wider than $2t$ in different geometrical shapes are obtained in order to leave a space beneath substrate surface for embedded channels. Finally, by coating structural material to the substrate in a conformal deposition, the $2t$ opening in between mask overhang is totally sealed when the deposition thickness is greater than t, while embedded channels with thickness t are concurrently formed at trenches/cavities in substrate. These channels are fully enclosed except fluidic access ports in which the exposed opening are originally greater than $2t$. The embedded channels can be micromachined by using a single mask and single device layer deposition. Because of high flexibility given from the fabrication technology, monolithic HAR embedded microchannels can be accomplished and implemented for various device applications.

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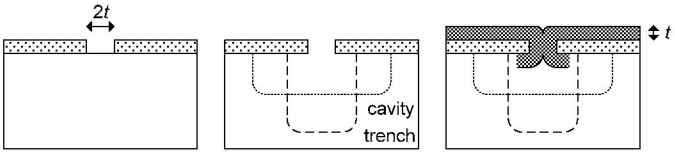

Figure 2. Design of the monolithic embedded channels.

For structural material selection, any material that can be conformally deposited on a substrate is a candidate to construct embedded channels. Parylene C (poly-para-xylylene C) is selected as the structural material on account of its desirable properties such as high mechanical flexibility (Young's modulus ~ 4 GPa), chemical inertness to organic and inorganic solvents, biocompatibility (FDA approved USP Class VI grade), and transparency (small light absorption in the visible region). The coating of parylene features a pinhole-free conformal room-temperature chemical-vapor-deposition (CVD) process, which is completely compatible with other CMOS/MEMS microfabrication technologies and enables final trench/cavity sealing in fabrication of the embedded channels. exploits single-layer-deposited parylene C as a promising polymer material to demonstrate details of the embedded channel fabrication and applications.

III. Fabrication

The embedded channel process begins with 0.5 µm wet oxidation as etch mask on a standard 4-inch silicon wafer. After oxide patterning, the challenge is to create HAR trenches with uniform sidewall undercut underneath overhanging etch mask before depositing a conformal structural layer to form rectangular embedded channels. This step was difficult with conventional process because mass-transport limitation in successive sidewall etching unavoidably leads to a non-ideal "vase-like" undercut profile [6]. As a result, illustrated in Fig. 3, a direct two-step complementary etching technique has been developed. First by controlling time-multiplexed periods of SF_6 etching and C_4F_8 polymerization in Bosch process of deep reactive ion etching (DRIE), reentrant (negative-tapered) trenches are etched with a designated slope. Positive-slope dry etching are then applied to complement the rectangular cross-section profile for the following structural layer deposition.

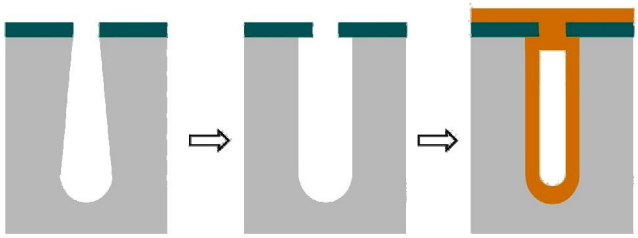

Figure 3. Quasi-rectangular HAR embedded channel fabrication process: (left to right) Reentrant DRIE trench etching; complementary positive-slope dry etching; conformal parylene deposition.

Fig. 4 gives the etching data in the first-step modified Bosch DRIE process. For 6.5 µm openings, 155-µm-deep trenches with 3.5-µm-wide bottom undercut can be created after 200 loops of multiplexed 14-second SF_6 etching (Fig. 5.a) in a PlasmaTherm™ DRIE system. After that the second-step complementary dry etching is applied. In this step SF_6 plasma etching and XeF_2 gaseous etching are selected to perform the dry etching. Results as shown in Fig. 5.b indicate that both etching methods are able to create quasi-rectangular ($90^o \pm 1^o$ sidewall angle) trenches with 2.5 µm oxide overhang. An 8 µm parylene C coating finally seals the trenches to construct embedded channels. Fig. 6 shows the micromachined parylene channel with internal aspect-ratio (internal channel height/internal channel width) around 23. The top close-up image of the channel in Fig. 6 also shows that excessive parylene would deposit only on top of the channels but not on sidewalls after the channels are sealed. This fact greatly reduces complexity of controlling thickness and uniformity of parylene C coating in HAR channel fabrication.

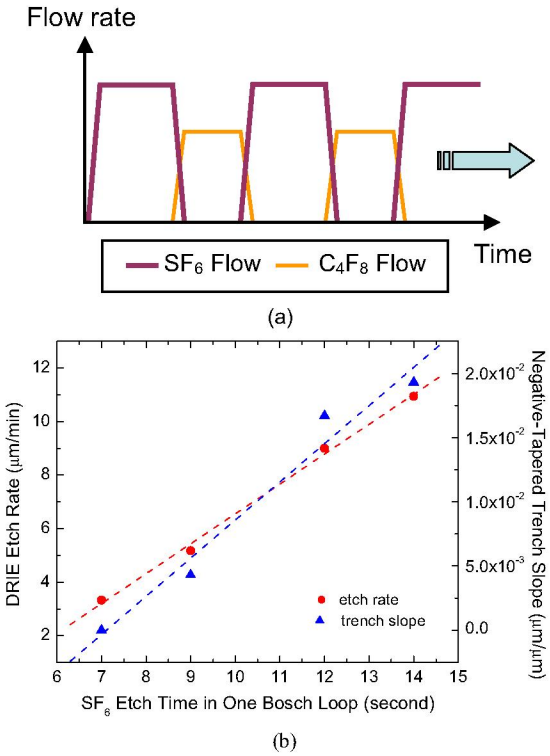

Figure 4. Modified Bosch DRIE process: (a) Time-multiplexed sequence of SF_6 etching and C_4F_8 polymerization in Bosch process. Aggressive trench etching is done by extending time of SF_6 flow; (b) Trench etch rate and etch slope with respect to SF_6 etch time in one modified Bosch loop.

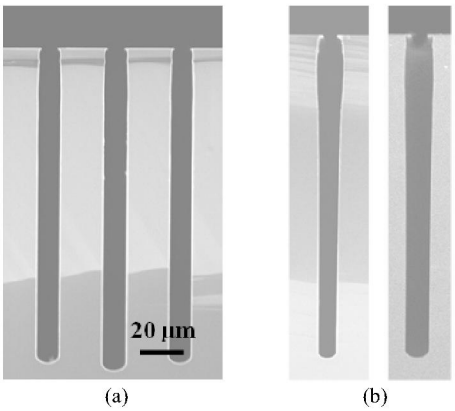

Figure 5. Two-step HAR Trench etching: (a) After reentrant DRIE etching; (b) After complementary dry etching by using SF_6 plasma (left) and gaseous XeF_2 (right). Note the oxide overhang on top of trenches.

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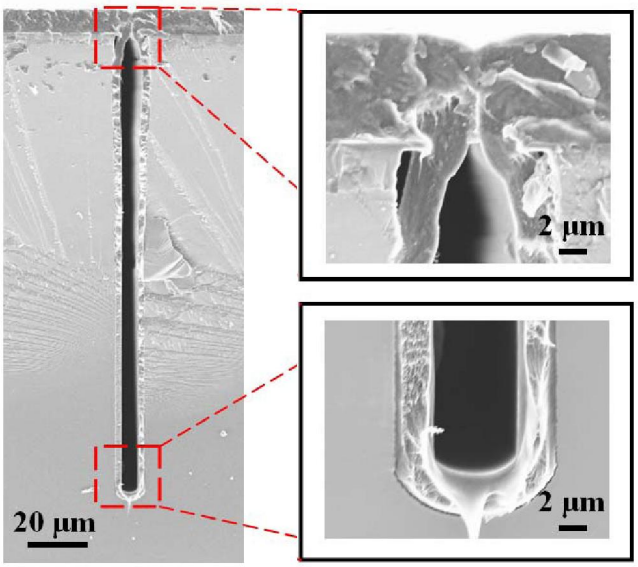

Figure 6. SEM images of fabricated monolithic HAR quasi-rectangular embedded parylene channel (left) and its cut-views (right).

Because of the attribute of conformal parylene C deposition, the wafer surface is highly planarized as the top of channel in Fig. 6 after the embedded channel process. This result guarantees the availability of further lithographic processes on the substrate consisting of embedded channels. With regular surface micromachining techniques, an additional parylene layer can be coated and patterned above the embedded channels to demonstrate the capability of process integration in this fabrication technology. Fig. 7 shows the fabrication result of thin-walled XeF_2 dry-released HAR parylene channels protected by a 10-µm-thick perforated parylene membrane with 20-µm-high gap. As a matter of fact, the parylene membrane was intact even after channel release, which implies the exceptional chemical resistance of parylene C. This example serves as an evidence that the presented channel fabrication technology facilitates on-chip integration with micro/nano sensors/actuators/structures via regular CMOS/MEMS lithographic processes.

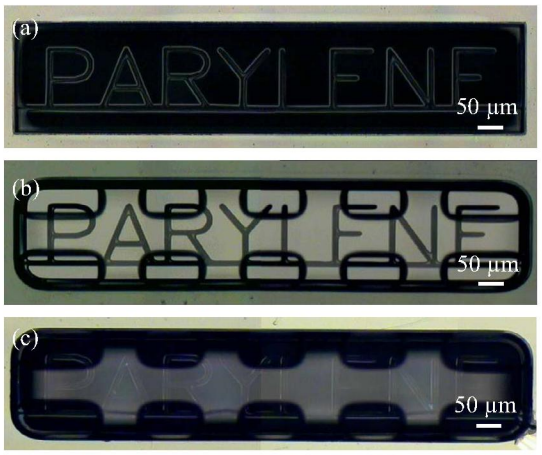

Figure 7. Micrographs of process integration (top-view): (a) Dry-released thin-walled channels; (b) Parylene protective net membrane on top of embedded channels; (c) Image of (b) after dry-release.

IV. Results and Discussion

The fully-dry microfabricated HAR embedded channels can be implemented to various devices. Here two types of examples featuring the channels are presented to demonstrate the capability of channel applications.

A. *Beams as Mechanical Elements*

Micromachined parylene solid beams have been reported previously [7]. Their HAR profile facilitates more flexible structural deformation so that higher mechanical responses can be achieved. Under the same design concept, the proposed embedded parylene channels can act as microbeams after they are dry-released with XeF_2 etching (Fig. 8). Because of the HAR thin-walled hollow profile, their structural rigidity can be much lower than that in general solid beams. Therefore, micromechanical devices featuring these beam structures can realize more compliant and corresponding higher device performance. More favorably, the proposed HAR hollow beams are fabricated with a single layer process so that they have higher reliability (i.e., less fatigue and delamination concerns) than multilayer microfabricated beams.

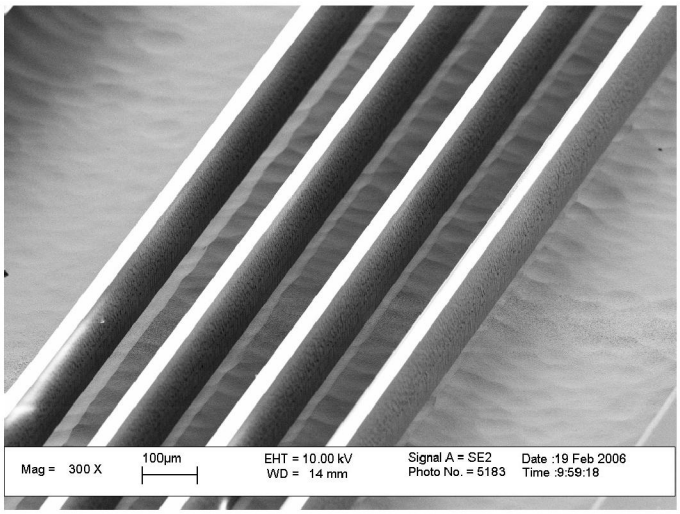

Figure 8. SEM image of suspended HAR hollow parylene beams.

B. *Columns as Fluidic Elements*

The monolithic HAR quasi-rectangular embedded parylene channels are also a breakthrough in terms of their long-column formation as well as their compact planar size. As shown in Fig. 9.a, a spiral parylene column longer than 1.1 m has been successfully fabricated with single-mask in a 3.3 mm x 3.3 mm chip. Its high-density configuration facilitates high-efficiency and high-throughput chip-based separation. As expected, the visible-light transparent property of parylene C provides the columns availability of having optical detection such as fluorescence imaging (Fig. 9.b) for chip-based analysis. The sensitivity of optical detection in this type of channels is greatly enhanced due to in-plane signal accumulation from projected light in vertically HAR channels. In addition, these HAR embedded channels have the advantageous characteristics such as high pressure capacity, low fluidic resistance, and high density (channel length per unit area on a chip). As a result,

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such a embedded parylene column can be incorporated as a prospective element to realize high-performance μGC and other high-throughput separation and analysis.

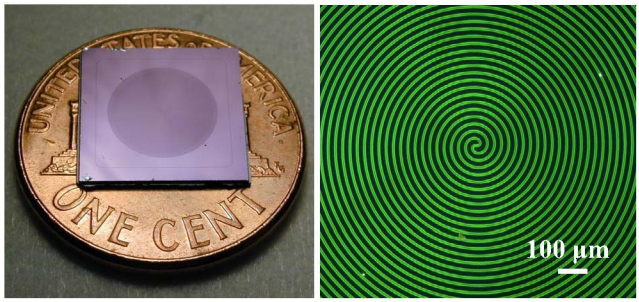

Figure 9. One prospective lab-on-a-chip application by implementing monolithic HAR embedded channels: (a) Chip-sized single-mask spiral parylene column with fluidic access ports sitting on a US penny; (b) Fluorescence image of (a) after dye filling to the transparent parylene column (center close-up of chip).

V. Conclusion

A novel channel fabrication technology has been successfully developed to create monolithic high-aspect-ratio (HAR) embedded (one-side buried) parylene microchannels in silicon substrate. Fully-dry etching techniques and single-layer conformal parylene deposition are employed to construct HAR quasi-rectangular channels with aspect-ratio higher than 20 in single silicon wafer. Various process examples are given to show the feasibility of fabrication and integration of this channel technology. Microstructures featuring the HAR parylene channels can be implemented to different MEMS applications, including HAR hollow beams in micromechanical devices and on-chip HAR columns in high-performance μGC and high-throughput separation and analysis. Currently, the work is focused on researching process control of two-step HAR trench etching, along with fabricating devices consisting of monolithic HAR embedded parylene channels to characterize their performance in microfluidics and lab-on-a-chip systems.

Acknowledgment

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