Ga^+ beam lithography for suspended lateral beams and nanowires

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The authors demonstrate the fabrication of suspended nanowires and doubly clamped beams by using a focused ion beam implanted Ga etch mask followed by an inductively coupled plasma reactive ion etching of silicon. This method will demonstrate how a two-step, completely dry fabrication sequence can be tuned to generate nanomechanical structures on either silicon substrates or silicon on insulator (SOI). This method was used to generate lateral nanowires suspended between 2 μm scaled structures with lengths up to 16 μm and widths down to 40 nm on a silicon substrate. The authors also fabricate 10 μm long doubly clamped beams on SOIs that are 20 nm thick and a minimum of 150 nm wide. *In situ* electrical measurements of the beams demonstrate a reduction of resistivity from $>37.5\ \Omega$ cm down to 0.25 Ω cm. Transmission electron microscopy for quantifying both surface roughness and crystallinity of the suspended nanowires was performed. Finally, a dose array for repeatable fabrication of a desired beam width was also experimentally determined. © *2010 American Vacuum Society.* [DOI: 10.1116/1.3497013]

I. INTRODUCTION

Focused ion beams (FIBs) are typically used as tools to mill silicon from a substrate to create structures that are difficult to otherwise fabricate.[1–3] However, recent research efforts have shown that Ga^+ beam FIBs can also be used as tools for creating an implantation layer that can be utilized as an etch mask for silicon. Some of the first observations noted that this implanted layer was resilient against potassium hydroxide (KOH) wet etching.[4] This etch mask was rapidly extended to various forms of deep reactive ion etching, both for gas-chopping[5] and mixed mode etch chemistries.[6] Although the underlying mechanism behind the masking capability of the implanted Ga to act as an etch mask is still unknown, a potential mechanism is the formation of an involatile gallium-oxygen or gallium-fluorine compound.[7] This implanted Ga etch mask has demonstrated an etch mask selectivity of better than 3000:1 for fluorine based plasma etching chemistry.[6,7]

Using the implanted Ga etch mask patterning technique, structures that typically require extensive fabrication can be dramatically reduced in fabrication complexity. Recent work by Sievilä *et al.*[8] demonstrated that this method of patterning silicon, followed by a wet etch of tetramethylammonium hydroxide to undercut the structures, can produce freestanding cantilevers and beams. Although impressive results were achieved, an alternative to the undercutting method can be achieved by using dry etching. The work presented here demonstrates a method to fabricate suspended nanowires of exceptional length by using a single implantation step and plasma etching—a completely dry fabrication sequence. By first implanting nanoscale patterns, subsequent cryogenic silicon etching can be performed to create nanowires as small as 40 nm in diameter and up to 16 μm in length. As a key feature of this technique, the cryogenic silicon etch was tuned to undercut the implanted Ga mask while maintaining vertical sidewalls on the micron scale. This undercutting permits the nanowire to be completely freed and released from the silicon substrate without requiring a critical point dryer. Further, we report electrical resistivity measurements of doubly clamped suspended beams fabricated using this method and the dependence of beam width on the implanted areal dose. The fabrication sequence demonstrated here offers a rapid and simple method to fabricate nanowires and beams in silicon.

II. FABRICATION

Fabrication of the nanowires and beams requires only two steps, implantation of a Ga etch mask and plasma etching. Implantation of the Ga etch mask was performed with a FEI Dual Beam Nova 200 or 600 Focused Ion Beam system operating at 30 kV. Using SRIM/TRIM simulations (http://www.srim.org),[9] the mean implantation depth was estimated to be approximately 27 nm with a vertical straggle length of 9.5 nm. This implanted region becomes a region of amorphous silicon and interstitial gallium, which is approximately 19 nm thick. At this beam voltage, the Ga^+ beam waist was approximately 16.5 nm. Using automated programs to control deflection of the beam, in a method similar to electron beam lithography, patterning of the silicon was performed. Mask patterning follows that of Henry *et al.*[7] This method of patterning has been demonstrated to achieve pattern sizes down to 30 nm.

Creating suspended lateral nanowires and beams required micron sized posts, 4–10 μm in diameter separated by 10–16 μm, for making electrical contact. Circles were patterned for these structures. For the nanowires and beams, rectangles of various widths connecting the two circles were implanted. The areal dose of the implantation etch mask was controlled by the deflection of a 300 pA beam (measured at

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TABLE I. ICP-RIE etching parameters for the cryogenic etch and silicon substrate.

Etch parameter	Value	Etch parameter	Value
SF_6	70 SCCM	ICP	900 W
O_2	4 SCCM	RIE	10 W
Temperature	−130 °C	Pressure	10 mTorr
dc bias	57 V	He backing	10 Torr

280 pA when blanking the beam) for a specified time. A minimum areal dose of 1.8×10^{16} cm^{-2} has been reported to be required for the implantation to mask any cryogenic silicon etching.[6,7] Increasing the areal dose increases the density of interstitial Ga with the longitudinal straggle remaining approximately constant. This increase in Ga density acts to protect the silicon for longer etch times, thereby increasing the maximum achievable etch depth, represented by a "dose array." The mechanism behind the masking is believed to be the interstitial Ga bonding to either oxygen or fluorine to create a nonvolatile compound.

Plasma etching was performed using an Oxford Instruments PlasmaLab 100 inductively coupled plasma reactive ion etcher (ICP-RIE) 380 system. The etch chemistry utilized was a mixed mode SF_6/O_2 with the etch table held at −130 °C, which is known as the cryogenic silicon etch.[10–12] Under cryogenic conditions, the fluorine and oxygen combine at the surface of the silicon to create a SiO_xF_y passivation layer,[13] typically a few monolayers thick, which protects the etched sidewalls from lateral etching. Under low forward (Fwd) power etching conditions, the fluorine radicals can etch the silicon at rates greater than 1 μm/min, with little milling of the implanted Ga etch mask. For a detailed discussion of cryogenic silicon etching, see Jansen *et al.*[11] Selectivity of this etch mask, defined as the ratio of the etch rate of silicon to the etch rate of the etch mask, has been demonstrated to be higher than 3000:1. Nominal etching conditions for this work are found in Tables I and II.

As a demonstration of this implantation method, 3 μm wide beams were implanted and etched on a silicon substrate. Under etching conditions similar to those for the nanowires, vertical sidewalls that are 10 μm tall were etched. The verticality of the sidewalls indicated that the etching was highly anisotropic with the exception of notching, which occurred directly under the etch mask. This notching was a lateral undercutting of the mask by approximately 1 μm. The low forward power of the cryogenic etch

TABLE II. ICP-RIE etching parameters for the cryogenic etch and SOI substrate.

Etch parameter	Value	Etch parameter	Value
SF_6	70 SCCM	ICP	900 W
O_2	4 SCCM	RIE	3 W
Temperature	−130 °C	Pressure	10 mTorr
dc bias	19–21 V	He back	10 Torr

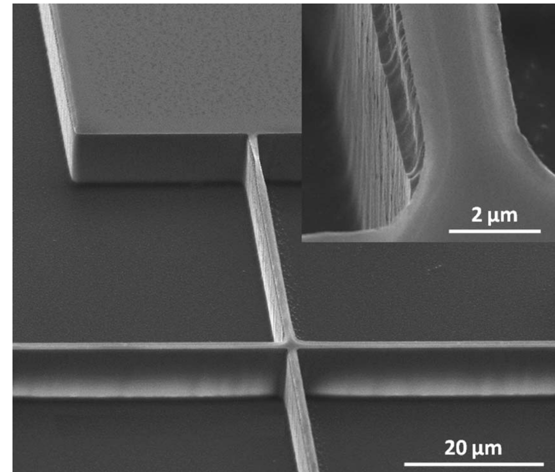

FIG. 1. SEM of silicon cryogenically etched structure using an implanted Ga etch mask. The anisotropically etched structure is 10 μm tall on *N*-type silicon. The inset is a 3 μm wide beam, which is undercut at approximately 1 μm.

resulted in a low dc bias between the plasma and etch table; measured at 21 V for 3 W of Fwd power. We hypothesize that by placing a metalliclike etch mask in this low electric field with thin sidewall passivation, fluorine ions' trajectories are electrostatically modified as they approach the silicon substrate. This effect permits a lateral undercutting of the implanted Ga etch mask on the hundreds of nanometers scale while permitting micron sized structures to be fabricated (Fig. 1). This lateral undercutting is used advantageously here to define and release lateral nanowires from the substrate during the same etch step used to define the micropillars. Although standard fabrication sequences use wet silicon etching to release nanostructures,[14,15] this method permits dry plasma etching to accomplish the same effect.

III. NANOWIRES ON SILICON SUBSTRATES

To fabricate the nanowires and investigate the minimum structure size achievable, the implantation technique was applied to single crystal *n*-type ⟨100⟩ silicon with resistivities of 2–8 Ω cm. The 4 μm diameter micropillars were dosed using a 280 pA Ga^+ beam to achieve an areal dose of approximately 1×10^{17} cm^{-2}. Nine micropillars were patterned to form a circular array, one pillar in the center surrounded by eight pillars. The separation of the pillars from the center pillar was 16 μm in 45° increments. Rectangle widths, beginning at 20–90 nm stepped in 10 nm increments, were then patterned connecting the center pillar with the outer pillars. The implantation times were 100 ms for each 10 nm in width. This set the dose to 1.1×10^{17} cm^{-2} for each nanowire. Upon completion of patterning, the silicon was etched for 3 min under similar conditions described in Table I.

It was observed that once the etch mask became completely undercut, the silicon substrate directly below was rapidly etched away. The resulting structures were a set of suspended nanowires, 16 μm long and approximately 20 nm thick (Fig. 2). Although the 20 and 30 nm structures did not

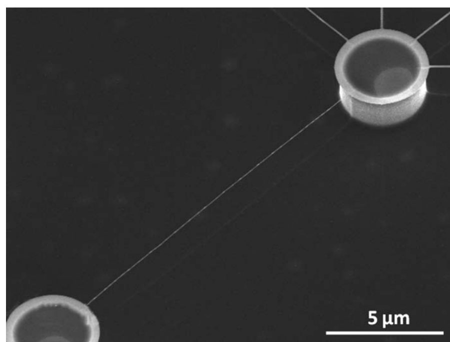

FIG. 2. SEM of a 16 μm long, 40 nm wide, and 20 nm thick silicon nanowire. The nanowire is suspended approximately 3 μm above the substrate using two 4 μm diameter micropillars.

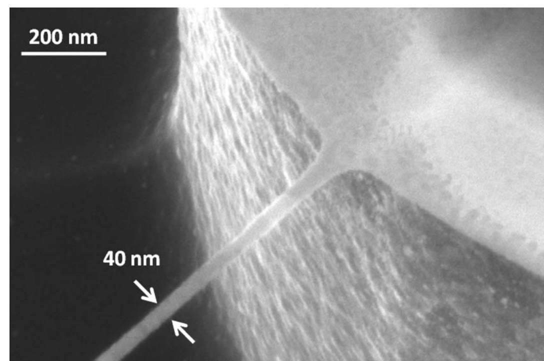

FIG. 4. SEM of a 40 nm diameter nanowire connecting to the 4 μm diameter post; note the visible difference between the implanted Ga etch mask and the silicon substrate. In this image, the single crystal silicon sidewall of the micropillar can be seen as mostly vertical with only a minor undercut.

survive the etching step, the 40–90 nm widths were completely undercut and freestanding (Fig. 3). Figure 4 demonstrates the capability of this patterning method by displaying a 40 nm wide and 16 μm long nanowire. Several observations were made about the nanowires. First is that the structures' edges were round and not square. This is because the Ga^+ beam is approximated as Gaussian and does not terminate sharply at the edges of the rectangle.[3] The second observation was that the nanowires had a localized spotting along the length of the wire. This feature is interpreted as segregations of gallium from the amorphous silicon due to a large local dose of Ga exceeding the solid solubility of silicon.[16]

Finally after the Ga^+ strike the silicon, the crystalline silicon becomes amorphous. Using a TF-20 transmission electron microscope (TEM), the patterned nanowires were tilted in a reflection holder to obtain higher resolution images of the nanowires as well as crystallographic information of their structure. Figure 5 shows a bright field TEM image of a 40 nm wide wire. From this figure we approximate a less than 5 nm surface roughness. To determine the crystalline structure of the nanowire, diffraction patterns were taken of the micropillar and nanowire (Fig. 6). The micropillar clearly displayed a diffraction pattern indicative of a well-defined single crystalline structure, while the halo rings of the nanowire diffraction pattern gave strong evidence that the ion implantation step converts the single crystalline silicon into a nanocrystalline or an amorphous material.

IV. NANOBEAMS ON SOI SUBSTRATES

Although the fabrication using crystalline silicon demonstrated that this technique would be viable for standard silicon processing, it did not permit electrical measurements of only the nanowire. If a two-probe electrical measurement were made using the two contact pillars, the resistance of the nanowire would be in parallel with the resistance of the two micropillars and the substrate; the latter resistance significantly less than the nanowire due to its geometry. In order to only measure the resistance of the nanowire, the structures were fabricated on silicon on insulator (SOI). The top layer of silicon was a 1 μm thick *n*-type single crystal with resistivities of 37.5–62.5 Ω cm, and the buried silicon dioxide layer was 1.5 μm thick. The high starting resistivity permits any measured increase in conductivity to be attributed with the Ga^+ implantation.

Implantation was performed using a 290 pA beam, and the micropillar diameters were set to 10 μm with areal doses of 1.01×10^{17} cm^{-2}. Three sets of pillars were placed in a

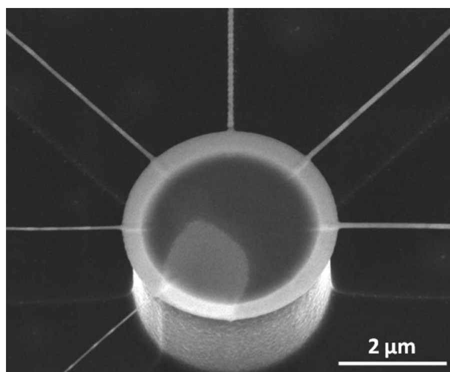

FIG. 3. SEM of the center 4 μm diameter micropillar post. The post serves as a support for the 40, 50, 60, 70, 80, and 90 nm wide silicon nanowires. The wires are 16 μm long.

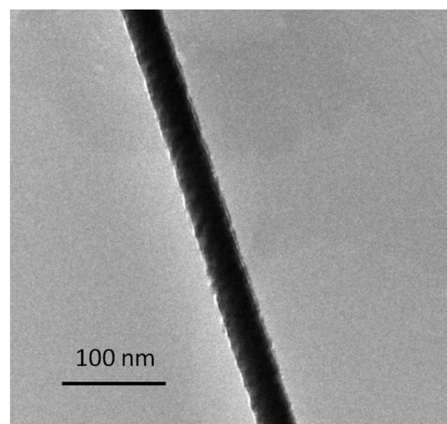

FIG. 5. TEM of a 40 nm diameter nanowire, 16 μm long; the nanowire demonstrates a surface roughness of less than 5 nm.

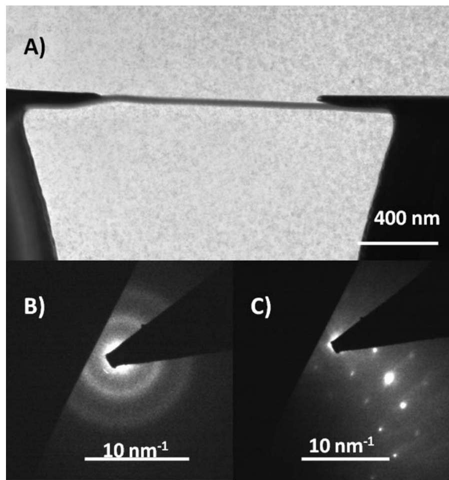

FIG. 6. TEM measurements of a nanowire fabricated on silicon. (A) Bright field TEM of a nanowire suspended between two 4 μm diameter posts; note the undercut of 400 nm below the implanted Ga etch mask. (B) Diffraction pattern of the suspended nanowire interpreted as nanocrystalline consistency. (C) Diffraction pattern of the micron post interpreted as single crystal silicon.

row and separated by 10 μm. The first pattern was a rectangle with a width of 50 nm, the second with a width of 75 nm, and the third with a width of 100 nm. The areal doses for the beams were 1.45×10^{17}, 1.21×10^{17}, and 1.45×10^{17} cm^{-2}, respectively. During the patterning, conductive copper tape was used to electrically contact the top silicon layer with the scanning electron microscopy (SEM) sample holder to prevent charging of the sample and resulting distortion. An 80 s cryogenic etch was then performed under the conditions stated in Table II. It should be noted that the Fwd power, and subsequently the dc bias, was significantly reduced for this etch. The result of this was a widening of the nanobeam. Although the etch mask was expected to widen due to the beam waist and the straggle seen during the implantation, a further widening was from the forward power reducing the critical dose needed to achieve a given etch depth. For these particular structures, the combinations of these effects were to widen the beams to 142, 194, and 252 nm. The nanobeam thickness was estimated to 20 nm based upon the straggle length.

For this experiment, two SOI samples that contained three sets of three beams were fabricated, where each set was identical. Each sample was then mounted in a FEI Quanta SEM equipped with a probe stage, producing images such as those seen in Fig. 7. The arrangement of the probe stage was such that the electron beam could view the sample at an angle of approximately 90°, while two tungsten probe tips made contact with the micropillar tops. The probe tips were connected to an Agilent Semiconductor Parameter Analyzer 4155C for *in situ* two-terminal *I-V* measurements (Fig. 8). Care was taken to ensure that no ground loops between the SEM and the Agilent machine existed, and all measurements were performed with the electron beam blanked and the SEM's infrared light off. Current measurements were made while sweeping voltage from −2 to 2 V for each of the beams. Typical

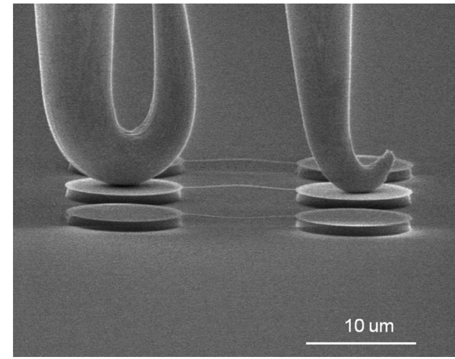

FIG. 7. SEM of a 10 μm, 194 nm wide beam fabricated on SOI being electrically probed in a FEI Quanta SEM using tungsten probes. The electrical *I-V* measurements were performed using an Agilent Semiconductor Parameter Analyzer 4155C.

measured currents from 10 to 60 nA at 1 V biasing. By measuring the exact length and width of the beams and using the approximated 20 nm thickness, resistivities were calculated to be 0.26, 4.38, and 7.48 Ω cm for the 142, 194, and 252 nm beams, respectively. It is interesting to note that this is a reduction in resistivity from ~50 Ω cm to these much lower values. The values quoted here are from one of nine sets of lateral beams measured and represent typical values measured. The nonlinearity observed in the *I-V* curves is assumed to be the effect of a Schottky diode created by contacting the tungsten probe to the silicon. Although further experiments should be made to determine the exact nature of the conductivity, it seems possible that the resistivity is dependent on the areal dosing of Ga and conduction is not through the silicon but the interstitial metal. These results are promising for using the nanowires and nanobeams for making suspended electrical connections.

To establish a higher degree of patterning precision, rows of 50, 100, and 150 nm beams connected to 10 μm diameter posts separated by 10 μm were fabricated with increasing implantation areal doses. The etching conditions are those

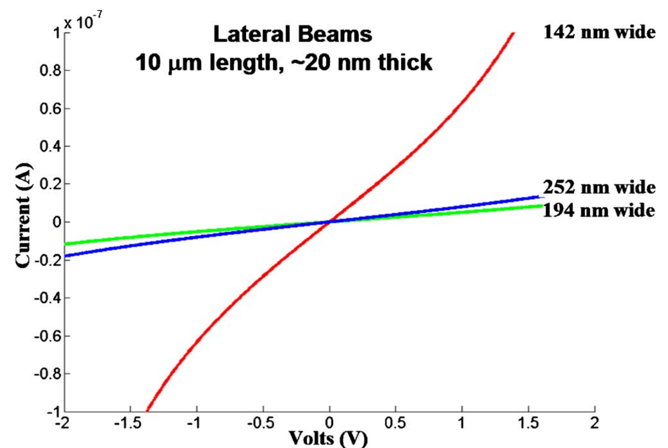

FIG. 8. (Color online) *I-V* measurements of three lateral beams, 10 μm in length, 20 nm thick, with measured beam widths of 142, 194, and 252 nm. Resistivity calculations indicate a decrease in resistivity from 64 Ω cm down to 0.258, 4.38, and 7.48 Ω cm, respectively.

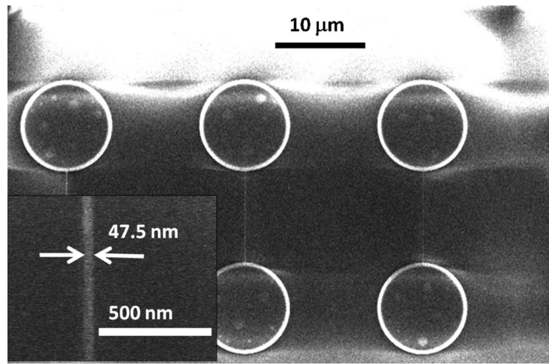

FIG. 9. SEM of three of 12 nanobeams on SOI, 10 μm long beams and 20 nm thick, which were part of the 50 nm dose array. The inset shows a 48 nm beam suspended approximately 1 μm above the buried oxide layer.

reported in Table II. The doses were increased from 1.25×10^{16} to 1.5×10^{17} cm^{-2} in 1.25×10^{16} cm^{-2} increments. It was expected that any areal dose below the 1.8×10^{16} cm^{-2} critical dose values would not mask; this was verified by the observation that the first set of 10 μm posts successfully masked was dosed at 2.5×10^{16} cm^{-2}. Although the 10 μm sized posts were properly masked, the beams were etched away until the dose of 3.76×10^{16} cm^{-2}; the 50 nm beam at this dose value was found to be broken off the posts and resting intact on the oxide layer. SEM images of the first three surviving beams from the 50 nm dose array are seen in Fig. 9. The inset image is the 3.76×10^{16} cm^{-2} dose with a beam width of 47.5 nm. The measured beam width dependence on the implanted dose is seen in Fig. 10. We extrapolate that for each ideal beam width, the measured widths matching the ideal were situated between the 4 and 5×10^{16} cm^{-2} doses. Finally, we note the consistency of beam width for a given dose between the electrically measured devices and the dose array.

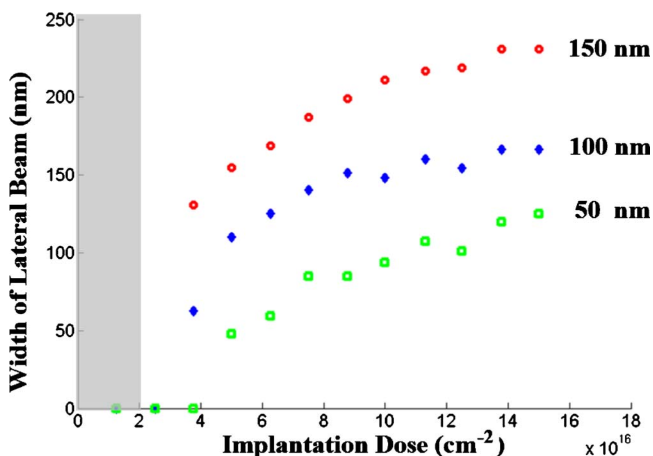

FIG. 10. (Color online) Lateral beam width's dependence on the areal implantation dose for 50, 100, and 150 nm rectangle widths. The shaded area denotes the dose where the implanted Ga dose was below the critical dose required to act as an etch mask. Note that only the micropillar posts survived at the 2.5×10^{16} cm^{-2} dose.

V. CONCLUSION

This work has demonstrated the use of a FIB implanted Ga etch mask for fabrication of lateral nanowires and doubly clamped beams. Using an ICP-RIE cryogenic silicon etch and the demonstrated inherent notching of silicon under the masks, these nanoscale structures were etched and released from the substrate in a single etch step. Nanowires 16 μm long with diameters as small as 40 nm were fabricated and suspended between micron sized posts. TEM images indicated that although the posts remained single crystal, the nanowire were amorphous. Fabricating similar structures on SOI permitted electrical measurements of the nanowires. From the *I-V* curves, a 100-fold reduction of resistivity was calculated. Although the mechanism behind the conductivity improvement is unclear, a possible dependency upon the areal dose was suggested. Further, the implanted dose was seen to modify the beam width, and arrays to precisely fabricate these nanostructures on SOI were experimentally determined. The two-step fabrication sequence described offered a method to pattern, etch, and release suspended nanowires using completely dry fabrication methods.

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