Multiple Phase Generation and Distribution for a Fully-Integrated 24-GHz Phased-Array Receiver in Silicon

Invited Paper

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ABSTRACT — **This paper presents an on-chip multi-phase LO generation and distribution technique used to implement a fully-integrated 24-GHz 8-path phased-array receiver in silicon. Sixteen LO phases are generated by an LC ring oscillator and distributed by a symmetric network to all eight paths. The 8-path array achieves a phase shifting resolution of 22.5° and a total array gain of 61dB.**

Index Terms — **RF receiver, phased-array, wireless communication, beam forming, multiple antenna systems, transmission lines.**

I. INTRODUCTION

Phased arrays are capable of beam forming and electronic steering by adjusting the relative phases of the signal received or transmitted by each antenna. In the past, the high price of discrete microwave modules limited the achievable complexity level of such systems for consumer applications. A low-cost fully-integrated silicon-based phased-array transceiver facilitates widespread commercial applications, such as ultra-high speed wireless communications and vehicular radar.

There is an industrial, scientific, and medical (ISM) band at 24GHz that can also be used for wireless communications. For indoor environments, the delay spread at 24GHz is smaller than that in lower frequency bands (e.g., 2.4GHz and 5GHz bands), allowing higher data rates [1]. Furthermore, an FCC ruling released in 2002 opened the 22GHz ~ 29GHz frequency band for ultra-wideband (UWB) vehicular radar applications [2]. Consequently, research on 24GHz range wireless technologies has accelerated, demonstrating various building blocks and single path receivers at this frequency [1]-[7].

To demonstrate the feasibility of a phased-array system on silicon and explore its advantages, we implemented the first fully-integrated 24GHz phased-array in silicon. The signal path design and performance of the array were presented in [3] and will not be repeated here.

In this paper, we focus on phase generation and distribution techniques as well as LO phase shifting used in the array. Section II covers the system architecture, LO phase shifting issues, and multi phase generation. In Section III, we provide detailed analyses of the phase distribution transmission lines. Measured performance of the 24-GHz phased-array is presented in Section IV.

II. SYSTEM CONSIDERATIONS

When a plane EM wave arrives at an antenna array at an angle α with respect to the normal to the array plane, the signal is received by each antenna at a different time due to the spatial path difference. In general, a constant time delay at the receiver can compensate the arrival delay and effectively focus the beam in a desired direction. In a one-dimensional array, the effective beam angle, α, is related to the delay difference of two adjacent elements, ΔT, the spacing of two adjacent antennas, D, and the speed of light, c, via

$$D.sin(\alpha)=c.\Delta T \quad (1)$$

With ideal delay element following each antenna, the beam forming works independently of the frequency and bandwidth of the signal. Unfortunately, there are practical challenges to implementation of such broadband delay elements in the RF signal path, *e.g.*, signal attenuation, noise, and linearity degradation, as well as signal dispersion. Fortunately, in many practical applications, particularly in wireless communications, the bandwidth of interest is a small fraction of the center frequency, and hence a uniform delay (linear phase) is only required over this narrow bandwidth.

An alternative approach for an integrated implementation of such a system is to perform the phase shifting in the LO path. If different down-converter mixers are driven with different phases, we can achieve the phase shifting at the LO and approximate the delay elements over a limited bandwidth. This architecture is particularly attractive for silicon-based integrated systems due to the large number of transistors available

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and the possibility of accurate multiple phase generation and distribution.

An important question is the impact of phase shifting on signal integrity. Figure 1 shows the simulated eye-diagrams of the received signal (without noise) for an 8-path phased-array receiver at bit rates of 4Gb/s and 8Gb/s at two different incident angles (45° and 90° with respect to normal) using a QPSK binary-coded complex modulation scheme with a carrier frequency of 24GHz. The inter-symbolic interference (ISI) is a function of signal's angle of arrival and the pulse shaping used. In this example, a square-root raised cosine filter with a roll-off factor, β, of 0.5 is used at both transmitter and receiver for pulse shaping. A β of 0.5 corresponds to a spectrum-efficiency of 1.33 bits/s/Hz.

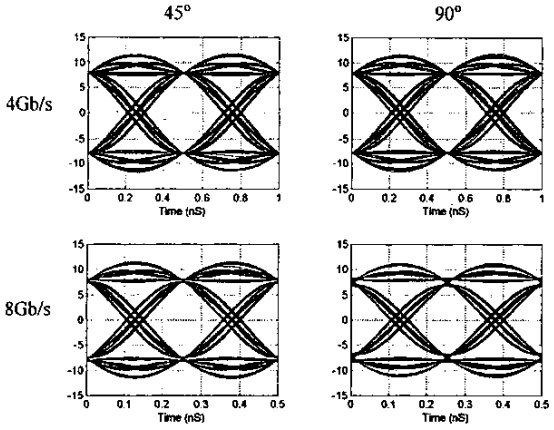

Figure 1: Eye diagrams of received signal

As can be seen from Figure 1, for a carrier of 24GHz, even for bit rates as high as 8Gb/s and an incidence angle of 90° (worst case), the eye remains open and the signal integrity is maintained without additional equalization. This shows the LO phase shifting approach to be a viable solution for wideband wireless communications at 24GHz. Of course, there is a gradual degradation of the eye integrity as the signal bandwidth continues to increase.

Figure 2 shows the top level block diagram of the 24GHz phased-array receiver. In our implementation, the multiple phases necessary for LO phase shifting are generated by an LC ring oscillator. It consists of 8 differential CMOS amplifiers with tuned LC loads connected in a ring, as shown in Figure 3. The VCO operates at 19.2GHz and generates 16 phases with identical interval of 22.5°. The VCO is phase locked to a reference of 75MHz by a third-order integrated frequency synthesizer loop, as shown in Figure 2.

A symmetrical network is used to distribute all 16 LO phases to each receive path, where local phase selectors

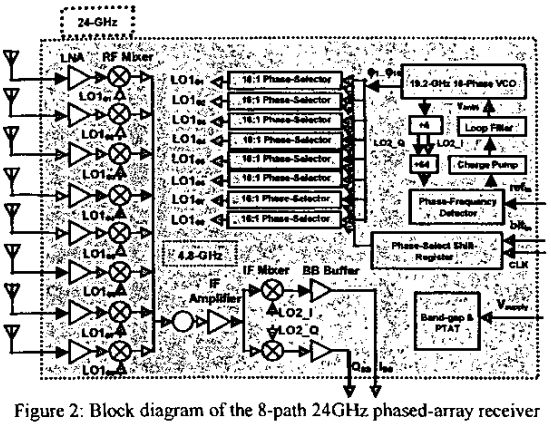

Figure 2: Block diagram of the 8-path 24GHz phased-array receiver

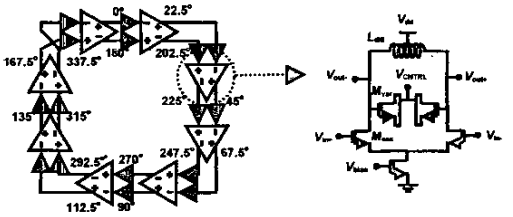

Figure 3: Schematics of the LC ring VCO generating 16 phases

choose the appropriate phase. The phase setting for each path is controlled by on-chip registers programmable through a standard serial interface. The details of the phase distribution network are discussed in the following section.

III. Symmetric Phase Distribution

It is essential that the 16 generated phases of the VCO are fed to each of the 8 phase-selectors in Figure 2 with equal amplitudes and delays. A symmetric binary tree structure, as shown in Figure 4(a), is used to distribute LO phases. Each path consists of 16 metal lines running in parallel, similar to Figure 4(b).

Due to the strong electromagnetic coupling between the closely spaced metal lines, the symmetry not only depends on the path length, but also on the phase arrangement within the bus. Several mechanisms, such as multi-mode excitation, coupling between non-adjacent lines, and boundary discontinuity of a finite array can cause phase and amplitude mismatches in the tree structures of Figure 4(a) and (b). To understand the multi-mode excitation, consider two identical lossless transmission lines T_1 and T_2 running in parallel and driven by two signal sources V_o and $V_o e^{j\theta}$, respectively. If $\theta=0°$ (even-mode excitation), the characteristic impedance of each line is given by,

$$Z_{even} = \sqrt{\frac{l + l_m}{c}} \qquad (2)$$

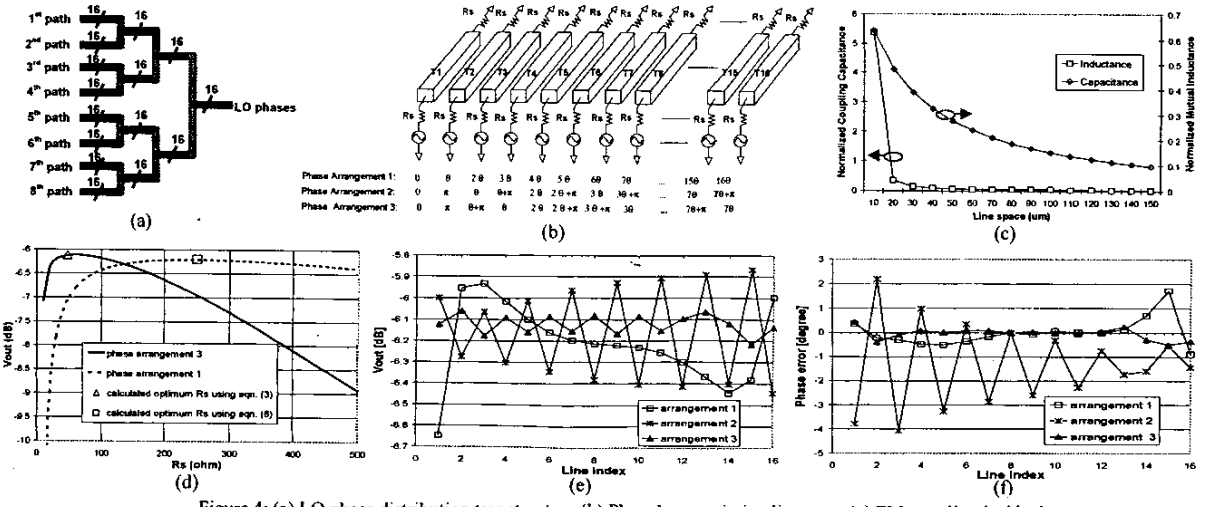

Figure 4: (a) LO phase distribution tree structure (b) Phased transmission line array (c) EM coupling inside the array (d) Vout vs. Rs (e) Amplitude matching (f) Phase matching

where c, l, l_m are per-unit-length capacitance to ground, inductance and mutual inductance, respectively. On the other hand, if $\theta=180^\circ$ (odd-mode excitation), the characteristic impedance of each line is given by

$$Z_{odd} = \sqrt{\frac{l - l_m}{c + 2c_m}} \tag{3}$$

where c_m is the per-unit-length coupling capacitance to the adjacent line. In general, the traveling wave can be considered as a linear combination of even-mode and odd-mode transmissions. Let Z_{o1} and Z_{o2} denote the characteristic impedances of T_1 and T_2, respectively. The magnitude and phase of Z_{o1} and Z_{o2} are related to phase difference θ by

$$|Z_{o1}| = |Z_{o2}| = \frac{\sqrt{2} Z_{even} Z_{odd}}{\sqrt{Z_{odd}^2 (1+\cos\theta) + Z_{even}^2 (1-\cos\theta)}} \tag{4}$$

$$\angle Z_{o1} = -\angle Z_{o2} = \arctan\frac{Z_{even}\sin\theta - Z_{odd}\sin\theta}{Z_{odd}(1+\cos\theta) + Z_{even}(1-\cos\theta)} \tag{5}$$

It can be seen that Z_{o1} and Z_{o2} form a complex conjugate pair, which are equal only for $=0^\circ$ or 180°.

Electromagnetic crosstalk between nonadjacent lines can cause phase and amplitude errors too [8]. EM simulations are performed on an array of 16 on-chip transmission lines, as shown in Figure 4(b). In our design, each line is 4μm thick, 5μm wide, 200μm long, with a 5μm edge-to-edge spacing. These lines are 12um above the silicon substrate. Figure 4(c) shows the extracted mutual inductance and coupling capacitance normalized to the inductance, l, and capacitance, c, respectively. It illustrates that although the capacitive coupling is negligible between nonadjacent lines, the magnetic coupling is significant and the mutual inductance decreases very slowly with the distance.

Figure 4(b) shows three different phase arrangements in a transmission line bus carrying multiple phases. If the array has infinite number of lines, arrangement 1 provides the best symmetry, and the characteristic impedance is expressed as:

$$Z_o = \sqrt{\frac{l + 2\sum_{k=1}^{\infty} l_{mk}\cos k\theta}{c + 2\sum_{k=1}^{\infty} c_{mk}(1-\cos k\theta)}} \tag{6}$$

where l_{mk} and c_{mk} are the mutual inductance and coupling capacitance between two lines with phase difference of $k\theta$. However, in a finite array, the discontinuity at the edge and the inductive crosstalk between nonadjacent lines can produce significant mismatch at the outputs of arrangement 1.

According to Ampere's law, placing differential phase pairs as shown in arrangements 2 and 3 can minimize magnetic coupling. If θ is small, ($\theta=22.5^\circ$ in this work) arrangement 3 has better phase and amplitude matching characteristics than the other two. This is because in 3 the adjacent lines of two different pairs are closer in phase so that the capacitive coupling between them is minimized. For a small θ, the characteristic impedance of the transmission lines in arrangement 3 can be approximated by the odd-mode impedance given by (3).

To compare these three proposed phase arrangements, the results of the EM simulations were employed in Agilent ADS. Each of the three arrays is driven by 16 evenly-spaced phases of a 19.2GHz sinusoid. The transmission lines see a resistance, R_s, at both input and output ports. Figure 4(d) illustrates the voltage at the output port of the central wire as a function of R_s. It verifies that using resistance values estimated by (6) and

(3) results in maximum V_{out} for arrangements 1 and 3, respectively. Figures 4(e) and (f) shows the magnitudes and phases of the voltages at the 16 output ports for 3 arrangements, it can be seen that arrangement 3 exhibits less mismatch, hence is adopted in our 24GHz phased array receiver.

IV. Measurement

The phased-array receiver is implemented in IBM 7HP SiGe BICMOS process with an HBT f_T of 120GHz and 0.18-μm CMOS transistor[10]. The die micrograph of the chip is shown in Figure 5. The chip occupies an area of 3.3 x 3.5 mm^2.

Table 1 summarizes the measurement results. To assess the array performance, an artificial wave front is generated by feeding the RF inputs of each receiver path via power-splitters and adjustable phase-shifters. This way the effects of antenna are separated from the receiver array performance. Figure 6 shows the normalized array gain as a function of signal incident angle at three different LO-phase settings for four-path operation. It clearly demonstrates the programmable spatial selectivity of the phased-array receiver, and more than a 20dB peak-to-null ratio which verifies the symmetric distribution of the LO phases.

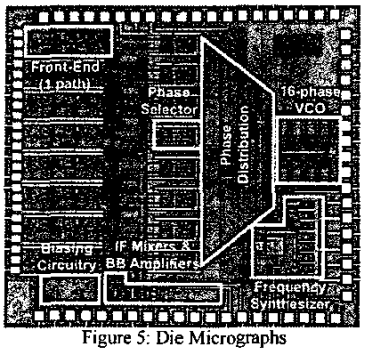

Figure 5: Die Micrographs

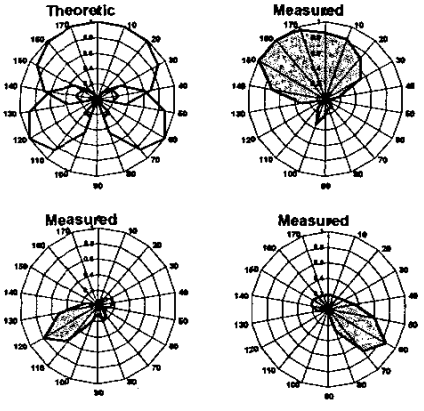

Figure 6: Measured pattern of a 4-path array at three different LO phase settings compared to the theoretical predictions (ideal case)

Table 1: Summary of the measured performance

Signal Path Performance (per path)	
Peak Gain	43dB
Noise-Figure	8.0dB
Input-Referred 1dB Compression Point	-27dBm
Input-Referred 3rd-Order Intercept Point	-11.5dBm (2 tones 5MHz apart)
On-chip Image Rejection	35dB
Current Consumption [*RF (each path) / IF*]	12mA / 12mA
S11	< -10dB
LO Path Performance	
Synthesizer locking range	2GHz (10%)
Synthesizer bandwidth	7MHz
VCO phase noise	-103dBc/Hz @ 1MHz offset
Current Consumption (VCO + buffers)	59mA
Complete Receiver Performance (8 paths)	
Total Array Gain	61dB
SNR Improvement	9dB
Phase-shifting Resolution	22.5°
Beam-forming Peak-to-Null Ratio	20dB (measured for 4 paths)
Power Dissipation @ 2.5V	364mA 287mA (w/o biasing and baseband buffers)
Technology	SiGe, 120GHz HBT, 0.18μm CMOS
Die Area	3.5mm x 3.3mm

II. Conclusion

An 8-path phased-array receiver with 22.5° beam-forming resolution is demonstrated. The LO-path phase shifting is realized through using ring VCO, symmetric phase distribution network and phase selectors.

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