SCALABLE FLEXIBLE CHIP-LEVEL PARYLENE PACKAGE FOR HIGH LEAD COUNT RETINAL PROSTHESES

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ABSTRACT

We present an innovative technology for the fabrication of a biocompatible parylene-based high lead count retinal prosthesis in which a prefabricated stand-alone application-specific integrated circuit (ASIC) is placed directly into the fabrication process of the other system components. The package is fabricated in such a way that the ASIC-to-electrode interconnects are patterned using standard photolithography. The density of interconnects is fully scalable to the limits of lithography. This packaging scheme also enables the simultaneous integration and interconnection of discrete components such as chip capacitors with the rest of the system. Electrical test results verify the efficacy of this cost-effective and high-yield packaging scheme, and pave the way for a monolithic implantable parylene-based intraocular system.

Keywords: BioMEMS, Neural prosthesis, Packaging, Parylene, Retinal prosthesis

INTRODUCTION

This work solves the current lack of a cost-effective, high-yield method for interconnecting foundry-fabricated driver circuitry with a radio-frequency (RF) coil and retinal stimulator. Electrical epiretinal prostheses that enable high-resolution vision require a high-density stimulating electrode array to be placed in close proximity to the remaining functional neurons of the macula. Interconnection of the flexible electrode array with an application-specific integrated circuit (ASIC) in a high lead count package remains a significant challenge to breaking the current resolution barrier. Driven by reports of parylene's biocompatibility [1-3] and its USP Class VI status, we are developing a monolithic parylene-based intraocular system comprising a power/data RF coil, a packaged analog/digital driving ASIC, and a retinal multielectrode array consisting of approximately 1000 electrodes (Fig. 1), for the treatment of age-related blindness [4]. To this end, we have specifically tested parylene C for its intraocular biocompatibility, and we have invented a new chip-level integrated interconnect (CL-I^2) packaging technology for integrating individual prefabricated chips into a flexible parylene electrode "skin" with high-density electrical interconnects limited in number only by photolithography. This technology is critical to the development of the retinal prosthesis because it enables integration of ASICs and discrete components with the retinal stimulator and RF coil and provides for high lead count interconnects. Parylene is ideal for this application because its strength and flexibility (Young's modulus ~4 GPa) will facilitate surgical implantation and enable the electrode array to match the retina's curved contour in the final implementation of the system.

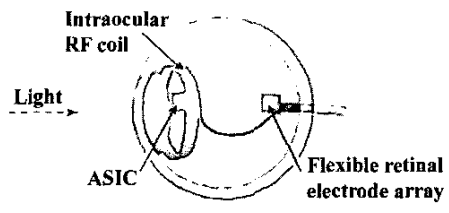

Fig. 1. Intraocular retinal prosthesis components and locations in the eye.

PARYLENE BIOCOMPATIBILITY STUDY

In order to assess the intraocular biocompatibility of the material, an approximately 2 cm × 0.5 cm piece of unmodified 20 μm-thick parylene C was implanted in the vitreous cavity of the right eyes of two rabbits for six months. The retinas of the right eyes of both rabbits were compared post-mortem with those of their left eyes that served as controls. Histological evaluation (example given in Fig. 2) reveals no discernable difference between right and left eyes, indicating that there was no detectable adverse immune response affecting the retina due to parylene implantation. These results indicate that parylene C is a biocompatible bulk material for an intraocular retinal prosthesis, and clear the way for the

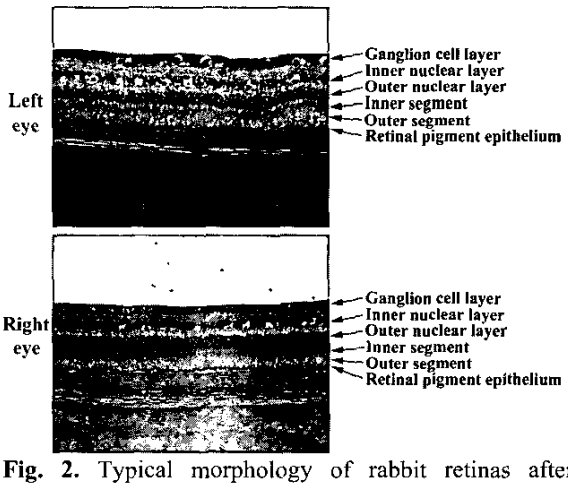

Fig. 2. Typical morphology of rabbit retinas after parylene C implantation in the right eye for six months (Left eye: control, Right eye: experiment).

design and fabrication of a flexible packaging system using parylene C as the primary substrate.

FABRICATION

Chips simulating MOSIS-fabricated ASICs were manufactured and used to demonstrate our new packaging technology in order to simplify testing and spare the real chips for future use. Three MOSIS chips used in a previous model of the retinal prosthesis were used as a model for these chips. The MOSIS chips were imaged using a WYKO interferometer, and were found to have mean dimensions of 2.500 mm in length, 2.617 mm in width, and 254.2 μm in total thickness. 100 Å of chrome and 2000 Å of gold were deposited on a 260 μm-thick silicon wafer. Using a photoresist mask, the metal was wet-etched to pattern pads of the same size and in the same locations as on the MOSIS-fabricated chips (approximately 70–100 × 100 μm^2 with a center-to-center pad spacing of approximately 200 μm), as well as a pattern of short-circuits connecting these pads to nearby pads. After stripping the photoresist, a second photoresist layer was spun on the wafer and patterned as a mask for a Bosch through-wafer etch in a PlasmaTherm deep reactive ion etching (DRIE) system. This etch defined the length, width, and thickness of the simulated chips as 2.49 mm, 2.61 mm, and 260 μm, respectively. Finally, the photoresist mask was removed from the individual chips. In this manner, chips comprising simple electrical shorts and intrinsic resistors were fabricated as our CL-I^2 package test structures (Fig. 3).

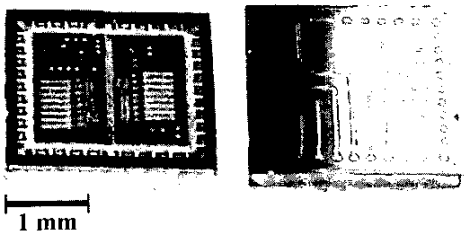

Fig. 3. MOSIS ASIC (left) next to test chip (right).

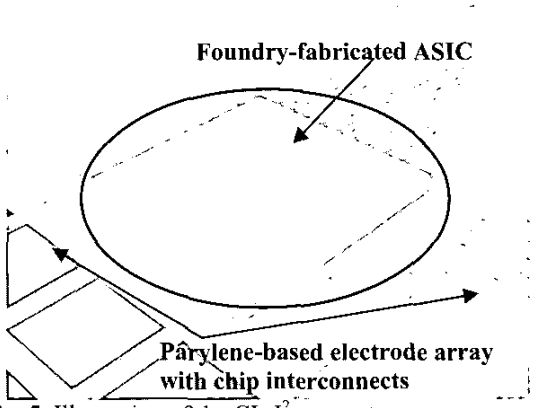

Fig. 5. Illustration of the CL-I^2 concept.

The only properties of our prefabricated chips that had to be known before incorporation in the CL-I^2 process were their overall length, width, and thickness, and the dimensions and locations of the contact pads. Fig. 4 gives a detailed CL-I^2 process flow and Fig. 5 provides an overhead depiction of the fabricated package. To begin the process, shallow alignment marks are etched into a standard 550 μm-thick silicon wafer using a thin photoresist mask and an SF_6 plasma. After stripping the photoresist, thick photoresist is spun on the wafer and 2.51 × 2.63 mm^2 holes are then patterned after alignment in a 10X reduction stepper. The through-holes are etched using the Bosch process. After photoresist removal, Nitto tape is placed on the frontside of the wafer. The chips are then self-aligned in the holes by inserting them from the backside (the Nitto tape enables frontside planarization), and they are mechanically sealed in place using several drops of sacrificial photoresist to fill the gaps around the chip, and a parylene C deposition (~12 μm). After removal of the Nitto tape, small vertical displacements of the chips are verified using a profilometer.

Fabrication of the electrodes, or, in this implementation, testing contact pads, is then performed on this wafer as if it were a whole wafer with prefabricated integrated circuitry. First, a photoresist sacrificial layer is spun on the wafer and patterned to expose the chip's surface. After baking to remove

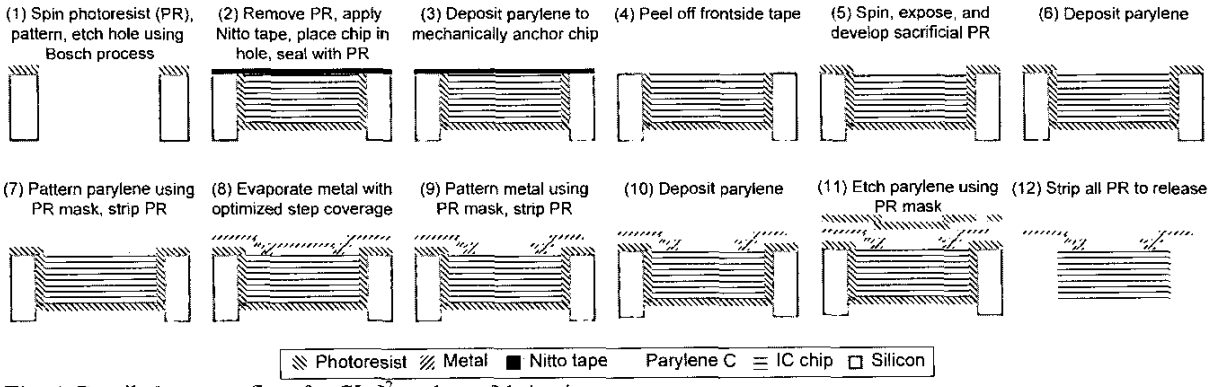

Fig. 4. Detailed process flow for CL-I^2 package fabrication.

excess solvent, approximately 3 μm of parylene C is deposited on the entire wafer. Photoresist is spun on the wafer, exposed in the 10X reduction stepper, and developed to pattern etch holes above the on-chip pads. This pattern is transferred into the parylene using an O_2 plasma in an RIE system, exposing the metal of these on-chip pads. 200 Å of titanium and 2000 Å of gold are deposited in a CHA SE600 RAP e-beam evaporation system using optimized step coverage, and patterned (using a photoresist mask and wet-etching) to define the remote contact pads and remote pad to on-chip pad interconnects. The top photoresist is stripped, and a second layer of approximately 10 μm of parylene C is deposited and patterned as before, but this time to open the remote pads/electrodes to enable electrical testing. Finally, all photoresist, including the sacrificial layer, is removed by soaking the wafer in acetone, releasing a flexible parylene skin with embedded interconnects to the packaged ASIC. It is important to note that the ASIC can be of any thickness generally less than that of the host wafer, and it can have parylene or any other coating deposited on it *a priori* to increase hermeticity, provided that the chip contacts are opened before the interconnect metal is laid down and patterned (Fig. 4, steps 8 and 9).

RESULTS AND DISCUSSION

Minimizing vertical displacement of the ASIC from the wafer surface is crucial for further successful photoresist spins and photolithography, and Fig. 6 shows that for most chips, this vertical displacement was less than 6 μm. Fabrication on the somewhat anomalous Chip 2, however, was also successful. The accurate horizontal alignment of the perimeter interconnects to the embedded chip is shown in Fig. 7. As designed, the chips are self-aligned to within 10 μm of lateral displacement. The embedded chip with remote contact pads is shown in Fig. 8(a), and Fig. 8(b) depicts the flexibility of this package. The electrical resistance values between remote pads connected to the on-chip pads in a quadrant of the chip (Table 1) are those expected: the electrical nature of the connection between

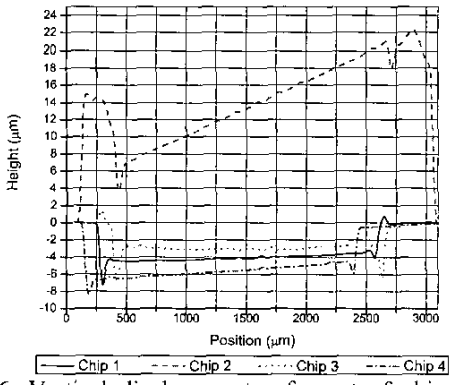

Fig. 6. Vertical displacements of a set of chips after mechanical sealing in the wafer (Fig. 4, step 4), where the top surface of the wafer corresponds to 0 μm.

pads 1 and 8, 2 and 7, 3 and 6, and 4 and 5 is a short with an average resistance of ~59.7 Ω, whereas, for example, shorted pads 3 and 6 show approximately the same intrinsic through-die resistance to pad 4. The measured I-V curve for the short (e.g. remote pad 3 across ASIC to remote pad 6) showed ohmic contact (Fig. 9(a)),

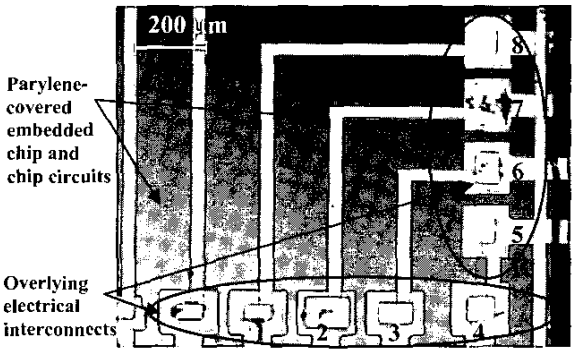

Fig. 7. Embedded chip with fabricated perimeter interconnects (numbered traces connect to numbered remote pads shown in Fig. 8(a)).

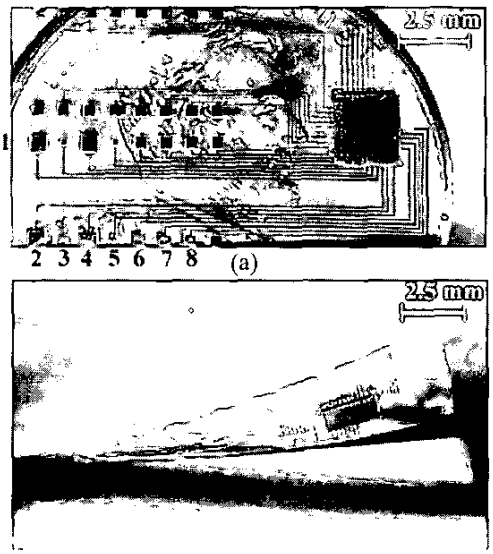

Fig. 8. (a) CL-I^2 packaged chip shown resting on a penny (numbered pads used to generate to Table 1), (b) Demonstrates flexibility of CL-I^2 package.

Table 1. Resistance in Ω between remote pads connected to the embedded chip (arrows indicate shorted pairs)

Pad	1	2	3	4	5	6	7	8
1		323000	327000	330000	327000	325000	322000	61.0
2	323000		577000	448000	441000	580000	60.9	325000
3	327000	577000		599000	582000	59.9	454000	319000
4	330000	448000	599000		57.1	587000	499000	319000
5	327000	441000	582000	57.1		569000	490000	320000
6	325000	580000	59.9	587000	569000		478000	321000
7	322000	60.9	454000	499000	490000	478000		316000
8	61.0	325000	319000	319000	320000	321000	316000	

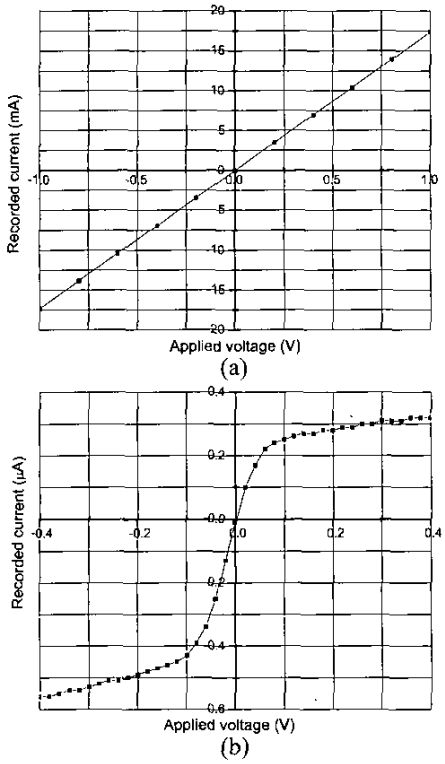

Fig. 9. Measured I-V curves for (a) short and (b) intrinsic circuit.

whereas for the intrinsic circuit (e.g. remote pad 3 through highly-doped intrinsic resistor to remote pad 4) it showed the expected Schottky effect (Fig. 9(b)).

It should be stressed that the lead count and interconnect density limitations for this technology stem only from the limitations of the microfabrication and photolithography equipment used to fabricate the CL-I^2 package, and, in particular, to pattern the first parylene etch (Fig. 4, step 7). All interconnects to the chip are fabricated simultaneously during the metal deposition step, and depend on optimal step coverage of the parylene sidewall (aided in part by the slightly isotropic nature of the O_2 plasma etch of parylene [5]). The CL-I^2 process thus avoids the use of tedious and comparatively low-density ball-wedge [6] or wire bonding.

Our method of incorporating discrete modules into a microelectromechanical systems (MEMS) process is far more cost-effective when compared with full-wafer IC processing and MEMS integration [7], because valuable space on the wafer is not wasted during the IC fabrication step. Furthermore, in comparison to other ASIC integration attempts [8], this packaging scheme is superior for biodevices because it takes advantage of parylene's low water-absorption [9] and highly-conformal pinhole-free deposition, and because the package is both flexible and biocompatible. Among the feasible uses for this technology is the interconnection of chips and discrete components, such as chip capacitors, fabricated using different materials and processes, to make large conglomerate circuits for neural prostheses and for other applications.

CONCLUSION

For the first time, the direct integration of individual prefabricated ASICs with CMOS compatible MEMS in a flexible, scalable, standard photolithography- and standard microfabrication-limited manner has been shown. This scalability means that our technology is capable of achieving the high lead counts required for neural prostheses. With the intraocular biocompatibility of parylene C now proven, this CL-I^2 package is particularly well-suited for retinal prostheses. Thus, we have presented an innovative, high lead count, biocompatible, and cost-effective technology for interconnecting ASICs with each other, and with retinal prostheses.

Acknowledgments

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