A Phase Diagram of Low Temperature Epitaxial Silicon Grown by Hot-wire Chemical Vapor Deposition for Photovoltaic Devices

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ABSTRACT

We have investigated the low-temperature epitaxial growth of thin silicon films by hot-wire chemical vapor deposition (HWCVD). Using reflection high energy electron diffraction (RHEED) and transmission electron microscopy (TEM), we have found conditions for epitaxial growth at low temperatures achieving twinned epitaxial growth up to 6.8 μm on Si(100) substrates at a substrate temperature of 230°C. This opens the possibility of growing high quality films on low cost substrates. The H_2:SiH_4 dilution ratio was set to 50:1 for all growths. Consistent with previous results, the epitaxial thickness is found to decrease with an increase in the substrate temperature.

INTRODUCTION

HWCVD epitaxial growth on large-grained templates is one strategy for the fast, low-temperature growth of large-grained films with hydrogen-passivated low-angle grain boundaries. We propose a structure in which a polycrystalline silicon template with grain sizes on the order of ten microns is fabricated on glass coated with a transparent, conductive oxide (TCO), by a solid-phase crystallization process called selective nucleation solid phase epitaxy (SNSPE) [1]. The template layer is designed to serve as the n+ layer of the device, and as the epitaxial template for n and p+ layers grown by HWCVD, using phosphine and tri-methyl boron as dopants (Fig. 1).

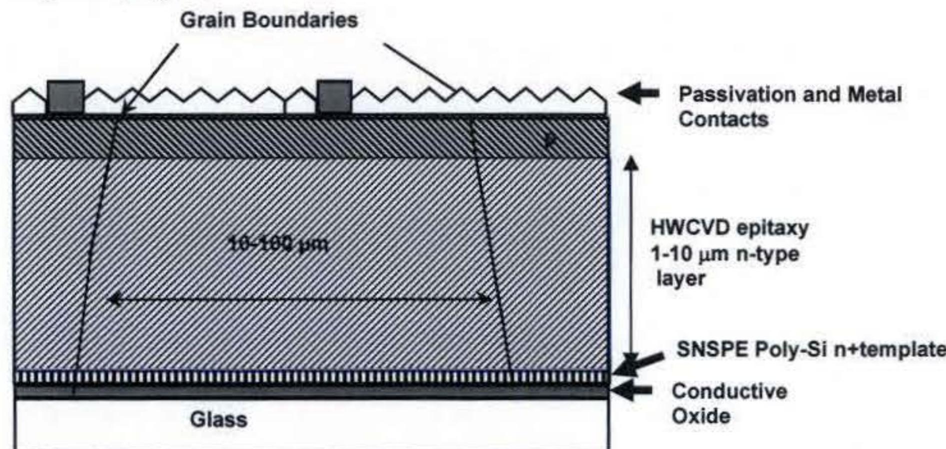

Figure 1: Schematic of proposed photovoltaic device incorporating epitaxial Si growth on a large-grained polycrystalline template fabricated by SNSPE.

Previously we have shown successful epitaxial growth in several orientations on large grained polycrystalline substrates at 300°C [2]. Although these films were only 1 μm twinned epitaxy and then broke down into polycrystalline silicon, they exhibited several-microsecond minority carrier lifetimes [3,4]. This suggests that HWCVD at low temperatures allows hydrogen to effectively passivate the grain boundaries in these films. Although nickel is known to degrade minority carrier lifetimes, even in small concentrations [5], the lifetimes of films on SNSPE large-grained templates are comparable to the lifetimes of films on Si(100). Under low light injection (LLI) conditions, the minority carrier lifetimes for films on Si(100) range from 5.7 to 7.5 μs, and the minority carrier lifetimes for films on SNSPE templates range from 5.9 to 19.3 μs as measured by resonantly coupled photo-conductive decay (RCPCD)[6].

Polycrystalline films grown by HWCVD have been used elsewhere in the fabrication of 1.5 μm-thick thin-film transistors with measured channel mobilities of 4.7 $cm^2/V\cdot s$ on glass substrates [7]. Using the Einstein relation [8],we can determine that, for comparable mobilities, the minority carrier diffusion coefficient in our films would be 0.1 cm^2/s. From this value and the minority carrier lifetime of ~ 7 μs, the minority carrier diffusion length would be approximately 9 μm, which is comparable to the thicknesses of the active layers for commercial thin-film photovoltaics [9]. The minority carrier lifetimes of films on SNSPE templates are comparable, making it possible that the growth of epitaxial films by HWCVD on large-grained SNSPE templates is a viable strategy for the fabrication of thin-film photovoltaics.

EXPERIMENTAL DETAILS

Epitaxial silicon thin films were grown on Si(100) substrates. In order to promote crystalline growth, we used a high hydrogen-to-silane flow ratio of 50:1, using a mixture of 1% SiH_4 in He. Total pressure ranged from 75 to 120 mTorr. Two tungsten wires with diameters of 0.5 mm were positioned between 3.5 and 4.2 cm from the substrate for a growth rate of ~1Å/s. In order to avoid contamination of our films from the stainless steel components of our wire assembly, we used much lower wire temperatures than what is normally seen in HWCVD. The wire temperature was set to 1350-1500°C, as measured by optical pyrometry, and substrate temperatures ranged from 230°C to 350°C. Before growth, substrates were placed in a UV-ozone cleaning system for 10 minutes, and then briefly immersed in HF. Once in the chamber, the substrates were brought up to the growth temperature and left for 30 minutes to remove any residual hydrocarbons. The substrate temperature was calibrated with a SensArray thermocouple wafer under vacuum, with the wires set at the growth temperature. Films with thicknesses in the range 100 nm to 7 μm were grown.

DISCUSSION

We found that the information about the microstructure at the sample surface provided by RHEED correlated well with the microstructure observed by TEM, allowing us to rely primarily on RHEED for analysis of film microstructure, eliminating the need for tedious sample preparation and analysis as required in TEM [[3,4]]. Figure 2 shows the RHEED pattern of two films of different crystalline morphology. The 1.3 μm thick film [Fig. 2(c)] is (100), but the 1.8 μm thick film [Fig. 2(d)] shows double diffraction spots of high intensity indicating twinned

growth and roughening along with a diffuse ring pattern consistent with a transition to polycrystalline growth. Atomic force microscopy (AFM) scans [Figs. 2(a) and (b)] show an increase in the rms roughness between the 1.3 μm and 1.8 μm thick films from 81 nm to 114 nm, as well as a decrease in the average feature size from 1.5 μm to 900 nm, consistent with the breakdown of epitaxial growth to twinned epitaxial growth and subsequently polycrystalline growth[10].

Figure 2. a) AFM image of 1.3μm thick epitaxial Si film. b) AFM image of 1.8μm thick poly/twinned film. c) RHEED pattern of epitaxial film shown in (a). d) RHEED pattern of mixed poly/twinned film shown in (b).

RHEED was used to characterize the crystallinity of 100 nm to 7 μm thick films, grown at 50:1 hydrogen dilution and temperatures between 230°C and 350°C. A completely defect-free epitaxial phase was observable by RHEED for film thicknesses at and below 1.5 μm, while twinned epitaxial and mixed polycrystalline phases were observed for film thicknesses above 1.1 μm (Fig. 3). We observe a general trend toward higher critical epitaxial thickness at lower substrate temperatures. We believe that the decrease in epitaxial thickness as substrate temperature increased is due to an interplay between surface hydrogenation at low temperatures and surface oxidation at high temperatures that reduces the epitaxial thickness. This is possibly related to the higher hydrogen content in HWCVD as compared to PECVD or MBE along with oxygen contamination in the deposition chamber [2,11].

Figure 3 also suggests that a greater substrate to wire spacing contributes to higher quality film growth. This could be due to the decrease in deposition rate as the substrate moves further away from the wires. The use of diluted silane also contributes towards this end due to the lower partial pressure in the chamber. The deposition rate is not the only factor in achieving a high quality film, but it does appear to be the most influential. Deposition rates in this study vary from a film average of 0.9 nm/min to 4.5 nm/min. Detailed TEM analysis is needed to determine the actual deposition rate for the various phases.

The thickest twinned epitaxial layer of 6.8 μm was seen at a substrate temperature of 230°C. At this temperature very low cost materials may be considered as potential substrate materials. The softening points of many inexpensive polymeric and glass materials (soda lime glass, 550°C; borosilicate glass, 500°C; polyimide, 320°C; polyetheretherketone, 250°C) lie above our process temperature.

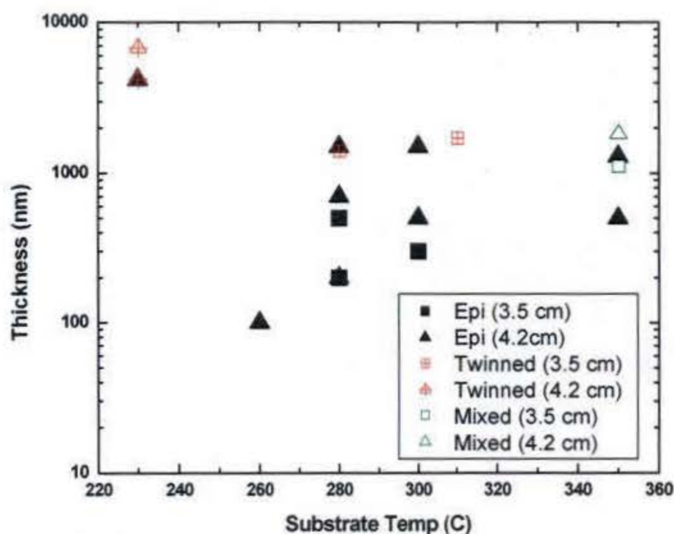

Figure 3. Phase diagram of Si epitaxial growth on a Si(100) substrate for 1% SiH_4 in He with H_2:SiH_4 dilution ratio set to 50:1, for substrate-wire separations of 3.5 cm and 4.2 cm. Total pressure ranges from 75 to 120 mTorr.

.CONCLUSIONS

We have previously shown that high quality epitaxial thickening of large-grained templates is a promising structure for future thin film silicon photovoltaic devices. We are now able to achieve even greater epitaxial thicknesses at lower temperatures, with 6.8 μm of twinned epitaxy at a substrate temperature of 230°C, and a H_2:SiH_4 dilution ratio of 50:1. At these low temperatures new substrates such as polymers become feasible.

ACKNOLEDGEMENTS

The authors would like to thank BP Solar for their support on this project and CER would like to thank Corning for their NPSC Fellowship support. Thanks also to Bob Reedy at the National Renewable Energy Lab for his SIMS expertise which helped us to identify and resolve our contamination issues.

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